DESIGN-FOR-TESTABILITY (DFT) TECHNIQUE FOR OPEN FAULTS IN CMOS LATCH/FLIP-FLOP

By

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Dissertation submitted in partial fulfillment of
the requirements for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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Approved by.

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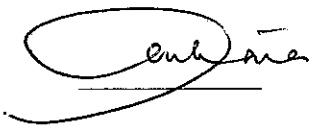
Universiti Teknologi PETRONAS

Tronoh, Perak

June 2008

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



MARLIANA BINTI MOHAMMAD

ABSTRACT

In this report, CMOS D-latch with and without open faults are designed. Schematics and layout are simulated using Cadence Spectre. The process parameter used in design is Technology AMI06. The results obtained from the simulation are observed for both cases (with open and without open fault). It is proven that there are certain open locations in CMOS D-latch could not be detected instantly. This is where the purpose of designing the DFT comes in. DFT circuitry is added to the D-latch to create voltage competition in the circuit. With DFT circuitry implemented in the D-latch, the open fault can be detected easily. From observation, the output at the memory state is flipped during testing. The layout for D-latch with added DFT circuitry is also included.

ACKNOWLEDGEMENT

I would like to take this opportunity to acknowledge and thank everyone that has given me all the supports and guidance throughout the whole period of completing the final year project. Firstly, many thanks to the university and the Final Year Project coordinators that have coordinated and made the necessary arrangements for this study.

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LIST OF ABBREVIATIONS

CMOS – Complementary Metal-Oxide Semiconductor

DFT – Design For Testability

CPU – Central Processing Unit

I_{ddq} – Quiescent Power-Supply Current

I_{DDT} – Transient Power-Supply Current

D-Latch – Data Latch

W/L – Ratio Of Width Over Length

V_{dd} – Drain-To-Drain Voltage

GND -- Ground

DRC -- Design Rule Check

LVS -- Layout Versus Schematic

CHAPTER 1

INTRODUCTION

1.1 Background Of Study

CMOS (Complementary metal-oxide semiconductor) is the semiconductor technology used in the transistors that are manufactured into most of today's computer microchips [8]. Design-for-testability (DFT) is a name for design techniques that add certain testability features to a microelectronics hardware product design. In this project, both concepts will be applied to the working process.

1.2 Problem Statement

The impact of resistive-opens is increasing with the latest technologies due to the increase in the number of interconnection layers and connections between layers. CMOS circuit opens are a result of various failure mechanisms during fabrication, resulting in actual breaks in the interconnect wires etc [1]. Memory elements like latches and flip-flops are widely used in the design of CMOS integrated circuits. Resistive opens affecting certain branches are undetected by logic and delay testing [2].

Since the technology nowadays is growing so fast, there is an increased need to evolve the design-for-testability technique for open faults in CMOS circuit. For this project, the DFT technique will be designed by using Cadence Spectre simulator.

1.3 Objectives

To design and simulate a CMOS latch with and without open faults.

CMOS latch will be designed using Cadence Spectre schematic. A schematic of CMOS with open fault will be compared to CMOS without the open fault to observe the difference in simulating.

To design the (DFT) technique for open faults in CMOS latch.

The DFT technique to test the open fault in the designed CMOS latch will be designed using the same software (Cadence Spectre). The designed DFT should be able to achieve the desired result which is to detect the open fault in CMOS.

To be able to simulate the DFT designed with Cadence Spectre simulator.

The designed DFT will be simulated using the Cadence Spectre simulator. The result should shows that the designed DFT is successful in detecting the open fault.

1.4 Scope Of Study

This project involved seeking information and research on the behavior of CMOS with open faults. A DFT to test the fault will be designed and simulated. Specifically, the study/project scope involved:

- Research on the information regarding resistive-open faults in CMOS circuit.
- Research on the previous DFT that others have designed.
- Designing CMOS circuit with and without open faults.
- Designing and simulate the DFT circuitry with the designed CMOS circuit.
- Designing layout from designed schematic.

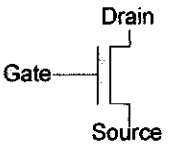
CHAPTER 2

LITERATURE REVIEW

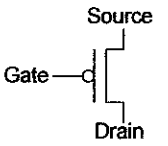
2.1 Complementary MOS (CMOS)

In CMOS technology, both p-type (PMOS) and n-type (NMOS) transistors are used to realize logic functions [17]. NMOS is an n-channel MOSFET and uses negatively charged electrons for electrical current flow. The circuit symbol for NMOS is shown in Figure 1(a). The gate terminal acts as the control electrode for the device. Applying a voltage on the gate electrode determines the current flow between the drain and source terminals.

PMOS uses positive charges for current flow. The circuit symbol for PMOS is shown Figure 1(b). The voltage applied to the gate determines the current flow between the source and drain terminals.



(a)



(b)

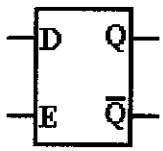
Figure 1: (a) NMOS (b) PMOS

CMOS logic circuits are based on the concept of using complementary pairs of transistors for switching [13]. If an input signal creates a path through the PMOS to V_{dd}, this will yields a high or logic 1 output. When the input creates a path through NMOS to GND, the output obtained will yields a low or logic 0.

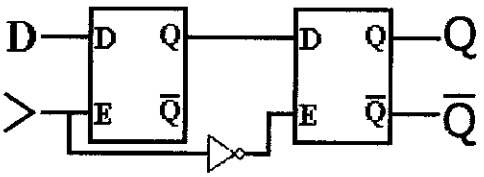
2.2 Latches/Flip-Flops

Several IC designs consist of latches and flip-flops circuit [4]. The basic principle of those circuits is it has an output which can be toggled between two states depending on the circuits' behavior [7][9]. Once the input is put in one state, it remains there until a change in the inputs causes it to toggle again.

A latch is a device that can receive and hold an input bit [9]. A simple D-latch forms the basis for many designs. The symbol of the D-latch is shown in Figure 2(a). The latch is transparent as a change in D is seen at the outputs after a circuit delay time. The design is based on the characteristic of the simplest static storage configuration called bistable circuit. A bistable circuit is one that can store either logic 0 or logic 1.



(a)



(b)

Figure 2: (a) D-latch symbol (b) D flip-flop symbol

A flip-flop differs from a latch in that it is non-transparent. Non-transparent means a change in D is cannot be seen at the outputs after a circuit delay time [4]. The D-type flip-flop is the most commonly used in CMOS circuit. The basic D flip-flop is a master-slave configuration obtained by cascading two oppositely phased D-latches. The clock signal controls the operation and provides synchronization. The symbol is shown in Figure 2(b).

2.3 Open Faults

CMOS opens are a result of various failure mechanisms during fabrication, resulting in actual breaks in the interconnect wires. [1] has stated that when the resistance in CMOS circuit have a high value, they result in stuck-opens which cause a memory behavior of the node; moderate resistances can be modeled on delay defects.

The stuck-open fault in transistor occurs when the drain or source contact is open [10]. In the stuck open fault model, the transistors are modeled as being permanently open [5], causing a memory effect in the circuit [12]. Despite of having this fault, the latch is still giving the correct output.

A resistive open appears when the conductive material is not completely broken [6]. Usually the open in CMOS circuit is modeled with resistance which can take various ranges of values. Resistive opens in gates can be classified in three cases [3] which are multiple open gates, single open gate in clock signal and single open gate in data signal.

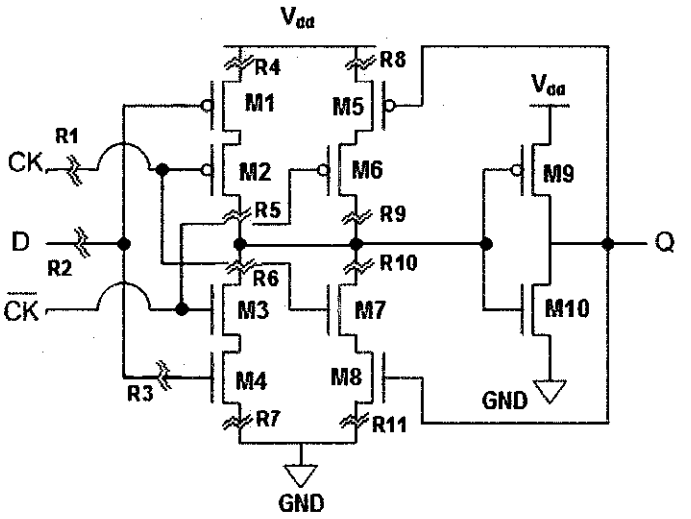


Figure 3: Possible open locations in D-latch

Possible open locations in D-latch are shown in Figure 3 [11]. An example of multiple open gates is R2. It is said so because D signal goes as input to both M1 and M4. If open exist in the path of D, it causes open to both M1 and M4, thus the name multiple open gates. As for single open gate in clock signal, the example can be observed at R1. R1 is in the path of clock signal, if the resistance here is high, it creates an open gate for clock signal. The same goes for single open gate in data signal, R3. The data signal is accepted at M1 but not at M4.

2.4 Other Design-For-Testability Methods

Throughout the years, several improvements have been made to open fault models and several studies have been done in fault testing. When considering CMOS technology, open fault becomes a significant one [10]. The fault model deals with physical failures producing a permanent conduction (open).

There are several methods have been proposed over the years on how to detect the faults happen in CMOS [2]. Some of the famous methods are:

1) I_{ddq} (Quiescent power supply current) Test: CMOS circuit uses very little power and in standby mode, it draws practically nothing, just the leakage current. Therefore, CMOS circuits with increased leakage current are defective. Such a defect causes current to increase and affect the functionality, the lifetime and the reliability of the circuit. The concept of I_{ddq} test is to validate circuit by measuring and observing the quiescent supply current [18]. I_{ddq} test can be used to detect several faults such as bridging faults, gate oxide defects and some stuck-open faults. One of the disadvantages with this method is that the measurement must be very precise since normal I_{ddq} is very low [15]. This measurement takes a significant amount of time. Other disadvantage is the circuit under test must contain all static devices or else the I_{ddq} will be very high even there is no fault in the circuit.

2) I_{DDT} (Transient power supply current) Test: I_{DDT} refers to the current drawn from the power supply during transient switching of CMOS gates [14][15]. It depends on the switching activity during state transitions. When a circuit switches states, a momentary path is established between the supply line V_{dd} and GND. It takes quite some time for the internal node signals to stabilize, this is when I_{DDT} is resulted. I_{DDT} testing is done by measuring the average transient current of the power supply during the

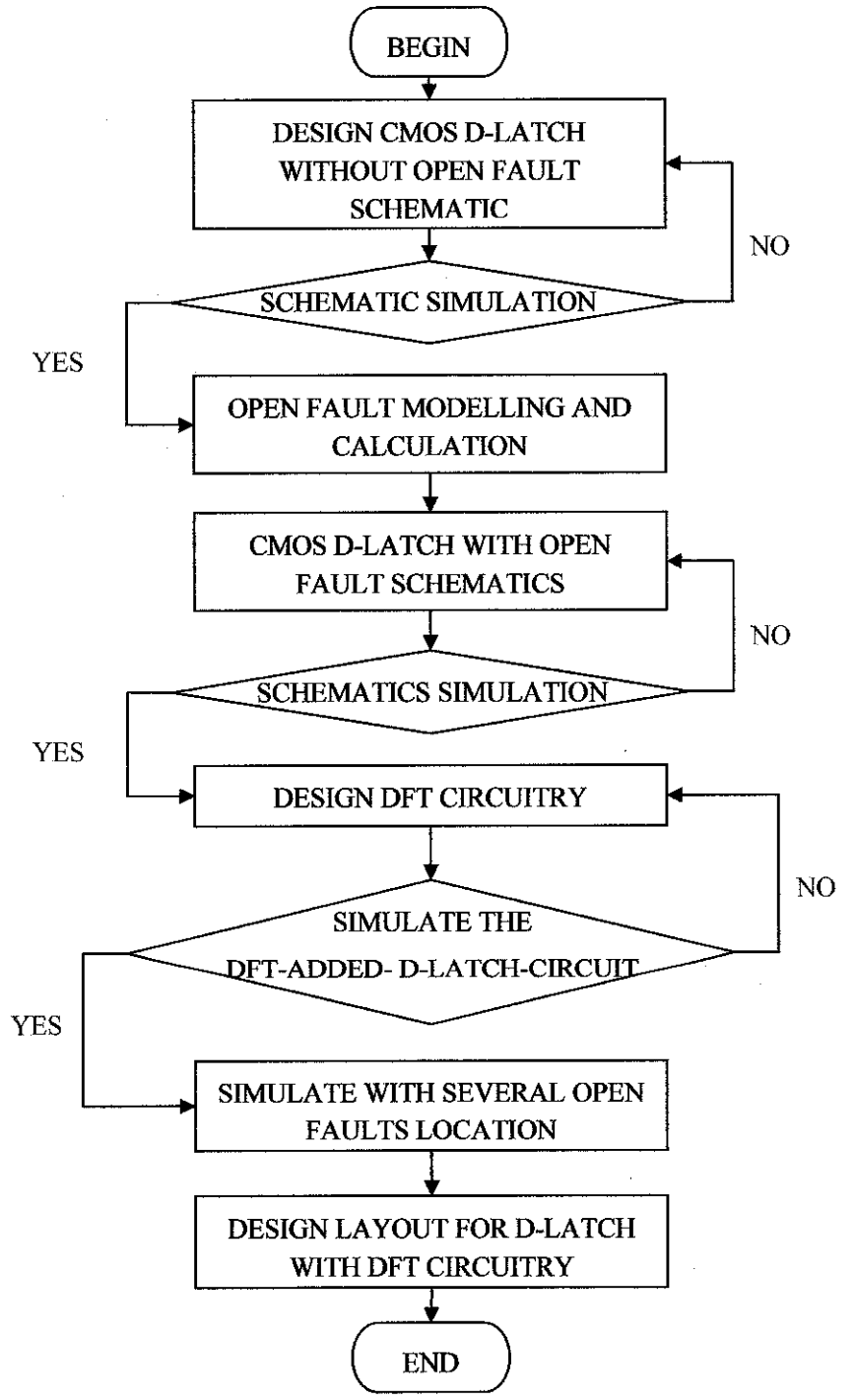
interval from the input change to stable state. The disadvantage of this method is it is difficult to differentiate normal system current transitions and defect results. This is because the circuit test would share power supply rails with other circuits in chip. Thus the fault is undetected due to I_{DDT} pulses from switching in other parts of the chip.

3) Test pattern: The method is to first initialize the gate output and then test for the existence of an open circuit. Generally, stuck-open faults require a sequence of two consecutive patterns to guarantee a test. Testing for stuck-open in P-transistor requires presetting the output node to logic 0 via a set-up pattern. Then, applying a test pattern that creates a conducting path to reserve the state to logic 1 and vice versa. There are several weaknesses for this method [16]. First, the timing errors due to differential path delays can cause upsets of the initializing pattern. Second, the test pattern takes longer detection time. Also, if the test patterns are applied at normal speed, the open cannot be detected as the circuit behaves as a dynamic latch. The detection cannot be guaranteed even if the test speed is slowed down [10].

CHAPTER 3

METHODOLOGY

3.1 Project Flowchart



3.2 CMOS Latch Without Open Faults

For the first part of the project, D-latch needs to be designed in analog CMOS using Cadence Spectre software. There are several ways to design the D-latch. To create D-latch, an entry node for the input bit is a must.

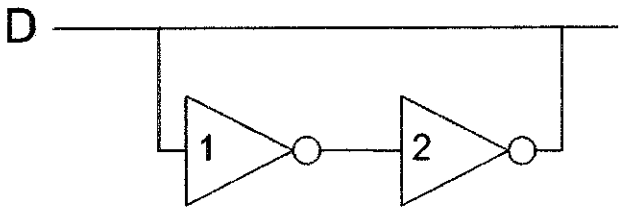


Figure 4: Basic input of latch

The value of D is held by the circuit formed by the inverter pair as in Figure 4. The presence of the feedback loop from the output of inverter 2 to the input of inverter 1 provides the desire latching. Clocked CMOS is used to synchronize the data flow by controlling the internal operation of the gate. Every cycle of clock allows a new group of data bits to enter the network.

The latch in Figure 5 uses clocked CMOS inverter as the input stage with clock CK controlling the loading. M1 and M4 are CMOS components for inverter 1. M5 and M8 are CMOS components of inverter 2.

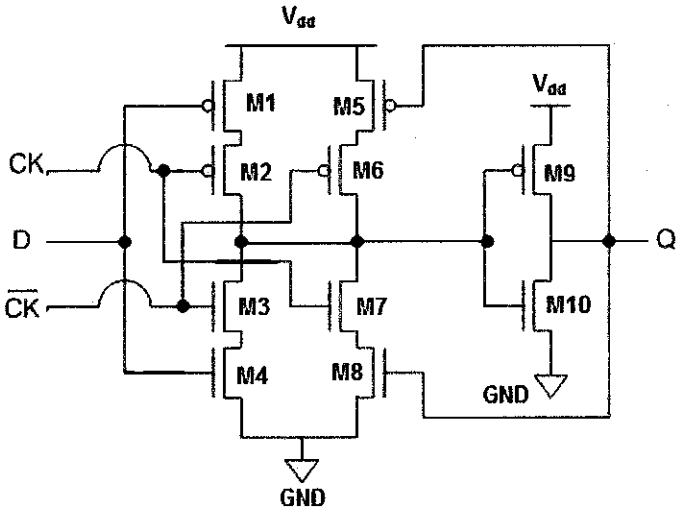


Figure 5: D-latch

When CK = 0, D is admitted into the circuit where it passes through the static inverter, M1 and M4 in Figure 6. When the clock makes a transition to CK = 1, the first stage is driven into Hi-Z state while the feedback loop is closed by the oppositely phased inverter, M5 and M8. This holds the output until the next clock cycle.

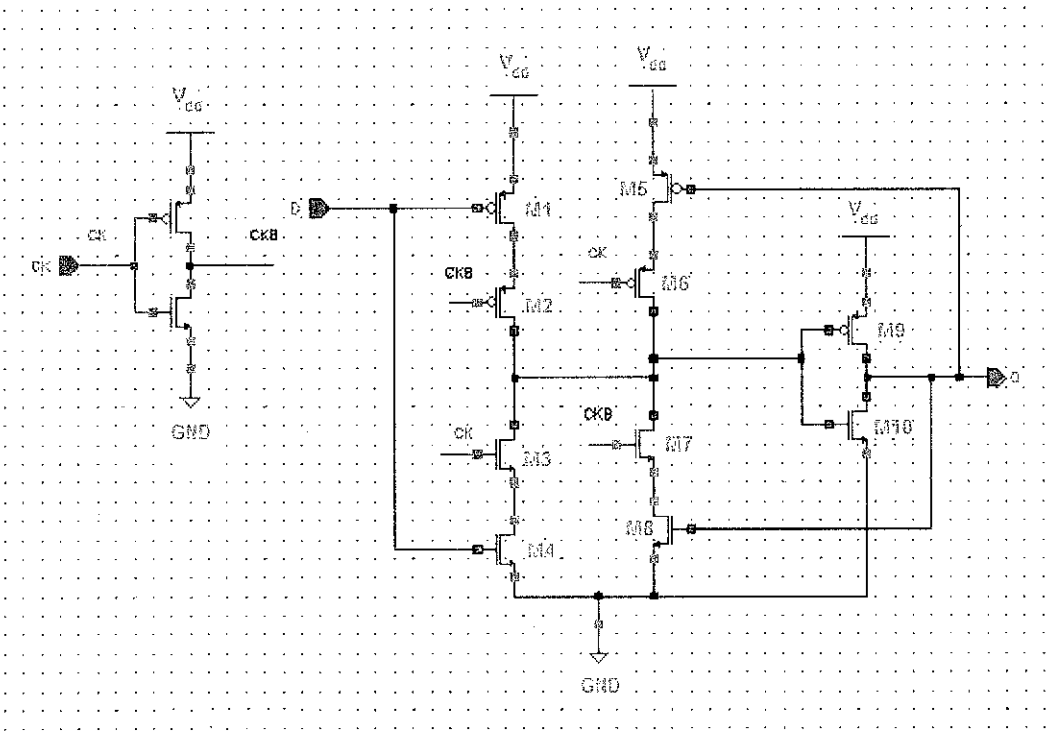


Figure 6: D-latch schematic in Spectre

3.3 CMOS Latch With Open Faults

After designing CMOS latch without open faults, next is to design one with the open faults. Open in CMOS circuit is modeled with resistance which can take various ranges of values. Diode-connected NMOS is used to model the open. The resistance value can be calculated using equation below:

$$R_N = \frac{1}{\beta_N (V_{DD} - V_{TN})}$$

Figure 7: Diode-connected NMOS

The calculation for R = 100 MΩ, R = 100 kΩ, R = 50 kΩ, R = 30 kΩ and R = 10 kΩ is given in Appendix 1.

There are certain locations in CMOS that are undetectable. Figure below shows the possible open locations in D-latch. There are more examples of open fault locations in CMOS circuit in Appendix 2. These locations are undetectable as shown in Chapter 4.

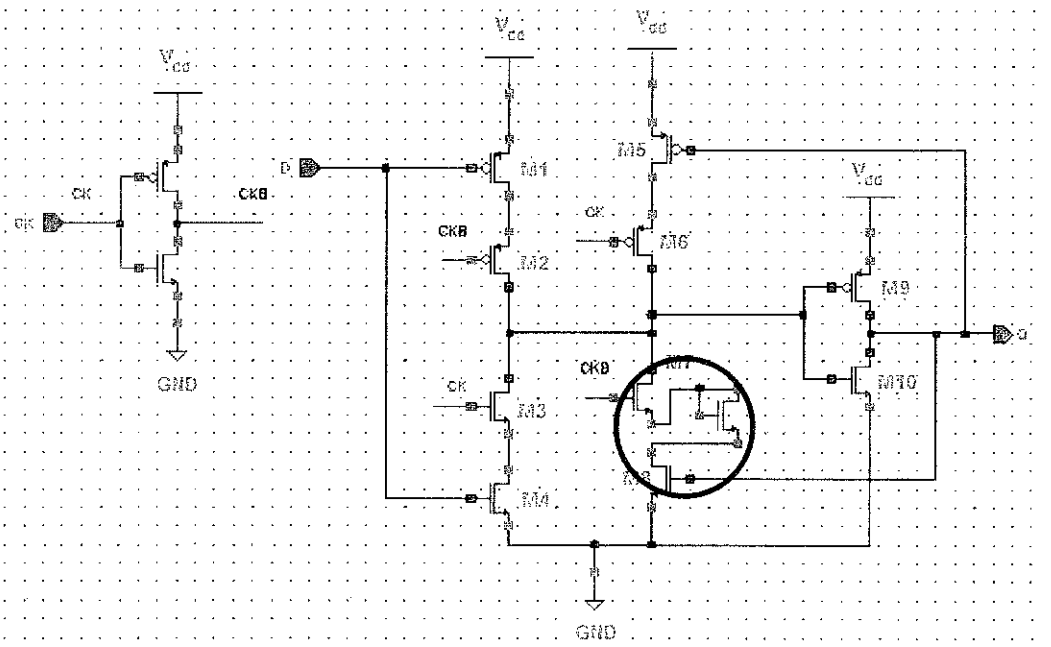


Figure 8: Open fault in CMOS latch

3.4 Designing DFT Circuitry

DFT circuitry is designed by adding two transistors which are controlled by two complementary inputs (Figure 9). Input S controls PMOS transistor and input SB controls NMOS transistor. Adding the circuitry to the D-latch circuit will create a voltage competition between the three networks (P-DFT, N-DFT, and the branch under test). The simulation result is shown in Chapter 4.

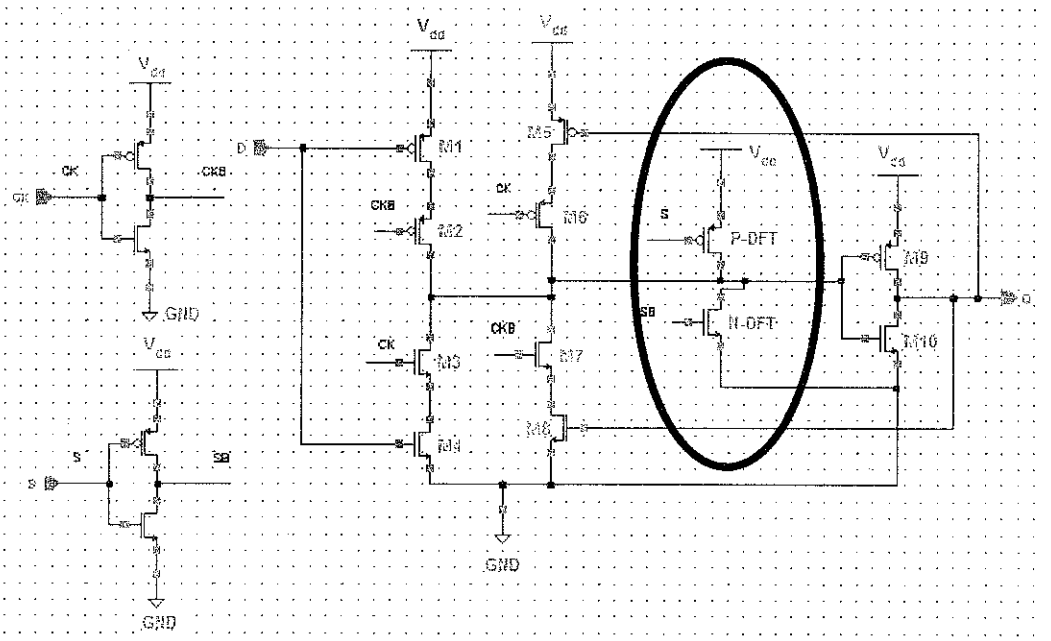


Figure 9: D-latch with DFT circuitry

To test the opens using the DFT circuitry, for NMOS (PMOS) the state is initialized to logic 1 (logic 0). N-DFT and P-DFT are activated and then deactivated as to invoke the circuit stabilization. The output of the circuit is observed in order to determine the fault detection.

3.5 Designing Parameters

The process parameter used in this project is Technology AMI06. In all the schematics, same parameters are used as to ensure that the results are as predictable. The designed transistor sizes (W/L) for NMOS is (3μ/600n)m and for PMOS is (1.5μ/600n)m. V_{dd} is set to 3 V. Parameters in CLOCK and DATA input signal are as follows:

Table 1: CLOCK, DATA, S parameters

PARAMETER	CLOCK	DATA	S
Voltage 1	0 V	2 V	2 V
Voltage 2	2 V	0 V	0 V
Rise time	0.1 ns	0.1 ns	0.1 ns
Fall time	0.1 ns	0.1 ns	0.1 ns
Pulse width	1 ms	1 ms	1 ms
Pulse period	2 ms	3 ms	2 ms

Since the pulse period is set to 3 ms, the input pattern fed to the CMOS D-latch is 011011011…and so on.

3.6 Designing Circuit Layout

Physical design is the actual process of creating circuits on silicon. Every layer in CMOS fabrication sequence is defined by a distinct pattern. The process of physical design is performed using layout editor. The completed circuit layout for D-latch with DFT circuitry is designed manually in Cadence Virtuoso using Technology AMI06. All the parameters such as transistors widths and lengths are the same with the schematic. Design Rule Check (DRC) and Layout Versus Schematic (LVS) results are given in Appendix 3.

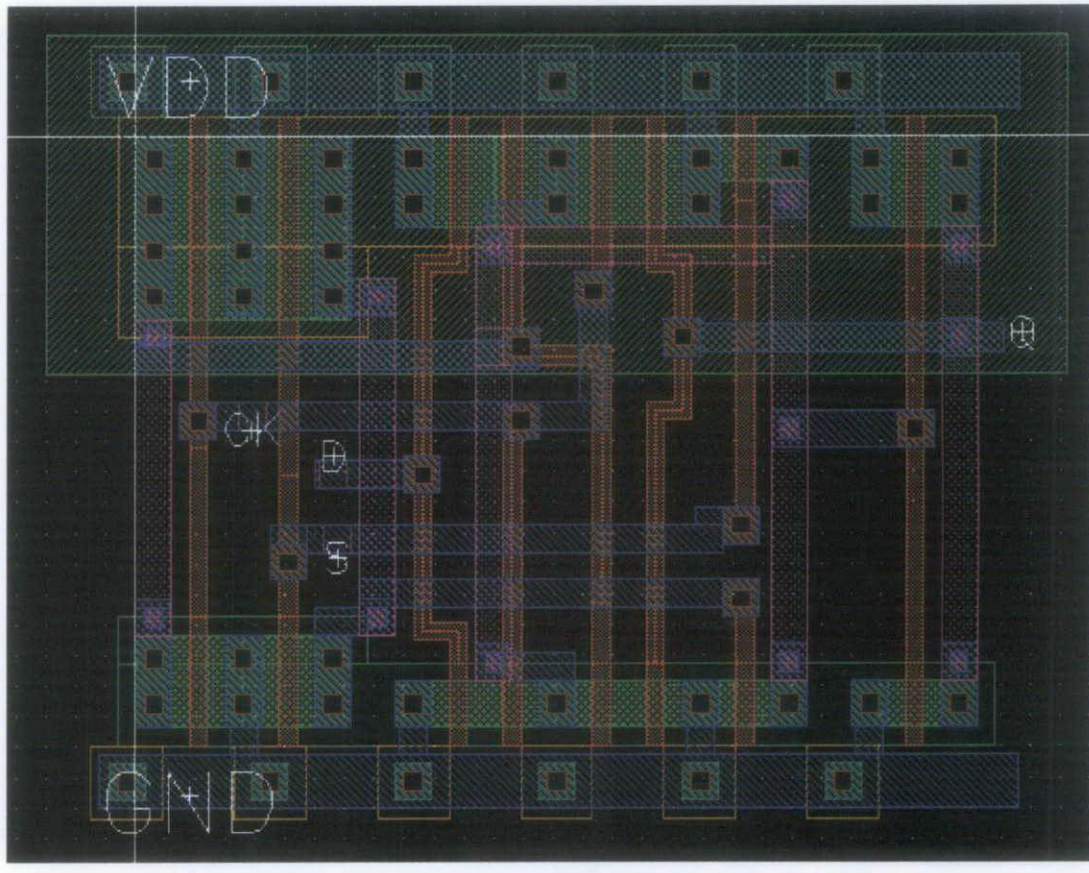


Figure 10: D-latch with DFT circuitry layout

CHAPTER 4
RESULTS AND DISCUSSION

4.1 Simulation Result For D-Latch Without Open Faults.

The simulation of the D-latch in CMOS implementation is shown below:

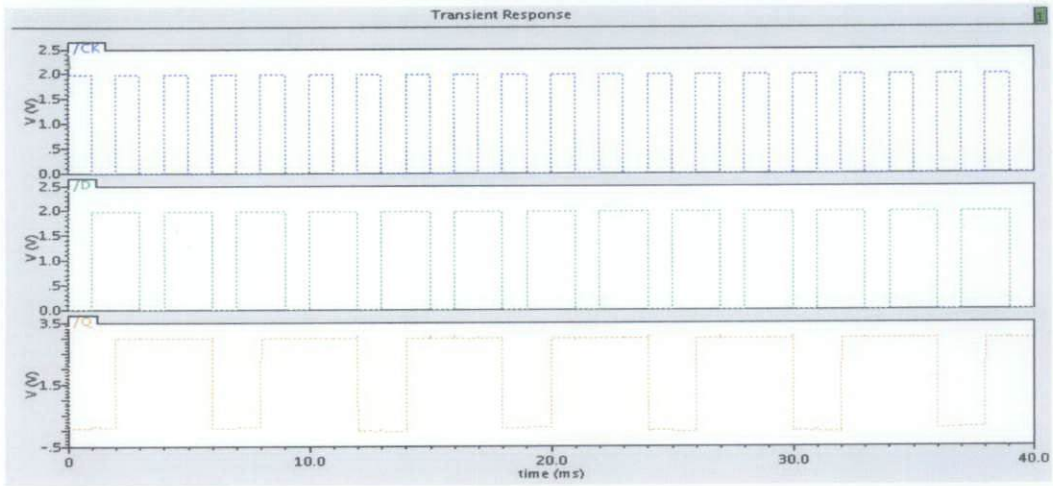


Figure 11: Inputs and output of D-latch in CMOS implementation

In Figure 11, the behavior of the output, Q is observed to be at 'low' state when CLOCK = 1 and DATA = 0. This means whenever the CLOCK = 1 (high), the output Q will follow the state of DATA. For CLOCK = 0 (low), it does not matter what the D input, the output, Q is unaffected and remain in it prior state. This is due to the memory behavior of D-latch. The truth table for the designed D-latch is shown in Table 2.

Table 2: Truth table for D-latch

Inputs		Output
CLK	D	Q
1	0	0
1	1	1
0	X	Q

4.3 Simulation Result For D-Latch With DFT Circuitry.

The simulation result for D-latch with DFT circuitry (from Figure 9) is shown below:

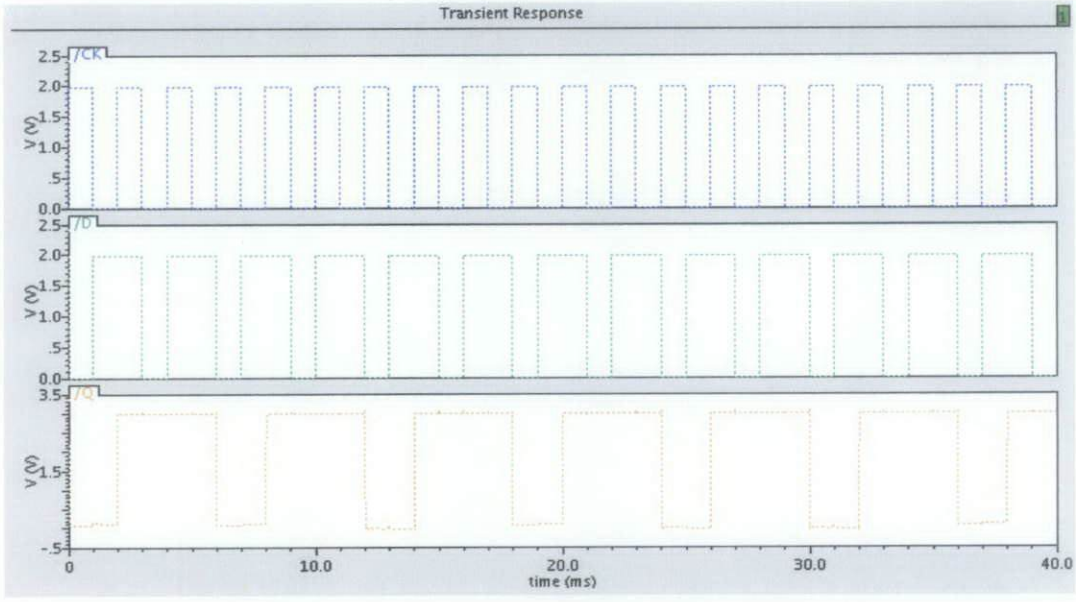


Figure 13: Inputs and output of D-latch with DFT circuitry

It is observed from Figure 13 that there is no difference in the output after the DFT circuitry is added. This shows that the DFT circuitry will not affect the operation of the D-latch.

Next, to prove that with this DFT circuitry the open fault in CMOS D-latch is detectable, open fault is simulated in NMOS, PMOS and both areas.

4.4 Testing Open Fault In NMOS area.

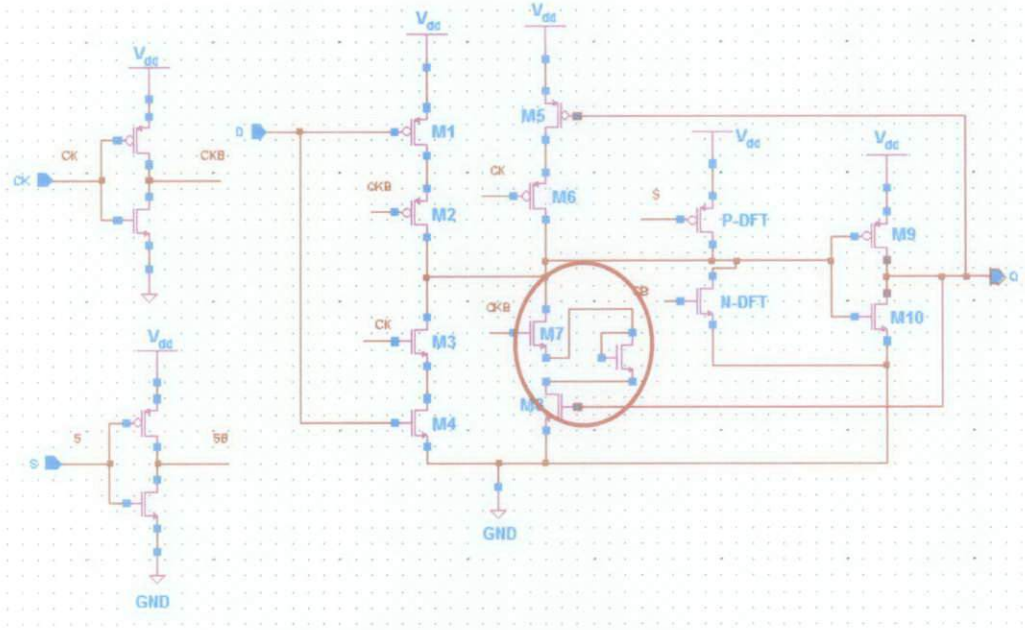


Figure 14: Open fault in NMOS area.

Open fault is created in NMOS area between M7 and M8. The simulation result for Figure 14 is shown below:

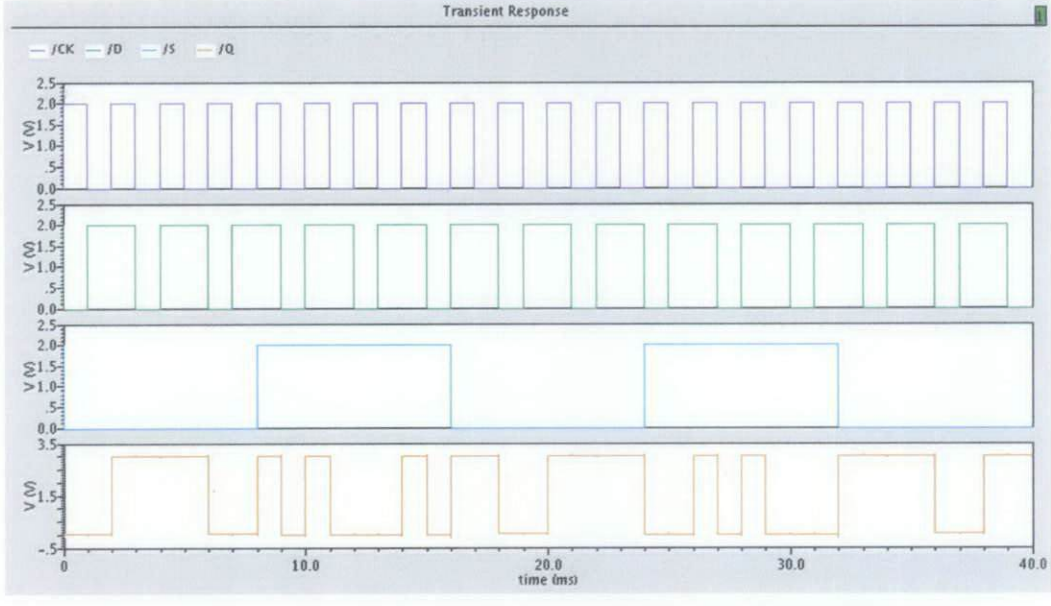


Figure 15: Inputs and output of D-latch with open fault in NMOS area.

From the simulation result in Figure 15, the output shown is not the same as in Table 2. The observed output Q, flipped its memory state when S = 1. The flipped state happens only when the circuit tries to retain logic 1 (high). This is due to the fact that NMOS is a pull-down circuit which it is weak at logic 1.

4.5 Testing Open Fault In PMOS area.

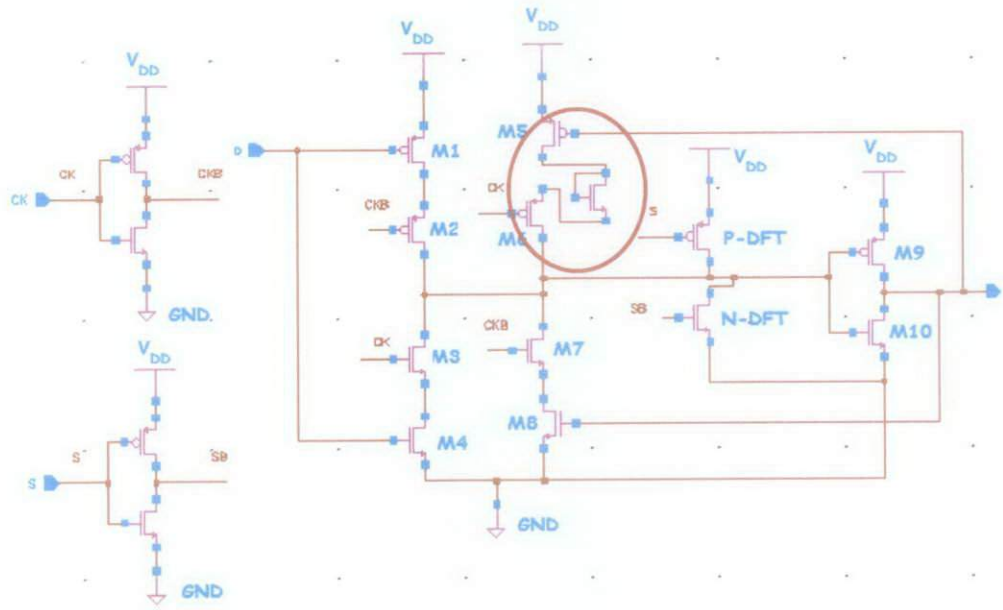


Figure 16: Open fault in PMOS area.

Open fault is created in PMOS area between M5 and M6. The simulation result for Figure 16 is shown in Figure 17.

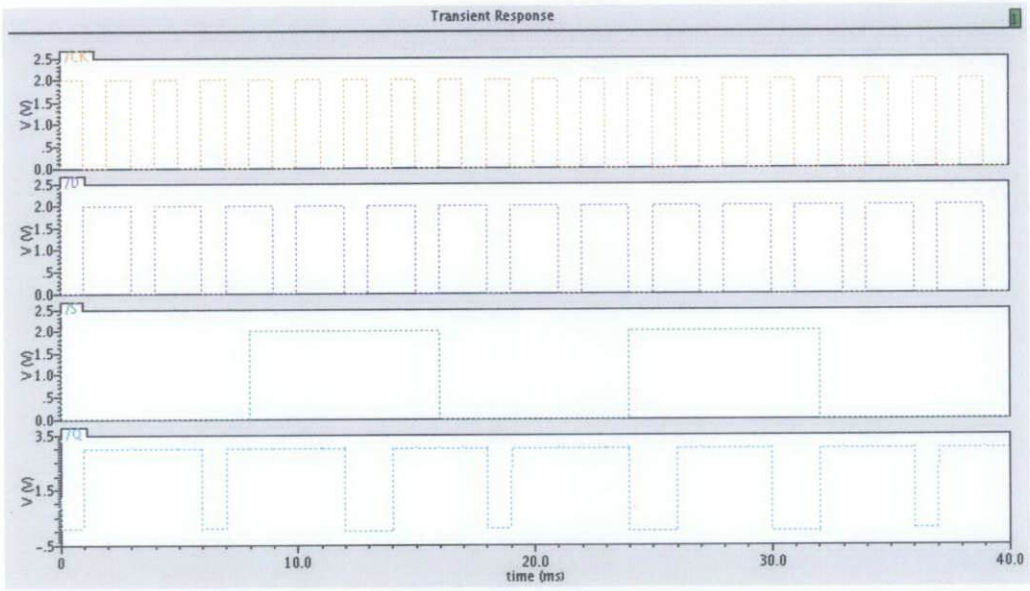


Figure 17: Inputs and output of D-latch with open fault in PMOS area.

From the simulation result in Figure 17, the output shown is not the same as in Table 2. The observed output Q, flipped its memory state when S = 0. The flipped state happens only when the circuit tries to retain logic 0 (low). This is due to the fact that PMOS is a pull-up circuit which it is weak at logic 0.

4.6 Testing Open Faults In NMOS and PMOS areas.

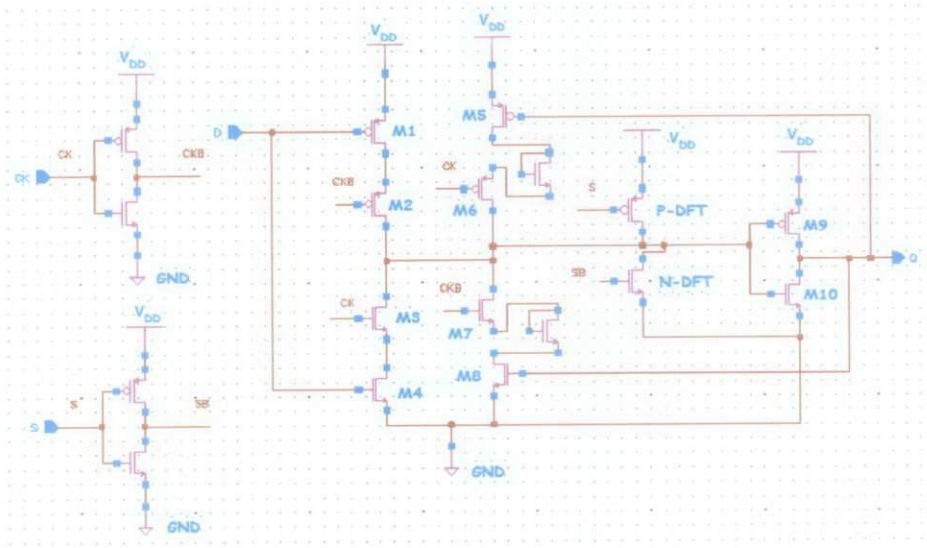


Figure 18: Open faults in NMOS and PMOS areas.

Open fault is created in NMOS area between M7 and M8, and PMOS area between M5 and M6. The simulation result for Figure 18 is shown in Figure 19.

Figure 19: Inputs and output of D-latch with open fault in NMOS and PMOS areas.

From the simulation result in Figure 19, the output shown is not the same as in Table 2. The observed output Q, flipped its memory state when S = 0 for PMOS and S = 1 for NMOS. The flipped state happens only when the circuit tries to retain logic 0 (PMOS) or logic 1 (NMOS).

Schematic and simulation result for D flip-flop is given in Appendix 2.

In order to observe the output behavior for different range of resistance values, the diode-connected NMOS is adjusted to give resistance value of R = 100 MΩ, R = 100 kΩ, R = 50 kΩ, R = 30 kΩ and R = 10 kΩ. Figures below show the output, Q comparison with defect free circuit.

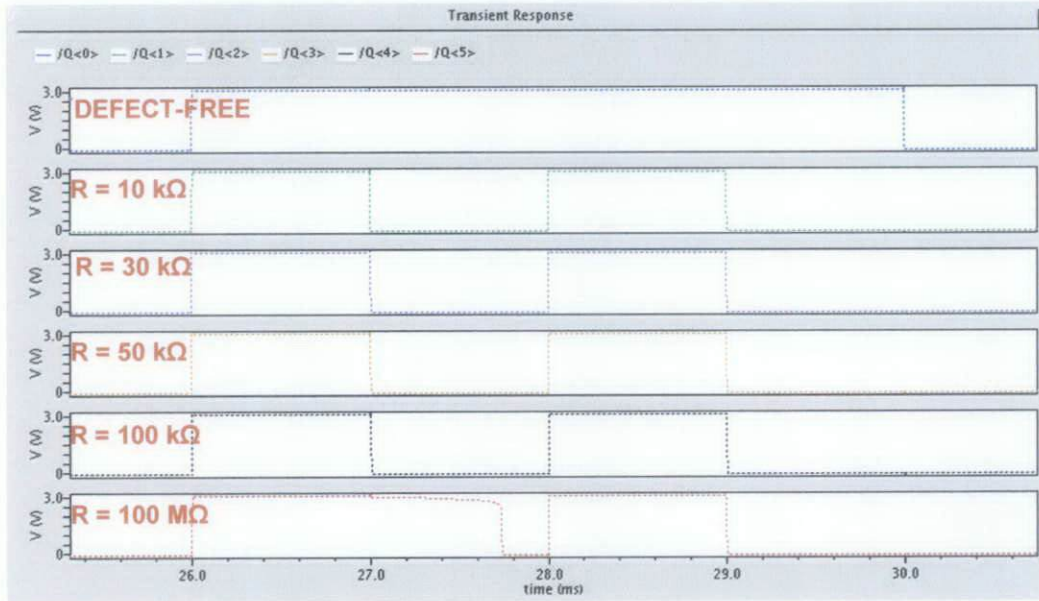


Figure 20: Simulation results comparison for R = 100 MΩ, R = 100 kΩ, R = 50 kΩ, R = 30 kΩ and R = 10 kΩ.

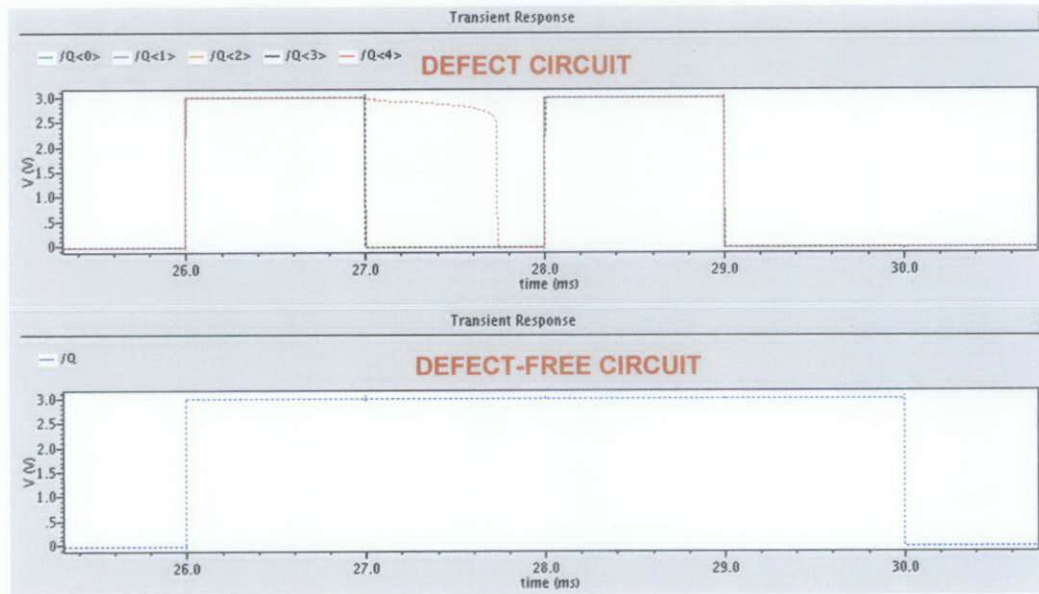


Figure 21: Comparison between defect and defect free circuit output

The simulation results show that the outputs for defect circuits are different from defect-free circuit simulation graph. Resistive-opens in NMOS branch is detected by N-DFT complimentary with P-DFT for resistive-opens in PMOS branch. S = 0 will activate the N-DFT. During the activation, there is a competition of the three networks (1) P-DFT, (2) N-DFT and (3) the branch under test (Figure 22). This causes the strength at the testing branch to decrease.

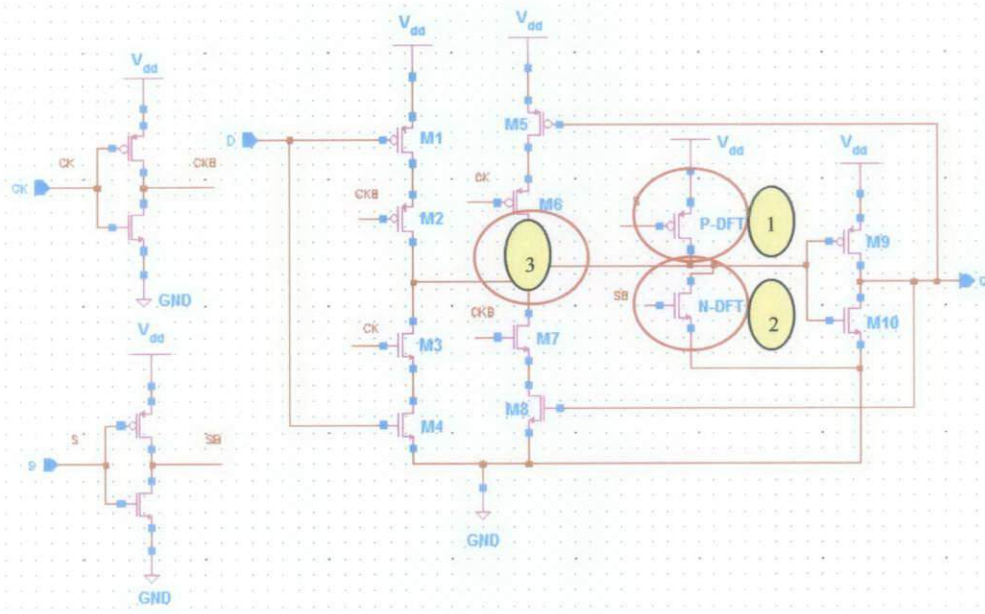


Figure 22: Networks under test

During the deactivation, the circuit tries to stabilize its state. The resistive opens flipped the state of the CMOS latch during memory phase. For NMOS (PMOS) area, the flipped state only happens when the initial state is 1 (0). Thus, the open fault is detected.

CHAPTER 5
CONCLUSION AND RECOMMENDATION

5.1 Conclusion

The simulation result shows that the output Q behaves as desired that is to follow the Data state when the CLOCK is high and to remain its state when the CLOCK is low. However, there are certain open branch situations which give the same output as a defect-free D-latch. This case is adverse in fabrication as this will lead to latent failure. Latent failure must be avoided to maintain the quality of the fabricated products. DFT plays its role in this design where its function is to detect the open branch and give the result at the output. The principle of the DFT is basically to manipulate the voltage strength between the P-DFT, N-DFT, and the branch under test.

5.2 Recommendation

For future works, more fault detections should be implemented on the DFT circuitry. The proposed DFT technique can be improved more by considering the sizing or the location of the circuitry. One should consider on how to optimize the use of the DFT in fault testing and its affect on the performances.

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APPENDIX 1

CALCULATION FOR RESISTIVE OPEN MODEL

$$R_n = \frac{1}{ß_n (V_{DD} - V_{Tn})}$$

$V_{DD} = 3$ V. $V_{Tn} = 0.7086$ V.

$V_{DD} - V_{Tn} = 3 - 0.7086$ V $= 2.2914$ V.

$C_{ox} = \varepsilon_{ox} / t_{ox} = (3.9)(8.854e^{-14}) / (1.41e^{-8}) = 2.449e^{-5}$ F/cm².

$k'_n = \mu_n C_{ox} = (533.6953445)\ (449e^{-5}) = 0.01307$ A/V².

$ß_n = k'_n (W/L)$

For R = 10 kΩ,

$ß_n = 1 / (R_n)\ (VDD - V_{Tn}) = 1 / (10k)\ (2.2914) = 4.3641e^{-5}$ A/V².

$(W/L) = 4.3641e^{-5} / k'_n = 4.3641e^{-5} / 0.01307 = 3.3391e^{-3}$

If L is fixed at 600 nm, therefore $W = 3.3391e^{-3} \times 600n = 2$ nm.

But Spectre has defined that the minimum value for W is 1.5 µm. Any values less than the minimum value will be defined as zero. So, for the purpose of getting the resistance value of R = 10 kΩ only, W will be fixed at W = 1.5 µm. L will be calculated as $L = W / 3.3391e^{-3} = 4.4922e^{-4}$ m.

For R = 30 kΩ,

$ß_n = 1 / (R_n)\ (VDD - V_{Tn}) = 1 / (30k)\ (2.2914) = 1.4547e^{-5}$ A/V².

$(W/L) = 1.4547e^{-5} / k'_n = 1.4547e^{-5} / 0.01307 = 1.1130e^{-3}$

$L = W / 1.1130e^{-3} = 1.3477$ mm.

For R = 50 kΩ,

$ß_n = 1 / (R_n) (VDD - V_{Tn}) = 1 / (50k) (2.2914) = 8.7283e^{-6}$ A/V².

$(W/L) = 8.7283e^{-6} / k'_n = 8.7283e^{-6} / 0.01307 = 6.6781e^{-4}$

$L = W / 6.6781e^{-4} = 2.2461$ mm.

For R = 100 kΩ,

$ß_n = 1 / (R_n) (VDD - V_{Tn}) = 1 / (100k) (2.2914) = 4.3641e^{-6}$ A/V².

$(W/L) = 4.3641e^{-6} / k'_n = 4.3641e^{-6} / 0.01307 = 3.3391e^{-4}$

$L = W / 3.3391e^{-4} = 4.4922$ mm.

For R = 100 MΩ,

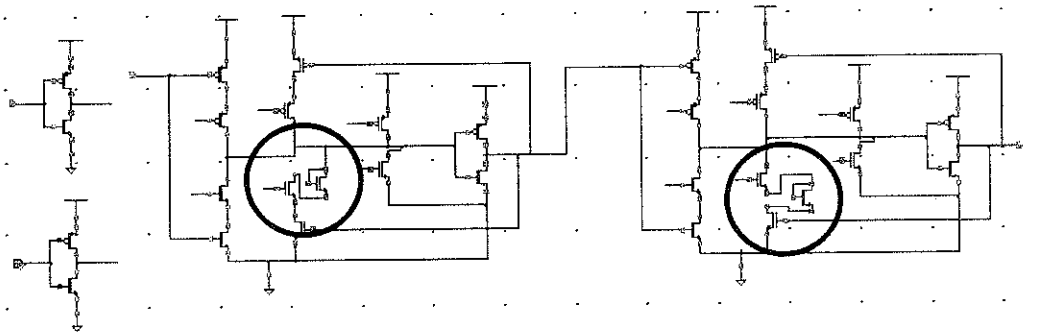
$ß_n = 1 / (R_n) (VDD - V_{Tn}) = 1 / (100M) (2.2914) = 4.3641e^{-9}$ A/V².

$(W/L) = 4.3641e^{-9} / k'_n = 4.3641e^{-9} / 0.01307 = 3.3391e^{-7}$

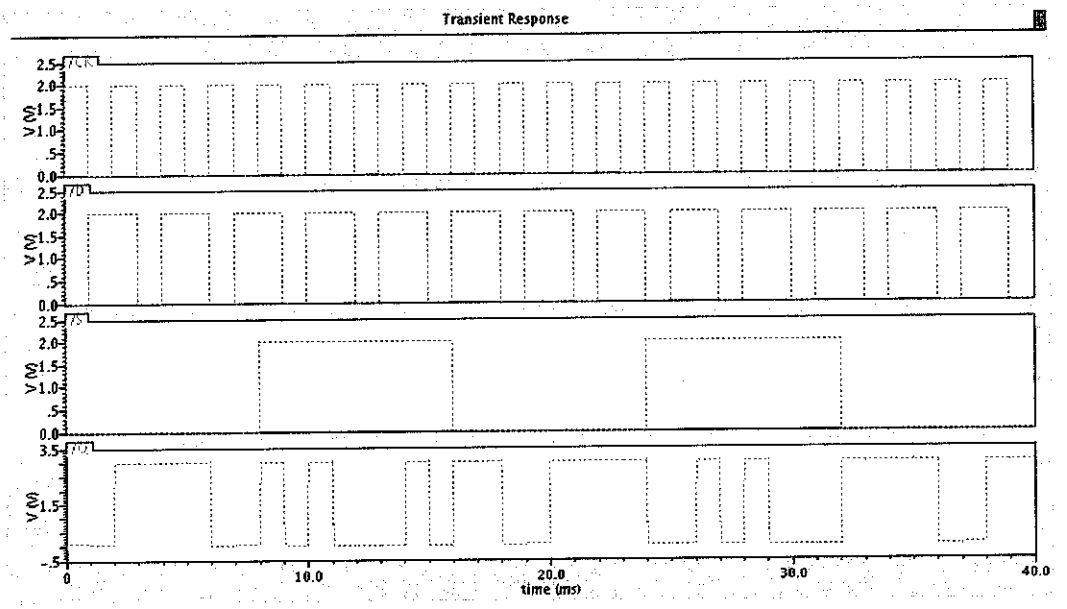
$L = W / 3.3391e^{-7} = 4.4922$ m.

APPENDIX 2

TESTING OPEN FAULTS IN D FLIP-FLOP



D Flip-flop Schematic with open faults

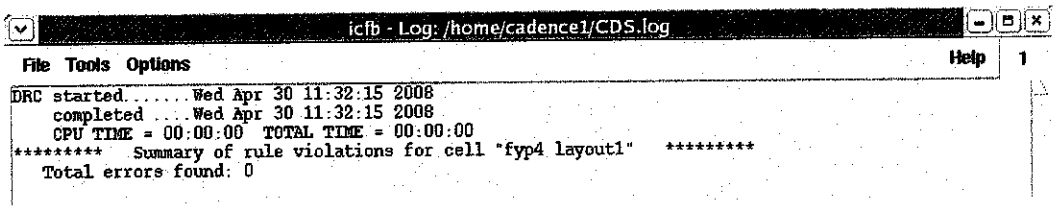


Simulation result

The open faults are created in NMOS areas. The observed output Q, flipped its memory state when S = 1. The flipped state happens only when the circuit tries to retain logic 1 (high).

APPENDIX 3

LAYOUT DESIGN RULE CHECK (DRC) RESULT



APPENDIX 4
LAYOUT VERSUS SCHEMATIC (LVS) RESULT

/home/cadence1/LVS/si.out

File Help 16

```
@(#)$CDS: LVS.exe version 5.1.0 02/06/2007 19:59 (cicln01) $

Command line: /cadence_autofs/cadence_binary/IC5141ISR20070210/tools.lnx86/dfII/bin/32bit/LVS.exe -dir /home/c
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/cadence1/LVS/layout/netlist
       count
         13              nets
         4               terminals
         8               pmos
         8               nmos

    Net-list summary for /home/cadence1/LVS/schematic/netlist
       count
         13              nets
         6               terminals
         8               pmos
         8               nmos


    Terminal correspondence points
    N7          N6          CK
    N11         N9          D
    N10         N10         Q
    N5          N5          S

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4


The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   16      16
        total                    16      16

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   13      13
        total                    13      13

                                 terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    4       6


Probe files from /home/cadence1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:
```

```
Probe files from /home/cadence1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/cadence1/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```