PROCESS TOMOGRAPHY

by

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FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
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CERTIFICATION OF APPROVAL

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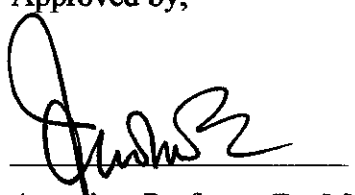
Approved by,



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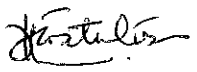
TRONOH, PERAK

June 2006

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



Maizatul Niza binti Zainal

ABSTRACT

Process tomography is a process of measuring the signals by using specific types of sensor, which are arranged around an object as to examine its internal condition. A number of principles can be applied in process tomography including optical tomography, resistive tomography, and acoustic tomography. This report describes the design of hardware system for electrical capacitance tomography. The electrical capacitance tomography is defined by measuring the electrical properties of dielectric components in a specific object via capacitive sensors. In this project, the hardware system is designed based on two major parts; sensor system and data acquisition system. A number of experiments have been conducted in order to obtain the best design of the sensor system and data acquisition circuits. Further improvements are suggested for future works.

ACKNOWLEDGEMENT

I would like to express my gratitude to the Almighty for giving me the strength and courage in completing the project entitled 'Process Tomography'.

Here, I dedicate my utmost appreciation to my project supervisor Associate Professor Dr. Mohd Noh Karsiti, who has guided me during the completion of this project and patiently examine my work into the details in order to produce an outstanding project and paperwork.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

2-D	Two dimensional
3-D	Three dimensional
A_{OL}	Open loop gain
ADC	Analog to digital converter
ADRESH	Analog digital results HIGH
ADRESL	Analog digital results LOW
BOR	Brown-Out-Reset
C	Capacitance
C_c	Cable capacitance
C_f	Feedback capacitance
C_{inp}	Amplifier input capacitance
C_x	Unknown capacitor
CA	Charge amplifier
CCP	Command Control Processor
ECT	Electrical Capacitance Tomography
FEM	Finite Element Method
GND	Ground
LBP	Linear Back Projection algorithm
LFP	Linear Forward Projection algorithm
Op-amp	Operational amplifier
PWM	Pulse Width Modulation
SNR	Signal to noise ratio
UART	Universal Asynchronous Receiver/Transmitter

CHAPTER 1
INTRODUCTION

1.1 BACKGROUND

Process tomography is a process of measuring the signals by using specific types of sensor. The sensors are arranged around an object, such as pipeline, to examine the internal condition of the subject. The information on the nature of the subject is obtained by reconstructing the measurements from the sensors into a 2-D or 3-D image. The instrument components for process tomography consist of the hardware and software parts. The hardware part consists of the sensor for the signal and the data control of the process tomography. Meanwhile, the software part includes the program for reconstructs the signals and displays the results. Process tomography is already well known in oil and gas industry, as this technology brings a lot of benefits for the engineers to observe and examine the internal condition of process line or equipment.

The applications for process tomography in industrial sectors have been practically used especially in chemical, oil, pharmaceutical, food, biological, minerals, nuclear, environmental, water, healthcare, and materials processing industries. These applications can be categorized into five groups [1], which are:

- modeling in laboratory environment.
- process monitoring and control in an industrial environment.
- equipment design and optimization in a laboratory or industrial environment.
- characterization of individual components or products.
- remote sensing in manufacturing, quality control, environmental protection, or pollution control, on an industrial /waste disposal site.

In Table 1.1, the information represents some examples of process tomography methods which are applied in the industry field [1].

Table 1.1 Examples of process tomography techniques in process industries

Process application	Process tomography method
Microstructural characterization of components, particles, pastes, foams, filters (1-10 000 μm)*	Magnetic resonance imaging. Neutron tomography. X-ray microtomography. Optical tomography.
Liquid mixing and multiphase flow (0.01-0.5 m)*	Optical tomography. Resistive tomography. Capacitance tomography. Acoustic tomography.
Powder mixing, transport, and conveying (0.01 – 0.5 m)*	Capacitance tomography. Electrodynamics tomography.
Groundwater monitoring and soil remediation (0.01 – 0.5 m)*	Impedance tomography.
Atmospheric pollution monitoring (50 m – 10 km)*	Laser absorption imaging.
Oilfield reservoir exploration (50 m – 50 km)*	Acoustic velocity imaging. Acoustic diffraction tomography.

* typical operating length scales

There are various types of sensor system available that can be implemented in the process tomography. Normally, the sensor systems are based on measurements of electrical characteristics by using the radiation, acoustic, or electrical sensor. For example, the capacitive, conductivity, or inductive types of sensors are used to measure the electrical properties of a target subject in either small or large object in plant such as vessel. These sensors are suitable to apply in electrical properties measurement based on the fast responses from the sensors compare to the others. The applications for the

other types of sensor are summarized in Table 1.2 [1].

Table 1.2 Sensors for process tomography

Principle	Practical realization	Comments
Electromagnetic radiation	Optical	Fast, optical access required
	X-ray and γ-ray	Slow, radiation containment
	Positron emission	Labeled particle, not on-line
	Magnetic resonance	Fast, expensive for large vessel
Acoustic	Ultrasonic	Sonic speed limitation, complex to use

Electrical capacitance tomography (ECT) is one of the industrial process tomography systems, which measures the electrical properties of dielectric components in a specific object by using the capacitive sensors. The capacitive sensors provide fast responses for the measurement of permittivity distribution of the mixture in the specific object [1]. The sensors consist of a few sets of electrode plates, which are arranged around the specific object. The capacitances between the combination pairs of the electrodes are measured by the capacitance measurement circuit. Then, the measurements are obtained by the sensor electronics and sent to the image-reconstruction computer. The computer generates the tomography images of the permittivity distribution from the measurements by the sensors. The ECT system requires good sensors and sensor electronics design in order to provide low noise level, high stability, and accurate measurement sensitivity distributions during developing 2-D or 3-D images.

1.2 PROBLEM STATEMENT

Process tomography is a system of measuring the signals from a specific object and displaying the signals into an image. The tomography system which applies the electrical capacitance principle will be developed as to provide a platform in exploring the potential application of process tomography in oil and gas industry. In ECT system, it consists of two major parts, which are the hardware and software. The capacitive sensor, measurement circuit, and data acquisition circuit represent the hardware of ECT. Meanwhile, the software system of ECT is the image reconstruction system; the system for imaging the permittivity distribution in the target object. Various principles of electronics circuit, sensor, and image reconstruction are required to accomplish this project.

1.3 OBJECTIVES AND SCOPE OF STUDY

For this project, it is expected to meet the following objectives which are:

- to design a functional hardware system of ECT; including the capacitance sensor, measurement circuit, and data acquisition system.
- to gain the information of potential image reconstruction system which are suitable applied in ECT.

Therefore, this system is required to be developed by following the criteria of ECT for application in oil and gas industry. As a result, these scopes are required to understand deeply on ECT system:

- electrical capacitance principle as to develop the sensor and measurement circuit of ECT .
- electronics theory and circuit design for control and data acquisition system.
- image reconstruction system, in order to display the cross-section of the target object.

A Gantt chart for a guide in completing the project is attached in Appendix B.

CHAPTER 2
LITERATURE REVIEW AND THEORY

2.1 OVERALL DESIGN OF THE SYSTEM

An ECT system can be divided into three main parts; the capacitive sensor, the data acquisition system, and the image reconstruction system. The sensor is the most critical part which involves the quality of the information obtains from the process. This information must be accurate in order to have the best result for the image reconstruction of the internal condition around the sensors. In Figure 2.1, the overall design of the system is illustrated [5].

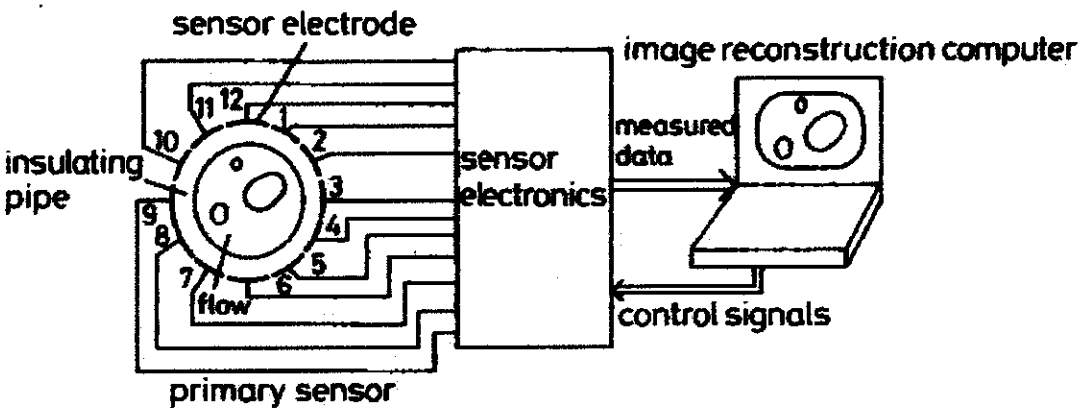


Figure 2.1 Electrical capacitance tomography system

2.2 CAPACITIVE SENSOR

Sensor is a device, which responds to a certain stimulus by an electrical signal. Stimulus is defined as the quantity or condition that the sensor sensed. There are two types of sensor; active and passive sensor. The active sensor depends on the external power for

its operation and then, the signal is modified by the sensor to produce an output signal. For a passive sensor, it is directly generates an electrical signal which has not to rely on any additional energy source.

A variety of sensing methods can be employed on measurements of transmission or electrical phenomena by using radiation, acoustic, or electrical sensors. The sensing system is chosen based on these factors [1]:

- The nature of the components (solid, liquid, gas, or the combination of these states).
- The information obtains from the process (steady-state, dynamic, resolution, and sensitivity required) and its purpose (laboratory investigation, optimization of equipment, process measurement, or control).
- Process environment (ambient operation condition, safety implication, and ease of maintenance).
- Size of the process equipment and length-scale of the process phenomena being investigated.

Capacitive sensors operate based on the mechanism of capacitance in between a number of two parallel plates. This type of sensor can be applied in a number of applications; such as in gauge displacement or position, and capacitance measurement for tomography system. The fundamental operating principles for the capacitive sensor rely on the distance between the capacitor plates and the dielectric material of the capacitor.

2.2.1 *Principle*

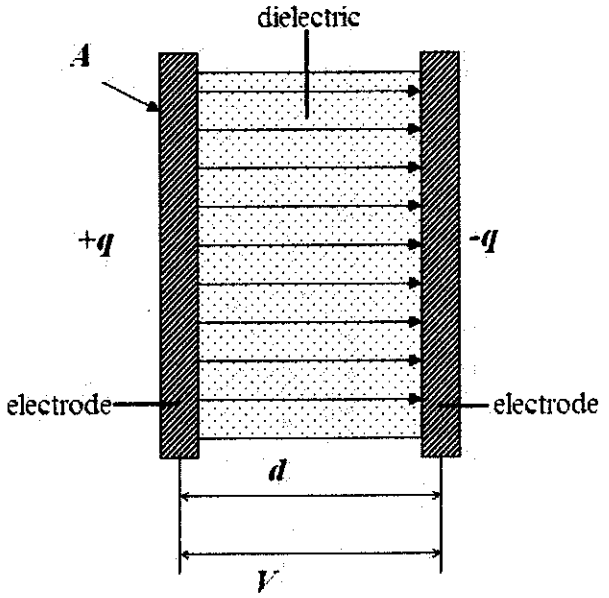


Figure 2.2 Electric charge and voltage define capacitance of a parallel-plate capacitor

A capacitor consists of a pair of plates, which can hold electric charges. The characteristics for the capacitor are the magnitude of charges (q) on both electrodes and the positive potential difference (V) between the electrodes. The ratio of charges to voltage is constant for each capacitor, and it is known as capacitance (C) of the capacitor. Capacitance is defined as the ability of an object or surface to store electrical charges. This ratio can be represented by

$$C = \frac{q}{V} \tag{1}$$

The capacitance is also known as a function of the distance between the two electrodes (d), the area of the plate (A), and the constant (ε_r) of the dielectric, which fill the space between the electrodes. The function for these variables is expressed as

$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} \tag{2}$$

where ε_0 = permittivity constant

$= 8.854 \times 10^{-12}$ F/m

SI unit for capacitance is 1 farad = 1 coulomb/volt which is represented by abbreviation F. In practical, submultiples of the farad are generally used such as

- 1 picofarad (pF) = 10^{-12} F
- 1 nanofarad (nF) = 10^{-9} F
- 1 microfarad (μF) = 10^{-6} F

2.2.2 Dielectric constant

The dielectric material between the electrodes of the capacitor is characterized by the dielectric constant. The dielectric constant is defined as the reduction in effective field because of the polarization of the dielectric. When the dielectric material is placed between the charged electrodes, the polarization of the medium will produce an electric field opposing the field of the charges on the plate. Therefore, the capacitance value will increase. When the value of the dielectric constant is high, the performance of the electrodes in the capacitor in holding the electric charges also will be better. Some examples of dielectric materials with their constant are shown in Appendix A. The dielectric material must be a good electric insulator as to minimize any DC leakage current through the capacitor.

2.2.3 Sensor characteristics

The electrodes of the capacitive sensors are arranged around the specific object and the capacitances between all the combination pairs of the electrodes are measured in order to build up the 2-D or 3-D images. Generally, for *N*-electrodes sensor, the numbers of independent measurements (*n*) are obtained by the combination formula of

$$n = \frac{N(N-1)}{2} \tag{3}$$

In Figure 2.3, it shows an example of twelve electrodes arrangement for the capacitive sensors. The capacitance between the electrodes; [1, 2], [1, 3], [1, 4], and until [11, 12] is measured sequentially with appropriate sensor electronics and the measured values are converted to voltage before they are linked to the image-reconstruction computer.

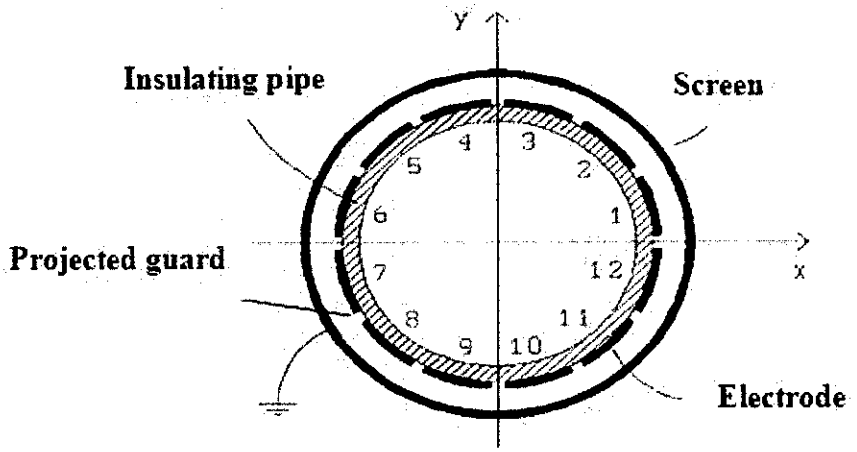


Figure 2.3 Cross-sectional structure of the capacitive sensors

The functions of components in the capacitive sensors are as followed:

- **screen** - to protect the sensor from interferences of external electromagnetic fields.
- **electrode** – to detect the capacitance between two electrodes.
- **projected guard** – to eliminate capacitances between back surfaces of adjacent electrodes and to reduce standing capacitance which insensitive to the dielectric distribution inside pipe liner.
- **insulating pipe** – to separate the material from the electrodes

A few parameters can be highlighted during designing the capacitive sensors, which are:

- the wall thickness of the insulating pipe.
- the gap between the screen and the electrodes.
- the gap between the projected guard with the electrodes.
- the permittivity of the insulating pipe liner.

2.3 DATA ACQUISITION SYSTEM

The basic system of data collection from the sensor is shown in Figure 2.4.

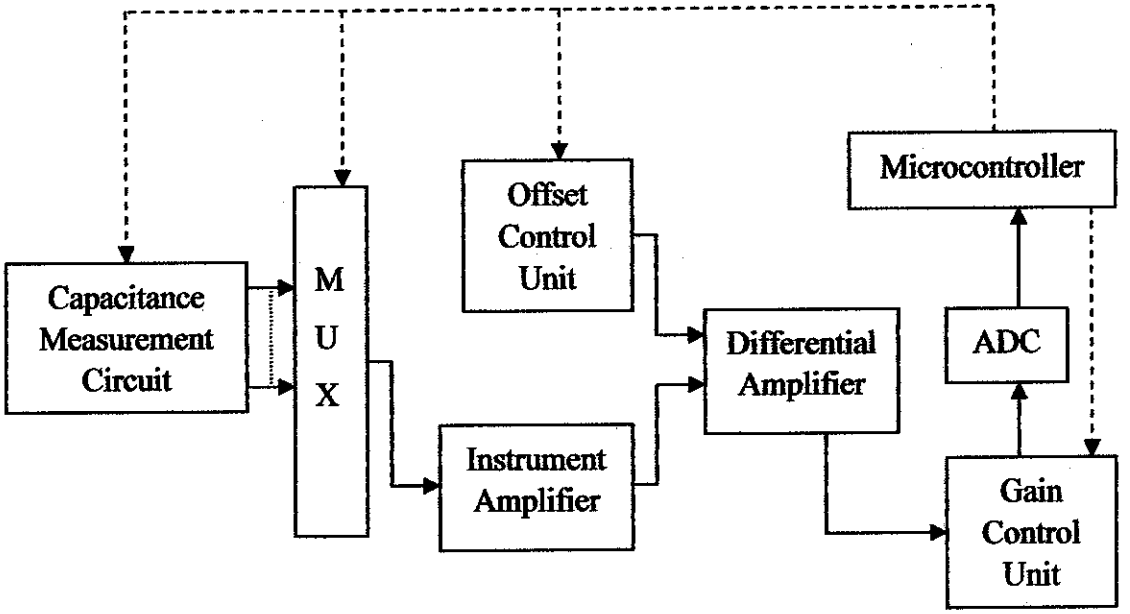


Figure 2.4 Data acquisition system

The major requirement for the capacitance measurement circuit is its sensitivity with the narrow area between the two selected electrodes. Stray-immune circuit satisfies this requirement because it only performs the capacitance measurement between the selected electrodes and insensitive to the stray capacitances either between the selected and the redundant electrodes or between the selected electrode and earth. The examples

of this type of circuit are ac ratio-arm bridges circuit with current detection and switched capacitor charge-transfer circuit. The characteristics for both circuits are shown in Table 2.1.

Table 2.1 Characteristics for the examples of stray-immune measurement circuit

Bridges circuit	Charge-transfer circuit
• Operate at frequency lower than a few hundred kHz • Low baseline drift • High signal to noise ratio • A parallel measurement channels with a modulator for each channel will create complexity	• Operate at frequency up to 2 MHz • Faster data-capture rate • Simple circuitry • To increase the speed, a parallel measurement channels could be used with low cost and no complexity

2.3.1 Amplifiers

Amplifier is composed with standard building blocks, such as operational amplifier (op-amp) and various discrete components (semiconductor, resistor, capacitor, and inductor). The functions of the amplifier are:

- to increase the signal amplitude (signal conditioning).
- to enhance the magnitude of the signal to noise ratio (SNR).
- as an impedance matching device.
- as an isolator between input and output.

For an op-amp with no feedback component, it is known as open-loop condition. In open-loop condition, the open loop gain (A_{OL}) is not a stable parameter. The gain changes with load resistance, temperature, and power supply fluctuation. However, an op-amp is rarely used without the feedback components because when A_{OL} is high, it may result in circuit instability, a strong temperature drift, and noise. The linearity, gain

stability, output impedance, and gain accuracy are improved by an amount of feedback and also depend on the characteristics of the feedback components.

2.3.2 Charge amplifier circuit

Charge amplifier (CA) circuit has extremely low bias current, which operates by producing charges that are proportional to the measurement variable and the charges can be converted into voltage. A basic circuit of a charge amplifier is shown in Figure 2.5.

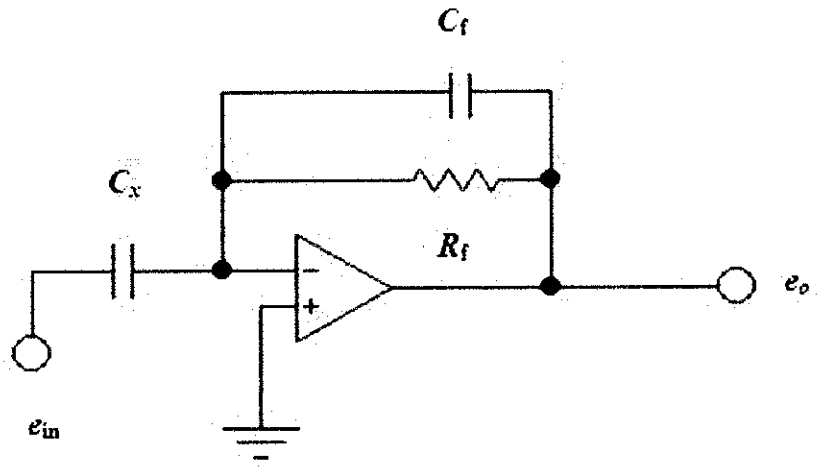


Figure 2.5 Charge amplifier circuit as charge-to-voltage converter

The charge amplifier circuit consists of a capacitor (C_f) that is connected into a feedback network of an op-amp. Its leakage resistance (R_f) which is in parallel with C_f, must be larger than the impedance of the capacitor at the lowest operating frequency [3]. Generally, the amplifier gives an output signal:

$$e_o = -\frac{C_x}{C_f} e_{in} \tag{4}$$

where; e_o = output voltage signal

e_{in} = input voltage signal

C_x = generated capacitance

C_f = feedback capacitance

CA is applied to provide a DC path for amplifier bias current. Without the R_f in the circuit, C_f will continue charging and then affect the output to drift into saturation [2].

The input stage of CA features a capacitive feedback connection, which balances the effect of the applied charge input signal. The feedback signal represents as the input charge, q_{in}. q_{in} is injected to the summing point (inverting input) of the amplifier. It is distributed to the cable capacitance (C_c), amplifier input capacitance (C_{inp}), and feedback capacitance (C_f). Therefore, the node equation of the input is:

$$q_{in} = -(q_c + q_{inp} + q_f) \tag{5}$$

By using the electrostatic equation q = VC and substitutes q_c, q_{inp}, q_f, and V_{inp} as the input voltage of the CA:

$$q_{in} = -[V_{inp}(C_c + C_{inp}) + V_f C_f] \tag{6}$$

Since the voltage difference between the inverting and the non-inverting input of a differential amplifier becomes zero under normal operating conditions, this can be assumed, as the V_{inp} equals to GND potential. With $V_{inp} = 0$, the equation might be simplified with:

$$q_{in} = -V_f C_f \tag{7}$$

Solving for the output voltage, V_{out} which also equals to the feedback voltage, V_f.

$$V_{out} = V_f = -\frac{q_{in}}{C_f} \tag{8}$$

The result shows that the output voltage of a CA depends only on the charges input and the feedback capacitance and it also the same with equation 4. Input and cable capacitances have no influence on the output signal.

2.3.3 Analog to Digital Converter

Analog to digital converter (ADC) is applied as to digitize the final signal from the gain control unit. PIC16F877 as shown in Figure 2.6 is going to be applied at the end of data acquisition system before the output signal is sent to the computer. PIC16F877 is a high-performance FLASH microcontroller that provides the high design flexibility. PIC16F877 features an integrated 8-channel 10-bit ADC. Peripherals include two 8-bit timers, one 16-bit timer, Watchdog timer, Brown-Out-Reset (BOR), In-Circuit-Serial Programming™, RS-485 type Universal Asynchronous Receiver/Transmitter (UART) for multi-drop data acquisition applications, and 12C™ or SPI™ communications capability for peripheral expansion. Precision timing interfaces are accommodated through two Command Control Processor (CCP) modules and two Pulse Width Modulation (PWM) modules [6].

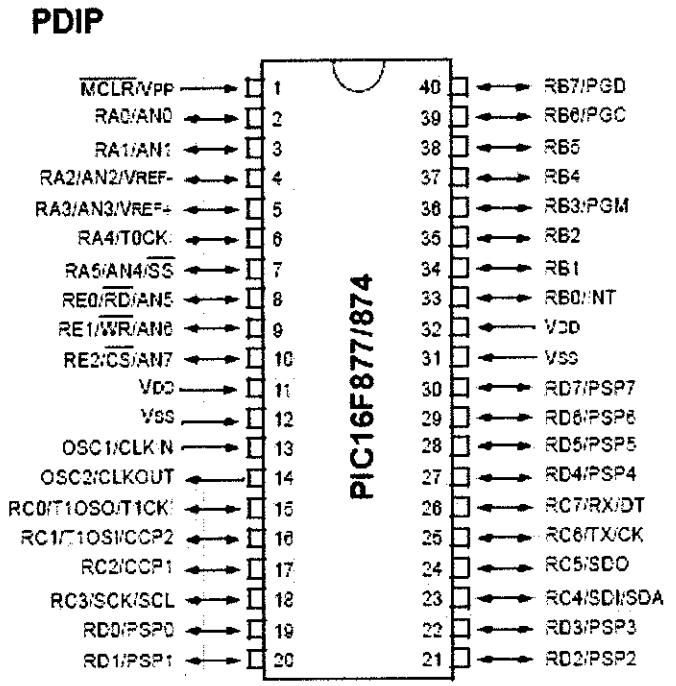


Figure 2.6 Microcontroller 16F877

2.4 IMAGE RECONSTRUCTION SYSTEM

The data presented to the computer are as an array of numbers which are related to the capacitance measurements taken between two electrodes. Linear Back Projection (LBP) Algorithm has been considered as one of the method to develop the image. From LBP algorithm, the normalized capacitance measurements are weighted by a predetermined sensitivity distribution function and back projected on to the object cross-section.

CHAPTER 3
METHODOLOGY

This project will be implemented in duration of 2 semesters. To be accomplished, this project will need several methods. Therefore, the project will be implemented by stages as listed below:

- First semester: Literature review / research / data gathering / circuit design / testing / analysis
- Second semester: circuit design and improvement / computer-device communication development / testing / analysis

3.1 LITERATURE REVIEW AND RESEARCH

Literature review and research will be done by obtaining the information through books, internet, and journals. These stages provide the important and useful knowledge for next step; the design stage.

3.2 CIRCUIT DESIGN

The design of capacitance measurement circuit is based on the switching period of charges and discharges the unknown capacitor (C_x) and also how to measure the charges from the capacitor. This design is based on the charge-transfer circuit design which has more advantages compare to the bridges circuit as mentioned in Table 2.1. The capacitance measurement circuit applies CA to convert the charges from into the voltage signal. This CA is designed refers to the output equation of the amplifier circuit.

There are two main components for the CA; R_f and C_f. The presence of R_f limits the lower bandwidth of the CA to a frequency, f_L given by the equation:

$$f_L = \frac{1}{2\pi C_f R_f} \tag{9}$$

A high value of R_f is required if the output is to reproduce slow changes in the measurement variable [2]. Therefore, R_f is set to be

$$R_f \approx 100\, Z_{C_f} \tag{10}$$

$$f_o \approx \frac{100}{2\pi C_f R_f} \tag{11}$$

The operating frequency, f_o is applied with a higher value than the f_L to obtain a stable DC output voltage. This condition requires a high speed of op-amp which its transient frequency, f_t is

$$f_t \approx 100\, f_o \tag{12}$$

The switching circuit of the switched capacitor charge transfer circuit is designed based on the charging and discharging stages of C_x. These stages are related to the RC time constant, τ which is the time for a capacitor to charge and discharge an amount of capacitance. This time constant relates with the time require for a capacitor to charge up to 63.2% of the applied voltage or discharge down to 63.2%. Usually the value of τ is equal to the value RC. For the capacitance measurement circuit, τ will be influenced by the R_fC_f in the CA circuit. A capacitor normally takes 5τ to charge and another 5τ to discharge. In the capacitance measurement circuit, four switches will be applied, which are connected to the source and detecting electrodes. Two switches are ON during charging period of C_x and another two are ON during discharging it.

3.3 EXPERIMENTAL

The design of capacitance measurement circuit is tested by using the values of the resistors and capacitors for the feedback components, which are obtained from the calculation, with a number of known capacitance values as the C_x. The output signals of the CA are observed. The observations from the experiment are analyzed to ensure the calculation values for the output voltage are the same as the output measured. Function generator, DC power supply, multimeter, high-speed op-amps, CMOS quad bilateral switches, resistors, multiplexer, capacitors, logic gates, and J K flip flop are used during the experiment.

3.4 ANALYSIS

The results from the tested circuit are analyzed by comparing the calculated values with the experimental values to prove that the circuit is able to operate as a capacitance measurement circuit. If the comparison raises a lot of differences, the circuit design is altered by using new values of components obtain from the calculation. The analysis is continued until the best design of capacitance measurement circuit is achieved.

3.5 COMPUTER-DEVICE COMMUNICATION DEVELOPMENT

During the hardware development, 2 major types of programming are used; C language for the microcontroller and the interface programming. The microcontroller is programmed due to convert the analog signal from the data acquisition system to the digital signal before the signal is transmitted to the computer. For interface programming, Visual Basic 6.0 programming is applied as to develop the communication between the hardware and the computer.

3.6 COMISSIONING AND VERIFICATION

After completing those procedures, the next step is commissioning. During this level, the verification and device 'test run' are carried out. This procedure will ensure that the device can work properly and withstand various conditions. The steps involve for this procedure are component assembly, test run, and trouble shoot.

CHAPTER 4
PROJECT WORK

4.1 HARDWARE

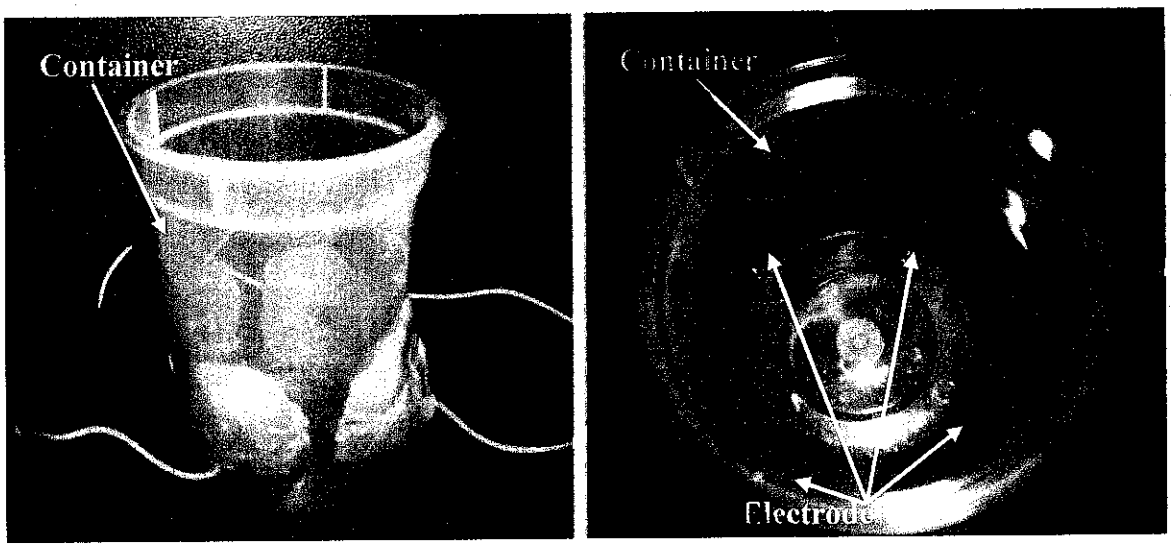
This project requires on designing the hardware system for the ECT. It consists of the capacitance electrodes, capacitance measurement circuit, multiplexer, instrument amplifiers, differential amplifiers, charge and discharge control circuit, offset control unit, gain control unit, control logic, and PIC microcontroller.

4.1.1 Sensor system

Capacitance sensors consist of a pair of selected electrodes which is controlled by the switching circuit via two pairs of CMOS switches. The capacitance between the selected electrodes is measured by the capacitance measurement circuit. For a complete sensor system, an even number of electrodes are arranged peripherally of an object.

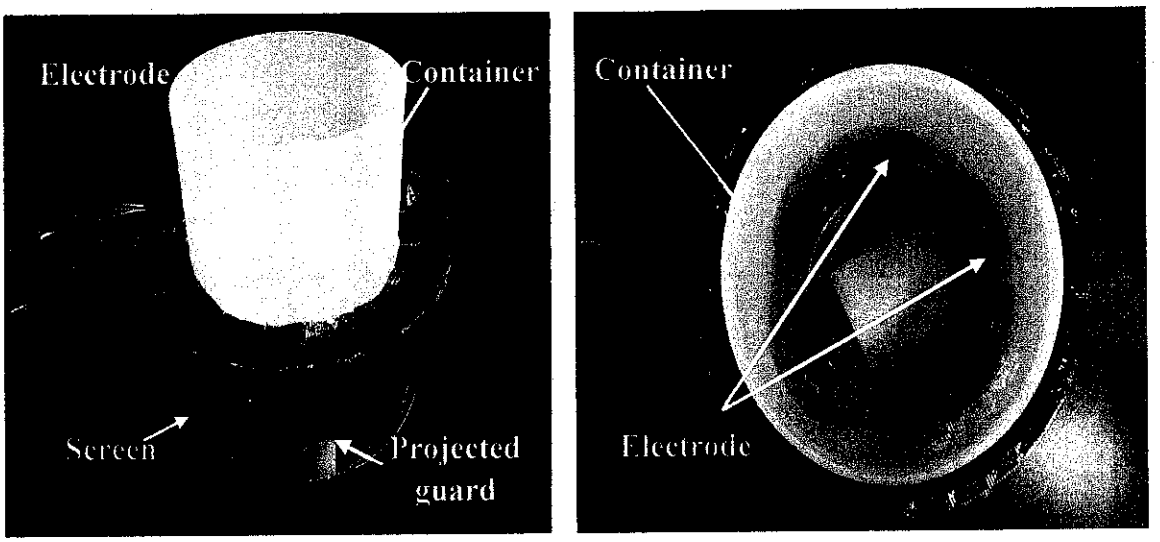
Firstly, the known values of capacitor (1-10pF) are used which represent as a pair of electrode in the sensor system. These capacitors are connected one by one to the capacitance measurement circuit as to observe the circuits' performance when the values of the capacitor are varied. After the performance is analyzed, a prototype of 4 electrodes sensor system (Figure 4.1) is constructed in order to repeat the same analysis with known capacitors. The capacitance for a pair of electrode depends on the distance between those electrodes. The capacitance between adjacent electrodes are higher than the opposite electrodes but the capacitance of electrodes 1 and 2; and 1 and 4 might not be the same due to the stray capacitance from the measurement circuit and also the

interference from the external electromagnetic field from surrounding. To reduce the interference of electromagnetic field, a prototype for 8 electrodes (Figure 4.2) is designed with an earthed screen around the electrodes. The electrodes are arranged alternately with projected guard to ensure that these electrodes will not touch each other and to reduce any stray capacitance contribute by the adjacent electrodes.



(a) (b)

Figure 4.1 Sensor system with 4 electrodes: (a) opposite view, (b) top view



(a) (b)

Figure 4.2 Sensor system with 8 electrodes: (a) opposite view, (b) top view

4.1.2 Capacitance measurement circuit

The measurement circuit is based on the charge transfer circuit and charge amplifier circuit. The charge-transfer circuit provides a fast data capture rate and it also simpler compares to bridge circuit. The performances of charge-transfer circuit which are represented by the CMOS switches in the circuit are as follows:

- The operation will be repeated at an operating frequency, f_o of the circuit. This frequency also known as the sampling frequency of the circuit.
- The sampling frequency is chosen so that:

$$f_s > 2f_x \tag{13}$$

where f_x is the frequency of C_x.

- The charge amplifier circuit is designed to have a low-pass bandwidth which satisfies:

$$f_o < f_s - f_x \tag{14}$$

- C_{in} is the capacitor uses to ensure the virtual earth potentials at the charge amplifier circuit remain stable during the high-speed charge and discharge stages.
- By choosing large integration time constant, $T_f = R_f C_f$ and large value of C_{in}, the charge measurement circuit will produce a DC output voltage proportional to the C_x.

- The output voltage of the charge measurement circuit is given by:

$$V_o = f_s V_c R_f C_x \tag{15}$$

Charge amplifier is a part of the charged-transfer circuit, which reacts as the converter to convert the generated charges from the capacitive sensors to voltage signal which operates at certain frequency. The switching circuit is connected to the CA circuit as to control the charging and discharging stages of the C_x.

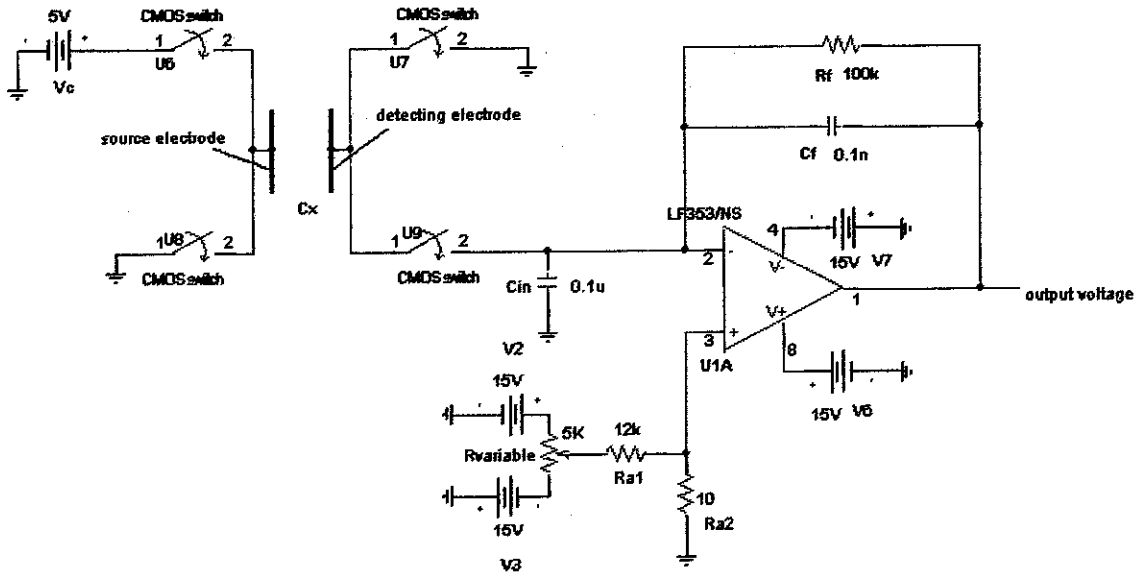


Figure 4.3 Capacitance measurement circuit

During designing the circuit, a few points are highlighted as to obtain the exactly values for the components for operating it in high speed.

- The CA circuit is conducted at frequency 10^6 for higher sensitivity.
- The value of C_f must be very small so it can measure C_x in small range.
- Its R_f which is in parallel with C_f, must be larger than the impedance of the C_f.

Thevenin theorem is used to eliminate the offset voltage at the noninverting input of the op-amp:

Given $V_{ios} = 10\text{mV}$

$V = |V_{cc}| = |V_{ee}| = 12\text{V}$

$$R_{pmax} = \frac{R_p}{2} \| \frac{R_p}{2} = \frac{R_p}{4}$$

$$\frac{V}{V_{ios}} = \frac{R_{a1}}{R_{a2}} = \frac{12}{10\text{m}} = 1.2\text{k}$$

$R_{a2} < 100\Omega$

Therefore, $R_{a2} = 10\Omega$, $R_{a1} = 12\text{k}\Omega$

$$R_{pmax} = \frac{R_{a1}}{10} = 1.2k\Omega$$

$R_p = 4 \text{ x } R_{pmax} = 4.8\text{k}\Omega$

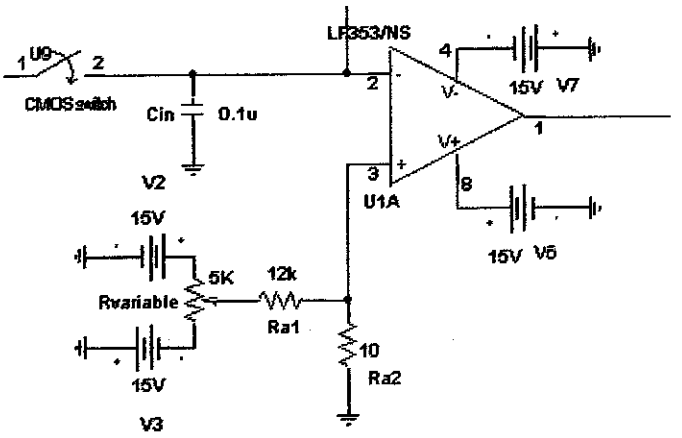


Figure 4.4 Compensation network: eliminate the offset voltage

4.1.3 Multiplexer

For this design, multiplexer is used to select only one measurement output from the measurement circuits at a time before the signal is digitized by the ADC. After all measurements are completely convert to digital signal, then all the data will be sent to the computer. IC CD4051B is applied to the circuit as the multiplexer.

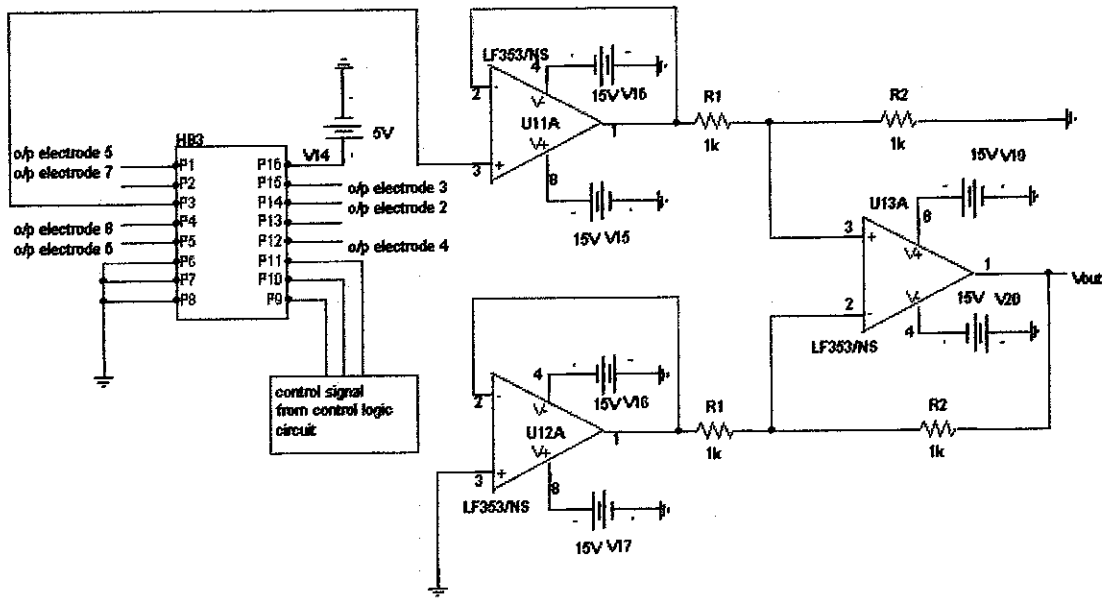


Figure 4.5 Multiplexer connected to the instrument and differential amplifier

4.1.4 Instrumentation amplifier and differential amplifier

An instrumentation amplifier is a type of op-amp that has been specifically designed to have characteristics suitable for use in measurement and test equipment. This op-amp is applied when accuracy and stability of the circuit are required. Along in the instrument amplifier is differential amplifier. The differential amplifier amplifies the difference between two input signals (-) and (+). This amplifier is also referred to as a differential-input single-ended output amplifier. It is a precision voltage difference amplifier, and forms the central basis of instrumentation amplifier circuits. This differential

amplification also been applied as the first stage of op-amps. The output equation for the circuit in Figure 4.2 is as follows:

$$V_{out} = (V_2 - V_1)\frac{R_2}{R_1} \tag{16}$$

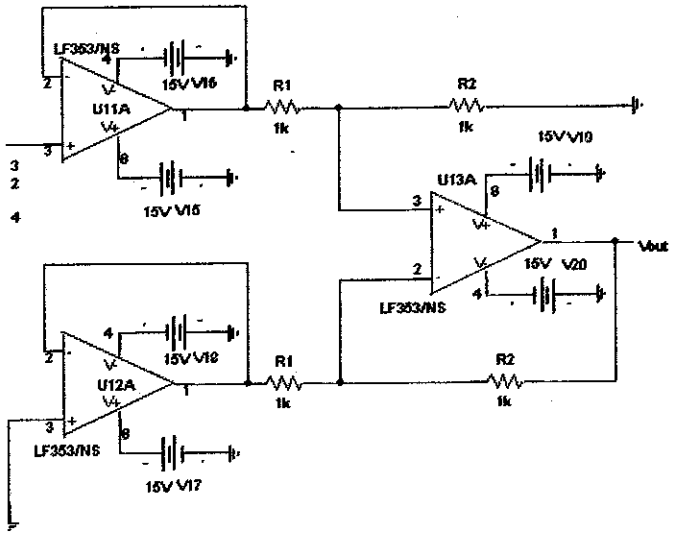


Figure 4.6 Differential amplifier with buffer amplifiers

4.1.5 Offset and gain control units

Offset control unit is established as to correct the drift by subtracting the baseline from the values measured afterwards. The offset value which is obtained during the calibration of the mesurement circuit is subtracted from each measurement value after the check. The calibration procedure is performed before the measurement and imaging process. The procedure is described from block diagram in Figure 4.7.

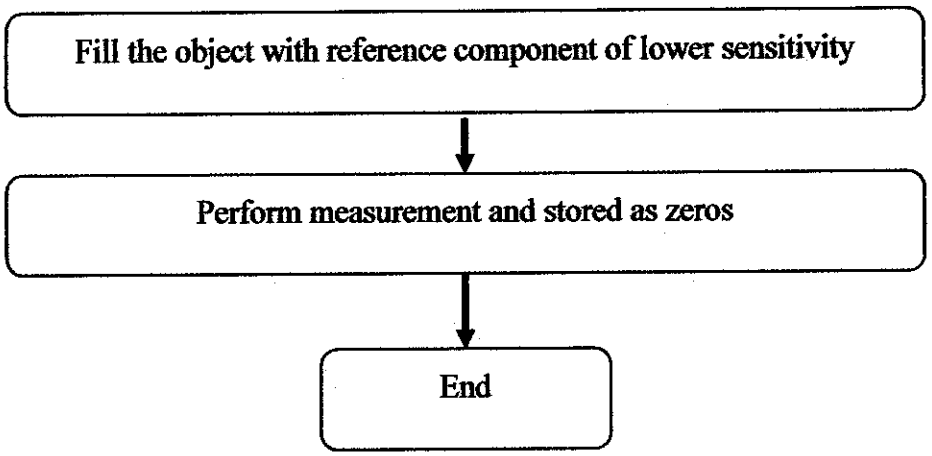


Figure 4.7 Calibration procedure

Gain control unit functions as to amplify the output signal with the selectable gains. Therefore, the output signal will deal with the large measurement range [7].

4.1.6 Analog to digital converter

PIC16F877 microcontroller circuit at the end of data acquisition circuit is able to convert the analog signal of the measurement to the digital signal before the output is trnasmitted to the computer for image reconstruction. The microcontroller needs to be programmed by using C language. The programmed codes are downloaded via MPLab software by using WARP13 external device.

PIC16F877 works on a 10-bit digital number. The 10-bit A/D data is loaded onto the register pair ADRESH:ADRESL which is a 16-it wide register pair. The A/D module has a high reference voltage of 5V and a low reference voltage of 0V. Therefore, the analog input must be varied between the ranges of 0 to 5V. An example to convert the corresponding voltage to a hexadecimal number is as shown below:

Since the maximum voltage allowed is 5V, the corresponding 10-bit binary number will be:

$11\ 1111\ 1111_2$ is equal to 1024_{10}.

This is the base ration for the next voltage value.

Eg:

Input voltage = 3.75 V

$$3.75\text{V}x\frac{1024_{10}}{5\text{V}} = 768_{10}$$

Therefore, 768_{10} is equal to $11\ 0000\ 0000_2$.

This microcontroller also uses as the part of serial communication to the computer. The programming is designed to select one by one the output signal to be transfer to the computer as in serial output.

4.1.7 Control logic circuit

The switching circuit and multiplexer is controlled via control logic by using J-K flip-flop integrated circuit (IC) and logic gates. The gates IC consist of AND and OR gate. The state transition diagram is applied to obtain how many states are required for the counter flip-flops change with each applied clock pulse. State transition diagram is used as to analyze, and design counters and other sequential circuits. The state transition diagram is illustrated in Figure 4.8. From the figure, each circle represents one possible state as indicates by the binary number. The arrows connecting the circles show one state changes to another as a clock pulse applied.

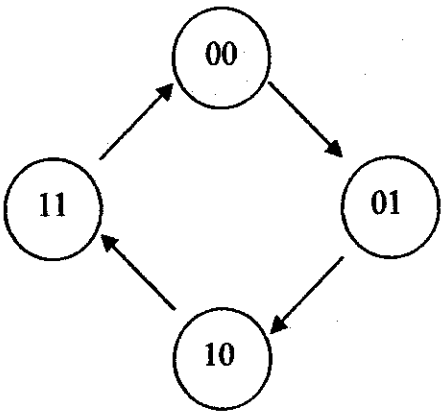


Figure 4.8 State transition diagram

The sequence circuit of the state transition diagram is developed by using the sequential circuit design method. This method involves the design of synchronous counter and logic circuit as to decode the various states of the counter to supply the logic level to each J and K input. The inputs to the decoder circuits will come from the outputs of the flip-flops. The Excitation Table (Table 4.1) is used to determine the J and K levels require producing any transition at the output.

Table 4.1 J-K flip-flop Excitation Table

Transition at output	PRESENT state Q(N)	NEXT state Q(N+1)	J	K
0 → 0	0	0	0	x
0 → 1	0	1	1	x
1 → 0	1	0	x	1
1 → 1	1	1	x	0

The signal for the charge and discharge switches, control signal for the multiplexer, and inhibit signal for the multiplexer are obtained from the output of the J-K flip-flop. The output signal of J-K flip-flop will be either connected directly or connected to logic gates first as to obtain the specific control signal for control input of both switches and multiplexer. The Karnaugh map (K map) is applied during logic control design as to simplify the logic equation and to convert the truth table to its corresponding logic

circuit in a simple process.

4.1.8 Communication circuit between hardware and computer

PIC16F877 microcontroller circuit is constructed to establish the communication between the hardware of ECT system to the workstation (computer). This microcontroller is programmed to read the output measurement from the data acquisition system. MAX232 integrated circuit also included with the connection of PIC6F84A as to control the communication of the serial communication. It either can be as a driver or receiver to the serial port of the computer. MAX232 also helps protect the processor from possible damage by static that may come from people handling the serial port connectors. Therefore, it is needed to establish the communication between the device, processor, and RS232 serial port.

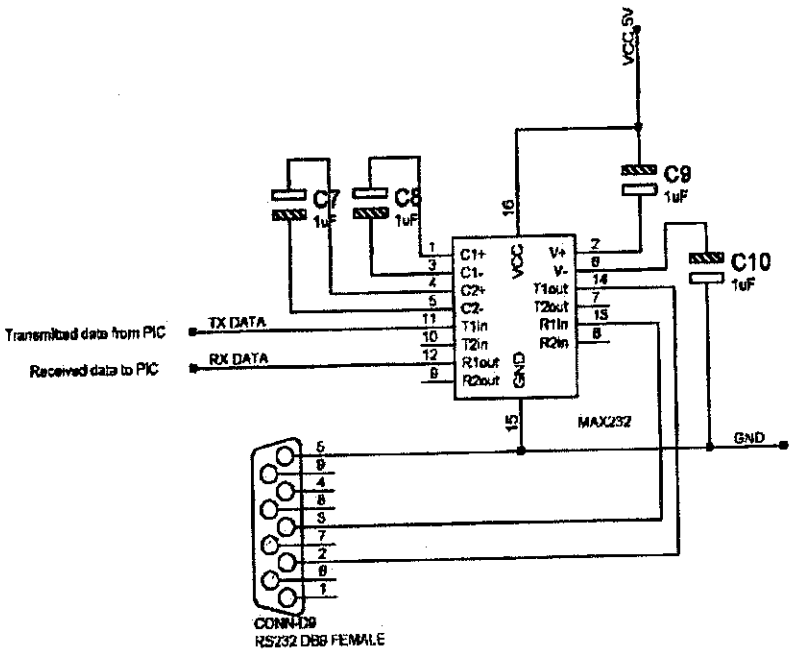


Figure 4.9 The connection between RS232 serial ports with MAX232

4.2 SOFTWARE

Mainly the software system is the visualization of the measured signals from the hardware system which are stored into the computer. For the image reconstruction, Linear Back Projection (LBP) Algorithm, Linear Forward Projection (LFP), and Finite Element Method (FEM) can be employed for the real time visualization.

4.2.1 Image reconstruction programming

FEM is based on the electrostatic field theory which investigates the complex capacitor sensor configuration. Then, it will model the pattern by dividing the cross section into P quadrilateral elements corresponds to the Q nodes. The resultant nodal potential will be used to determine the capacitance between electrode pair i-j by performing:

$$Ci = -\frac{1}{V}\int_{Li}\varepsilon(x,y)\nabla\phi(x,y)\vec{dl} \tag{17}$$

V = voltage at source electrode

Li = curve encompassing the detecting electrodes

Φ(x, y) = depends upon the dielectric distribution

FEM will represent the pipe cross-section as an array of sensitivity values:

- Each value will correspond to the magnitude of capacitance change at the pixel (p).
- $S_{i,j}(p)$ is the precalculated of the sensitivity matrix
- $G(p)$ is the grey level of the image
- $\lambda_{i,j}$ is the normalized capacitance measurement

From equation 18, the first image is reconstructed from the value of the measured capacitance and the sensitivity matrix.

$$G^{(0)} = SC \tag{18}$$

The sensitivity matrix is performed by:

$$S_{i,j}(p) = \frac{C_{i,j}(p) - C_{i,j}(\text{empty pipe})}{C_{i,j}(\text{full pipe}) - C_{i,j}(\text{empty pipe})} \tag{19}$$

Next image is obtained from the iterative process. The capacitance is estimated from current image $G^{(k)}$ and sensitivity matrix ,S by applying the LFP algorithm.

$$G^{(k+1)} = G^{(k)} + \alpha S(C - SG^{(k)}) \tag{20}$$

α = step length

CHAPTER 5
RESULT AND DISCUSSION

During the project commissioning, some experiments are carried out to obtain the results with high efficiency and reliability. According to the requirement, the experiment is performed by using the known values of C_x in order to observe the linearity of the output. As long as the output voltage is proportional to C_x, the result is acceptable. The circuit for this experiment is shown in Figure 5.1.

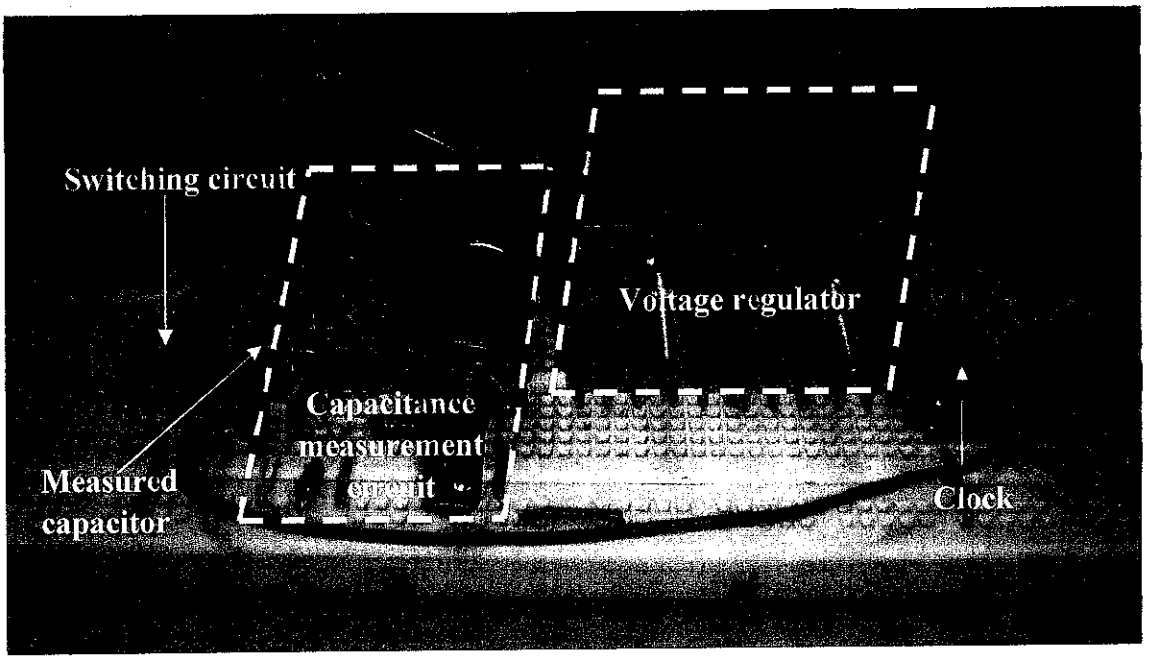


Figure 5.1 Test circuit for capacitance measurement

The conditions for each experiment are listed in Table 5.1. The output graph for each result is illustrated in Figure 5.2. The conditions for each experiment are based on these settings:

Table 5.1 Conditions for each experiment

Condition	C_f(pF)	R_f(MΩ)	f_s(kHz)
A	0.5	50	16
B	0.5	50	32
C	0.5	50	32
D	0.5	50	64
E	0.5	50	64
F	0.5	50	128
G	0.5	50	250
H	0.5	50	500
I	0.5	10	500
J	0.5	50	1000
K	0.5	10	1000

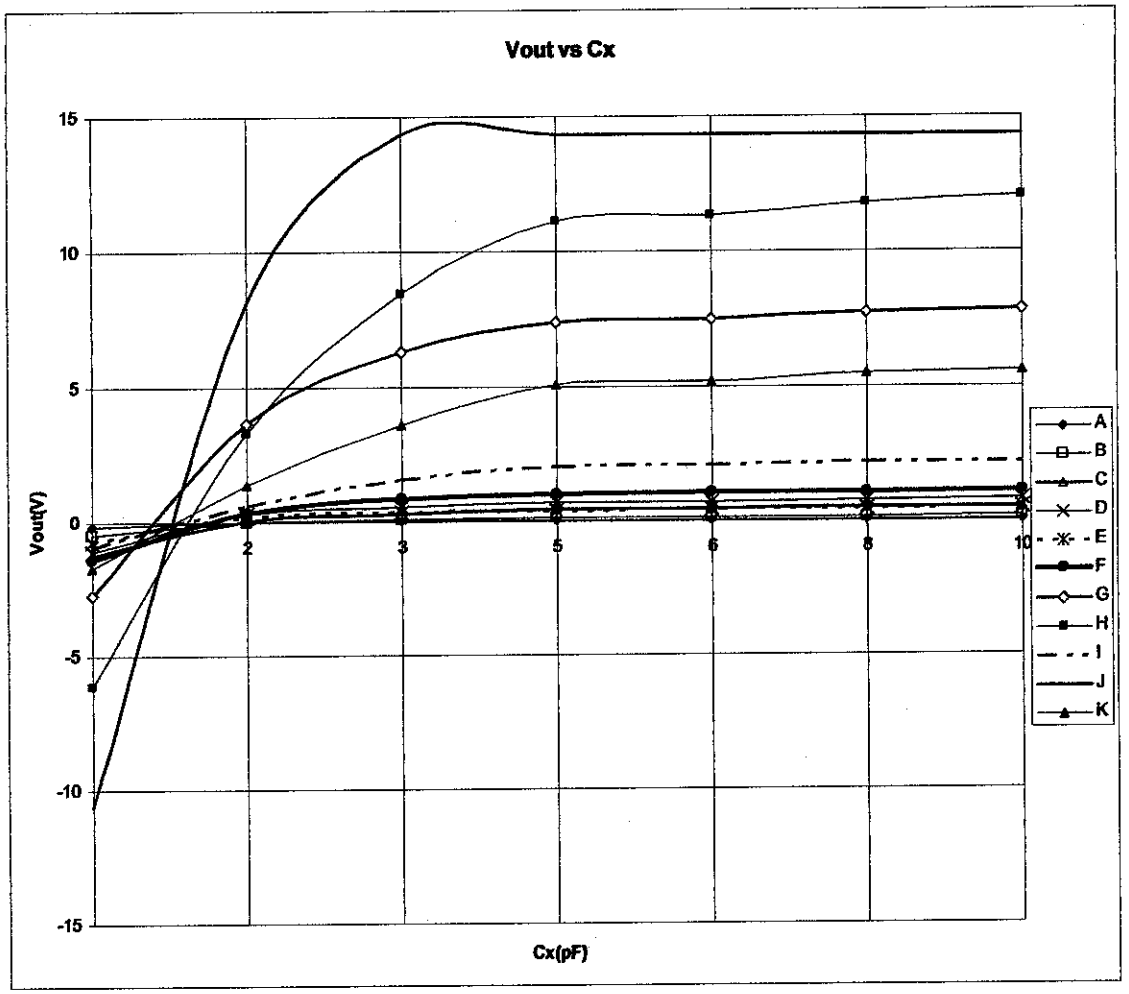


Figure 5.2 The linear response of output voltage vs known capacitor, C_x

In this experiment, the outputs are not stable when f_s are higher than 64 kHz. For capacitance measurement circuit, it is required to operate in high frequency as to increase the sensitivity of the circuit with the output measurement. From those results, the circuit is reconstructed to increase the accuracy of the output in high operating frequency. The values for new circuit design of capacitance measurement circuit are listed in Table 5.2. The graph of output voltage vs C_x is represented in Figure 5.3.

Table 5.2 Results of output voltage (mV) for C_f = 0.1nF, and f_s = 1MHz

C_x (pF) / R_f (Ω)	1	2	3	5	6	8	10
100k	34.8	510.6	885.7	2030	2310	3550	4300
51k	22.9	266.8	458.2	1040	1170	1810	2180
43k	20.2	235.2	404	915	1020	1560	1920
36k	11.4	185.6	322.7	740	846	1290	1560
24k	15.5	132.2	223.5	501.9	562.7	865.7	1050
12k	12.7	71.5	117.4	257.2	286.7	440.4	530.9
1k	9.57	14.5	18.3	29.9	32.3	45.2	52.7

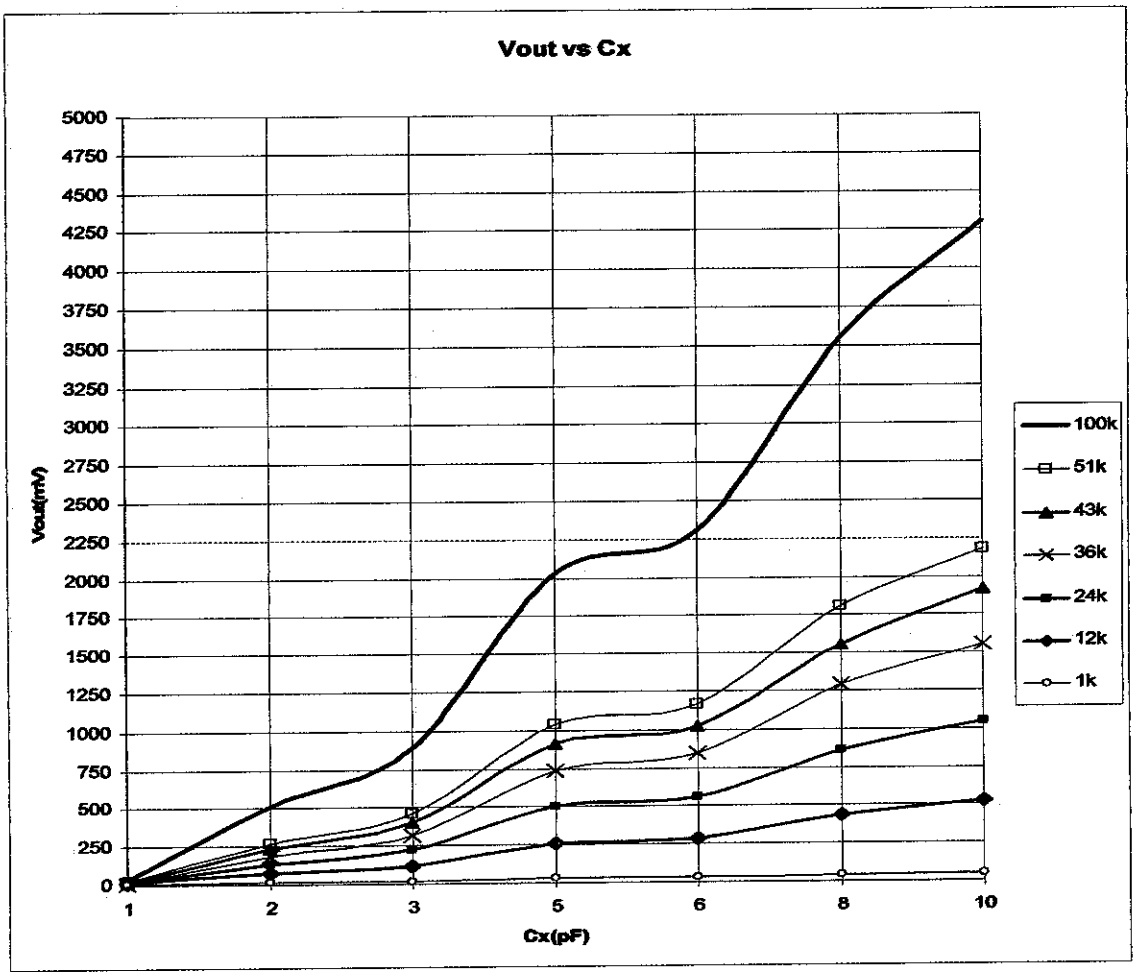


Figure 5.3 Positive linear response for output voltage vs known capacitor, C_x

Based on Table 5.2 and Figure 5.3, the results show that when the value of R_f is increased, the output voltage will give more difference between the reading when the value of C_x is changed. Therefore, if there is any capacitance change in the target object, the circuit will capable to give a big difference in the output voltage.

This capacitance measurement circuit on the breadboard is tested with 4 electrodes system and the output voltage is measured manually using digital multimeter. The output voltage is quite small compare when the circuit is tested with known capacitor. This condition happens due to the effect of stray capacitance from the wiring and the circuit itself. Therefore, the sensor system is tested with printed circuit board (PCB) by using circuit as in Figure 5.4 and the output voltages are compared with the previous measurement. The result is showed in Figure 5.5.

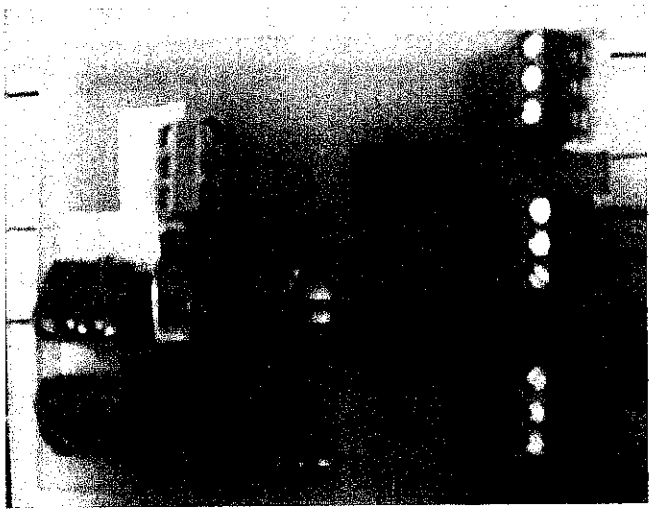


Figure 5.4 Capacitance measurement circuit on the PCB

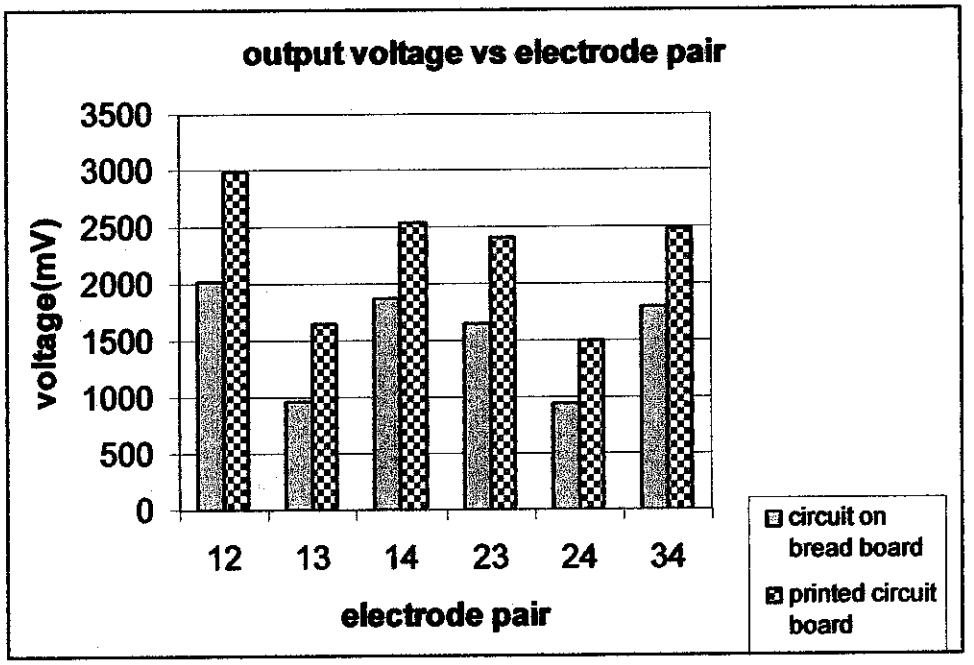


Figure 5.5 Comparison of output voltages from circuit on the breadboard and PCB

Based on Figure 5.5, the effect of stray capacitance from the wiring can be reduced by designing the circuit on a PCB. This method will reduce the stray capacitance because of the large earth plane on the printed board. The efficiency of the measurement circuit also increases due to the high sensitivity of the circuit to the small changes in the measured capacitance.

The capacitance measurement circuits are tested with the 8 electrodes capacitive sensor for observing the circuits' sensitivity with the measured capacitance. The sampling test is conducted twice with electrode 1 as the source electrode and the other electrodes as the detecting electrodes. Therefore, the will be 7 measurements obtained during the sampling test. The output voltages for the sampling test are illustrated by the bar graph in the Figure 5.6.

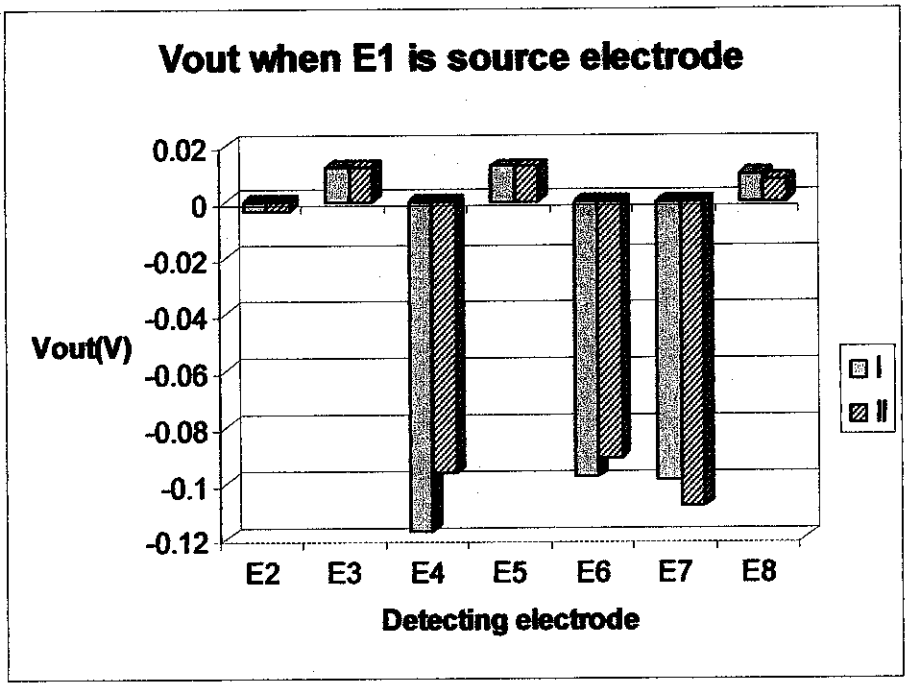


Figure 5.6 Output voltage for 8 electrodes capacitive sensor

From Figure 5.6, it shows that the output voltage for both sampling times are quite similar, means that the time delay that contributes from the components are quite small and do not bring big effect for sampling the output voltage. The negative values of the output voltage represent that the measurement is conducted at very low sampling frequency so it requires conducting the sampling at higher frequency as to increase the sensitivity of the measurement circuit.

The control logic circuit is designed based on the sequential circuit design method. The truth table of controlling the circuit for sampling test is attached in Appendix C. This design process involves the transition diagram from state 0000 to state 1111. After that, the Excitation Table (Table 4.1) is referred to build the truth table for the J-K flip flops transition level. From this truth table, the K map method is applied as to simplify the corresponding logic circuit. As the result, the control signal for inputs of flip-flops, multiplexer control, and switches are as follow:

- J-K flip-flops
  - $J_{Q0} = 1, K_{Q0} = 1$
  - $J_{Q1} = Z, K_{Q1} = Z$

- $J_{Q2} = YZ$, $K_{Q2} = YZ$
- $J_{Q3} = XYZ$, $K_{Q3} = XYZ$

- Multiplexer
  - $A = Y$
  - $B = \overline{W}X + W\overline{X}$
  - $C = W$
- CMOS switches (S_{xS} = source switch, S_{xG} = ground switch, S_{xM} = measurement switch)
  - Electrode 1
    - $S_{1S} = \overline{Z}$
    - $S_{1G} = Z$
  - Electrode 2, 3, 4, 5, 6, and 7
    - $S_{xS} = 0$
    - $S_{xG} = \overline{Z}$
    - $S_{xM} = Z$
  - Electrode 8
    - $S_{8G} = \overline{Z}$
    - $S_{8M} = Z$

To obtain the best design of hardware system for the 8 electrodes sensor system, the measurements circuit is tested with only two complete cycles of measurement with electrode 1 is the source electrode. The sampling time for the measurement is important because of the measurement from each detecting electrode happens in 0.5us. Therefore, the sampling time for the output must be faster enough. Latching method is applied as to hold first the output values in digital form before it is transmitted to the computer. The hardware system for the ECT is referred in Figure 5.7.

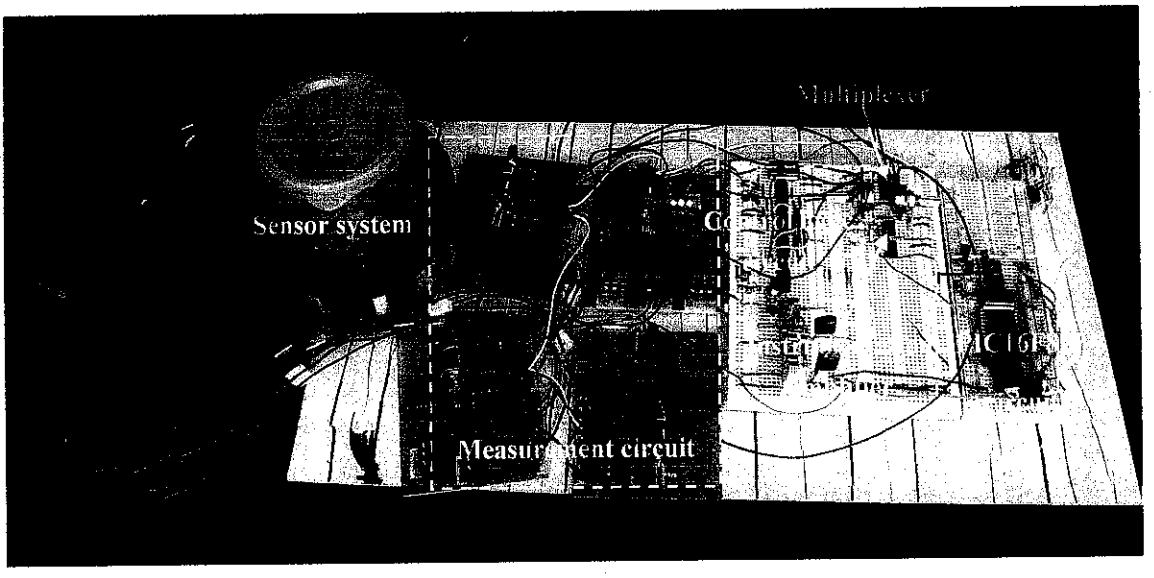


Figure 5.7 Hardware system of ECT

CHAPTER 6
CONCLUSION AND RECOMMENDATION

6.1 CONCLUSION

As the conclusion, the project brings the opportunity to learn and develop the capacitive sensors system base on from the literature review and research which have been done before. This hardware part exposes the student in circuit design and gain experiences in troubleshoot the circuit. From the experiment of circuit measurement circuit, the charge-transfer circuit can be used as the one of the main circuit to measure the capacitance in term of voltage. High operating frequency of the op-amp and ceramic capacitors are used to obtain a good result from the experiment. The components also need to be examined first before starts the experiment to ensure all of them are working when they are connected to the power supply.

The limitation in designing the circuit is to find the op-amps which capable to operate with high frequency. This first design of capacitance measurement circuit only capable to measure the C_x from 1nF to 0.1nF only. This condition happens because of the operating frequency is bigger than the transient frequency of the op-amp. The operating frequency of this circuit must be 100 times less than the transient frequency. Due to this limitation, op-amp LF353 and with new values for other components are used for the measurement circuit. By using this design, the circuit is capable to measure from 1pF to 10pF. To increase the sensitivity of the circuit, it is designed on the PCB with large earth plane.

The sampling time to transmit the measured output voltage to the computer also important due to obtain the right values during the sampling. When the transmission involves a number of components before the data is sent to the computer, it will contribute some delays which will interrupt the right time for the data to be transmitted. To overcome this problem, latching method is applied to the data before it is transmitted in order to hold first the data and avoid the controller from loss it.

6.2 RECOMMENDATION

From this project, the whole circuit of the hardware system must be designed on the PCB in order to reduce the effect of the stray capacitance from the wiring. This way will improve the sensitivity of the circuit with the small changes in the measured capacitance. The prototype of the sensor system can be upgraded by increasing the size of electrodes and reduce the distance between the adjacent electrodes. The screen and projected guards also can be improved by using a harder plastic as to reduce more on the interference of the electromagnetic field from the surrounding. The sampling time for the output signal can be increased by applying higher frequency in the control circuit. The status of the electrodes can be controlled by using the PIC as to increase the effectiveness of the control logic circuit. The control logic circuit can be implemented by using only the PIC via programming the state machine of control logic circuit into the PIC. This will make the data acquisition circuit becomes less complexity.

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APPENDICES

APPENDIX A

DIELECTRIC MATERIAL AND DIELECTRIC CONSTANT

Examples of dielectric material with its constant

Dielectric material	Dielectric constant, ε_r	Dielectric material	Dielectric constant, ε_r
Air	1	Air dry (68^0F)	1.000536
Water	4-88	Water (32^0F)	88
Water (68^0F)	80.4	Water (80^0F)	80
Water (212^0F)	55.3	Water (390^0F)	34.5
Water (steam)	1.00785	Mineral oil (80^0F)	2.1
Petroleum	2.0-2.2	Heavy oil	3
Gasoline (70^0F)	2	LPG	1.6-1.9
Wood (dry)	2-6	Wood (pressed board)	2.0-2.6
Wood (wet)	10-30	Wax	2.4-6.5
Lime	2.2-2.5	Vaseline	2.2-2.9
Thinner	3.7	Teflon (4f)	2.0
Teflon (FEP)	2.1	Teflon (PCTFE)	2.3-2.8
Teflon (PTFE)	2	Polyester resin	2.8-4.5
Paper (dry)	2	Mica	2.6-3.2
Silica (aluminate)	2	Silica (sand)	2.5-3.5
Paint	5-8	Porcelain	5-7
Corn	5-10	Cereals (dry)	3-5
Ash	1.7-2.0	Industrial alcohol	16-31
Cement (plain)	1.5-2.1	Cement (Portland)	2.5-2.6
Cement (powder)	5-10	Chlorine (-50^0F)	2.0
Chlorine (32^0F)	1.5	Alumina	9.3-11.5

APPENDIX B

GANTT CHART FOR FIRST SEMESTER OF TWO SEMESTERS FINAL YEAR PROJECT

FYP 1

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	**Selection of Project Topic**	■													
	-Propose Topic														
	-Topic assigned to students														
2	**Preliminary Research Work**		■	■											
	-Introduction														
	-Objective														
	-List of references/literature														
	-Project planning														
3	**Submission of Preliminary Report**			●											
4	**Project Work**				■	■	■	■							
	-Reference/Literature														
	-Measurement circuit design / Laboratory Work														
5	**Submission of Progress Report**								●						
6	**Project work continue**								■	■	■	■			
	-switch design/switched capacitor charge transfer circuit design / Laboratory Work														
7	**Submission of Interim Report Final Draft**												●		
8	**Oral Presentation**													●	

9	**Submission of Interim Report**														●

● Suggested milestone

▬ Process

FYP 2

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	**Project work continue**	■	■	■	■											
	-Circuit development															
	-Part by part troubleshooting															
2	**Submission of Progress Report 1**					●										
3	**Project work continue**					■	■	■	■							
	- Circuit development															
	-Part by part troubleshooting															
	-Research and study on imaging															
4	**Submission of Progress Report 2**								●							
5	**Project work continue**								■	■	■	■	■	■	■	
	-Research and study on imaging															
	-Programming on controller															
	-Programming on Visual Basic 6.0															
6	**Submission of Draft Report**													●		
7	**Submission of Final Report**															●
8	**Project work continue**	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	-Troubleshooting and adjustment															
	-Revision on the current project status															

● Suggested milestone

■ Process

APPENDIX C

TRUTH TABLE AND K MAP FOR CONTROL LOGIC CIRCUIT DESIGN

Condition:

- source electrode = 1
- detecting electrodes = 2, 3, 4, 5, 6, 7, 8

State transition diagram

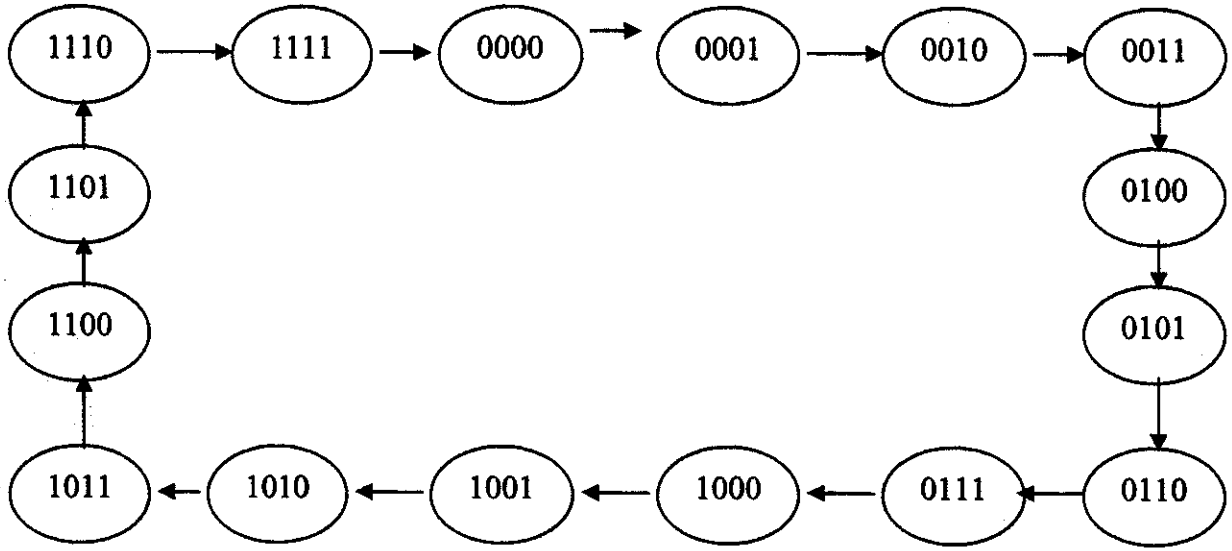


Table Ç1: Switching and multiplexer control status

Multiplexer			S_{1S}	S_{1G}	S_{2S}	S_{2G}	S_{2M}	S_{3S}	S_{3G}	S_{3M}	S_{4S}	S_{4G}	S_{4M}	S_{5S}	S_{5G}	S_{5M}	S_{6S}	S_{6G}	S_{6M}	S_{7S}	S_{8G}	S_{7M}	S_{8G}	S_{8M}
C	B	A																						
X	X	X	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0
X	X	X	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1
X	X	X	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0
0	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1
X	X	X	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0
0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1
X	X	X	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0
0	1	1	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1
X	X	X	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0
1	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1
X	X	X	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0
1	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1
X	X	X	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0
1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1
X	X	X	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0
1	1	1	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1

Table C2: Circuit excitation table

PRESENT STATE				NEXT STATE				J_{Q3}	K_{Q3}	J_{Q2}	K_{Q2}	J_{Q1}	K_{Q1}	J_{Q0}	K_{Q0}
Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0								
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	1	0	0	X	0	1	X	X	1	X	1
1	1	0	0	1	1	0	1	X	0	X	0	0	X	1	X
1	1	0	1	1	1	1	0	X	0	X	0	1	X	X	1
1	1	1	0	1	1	1	1	X	0	X	0	X	0	1	X
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

K maps for control signal of J K flip flops

WX \ YZ	00	01	11	10
00	0	0	0	0
01	0	0	**1**	0
11	X	X	**X**	X
10	X	X	X	X

$J_{Q3} = XYZ$

WX \ YZ	00	01	11	10
00	X	X	X	X
01	X	X	**X**	X
11	0	0	**1**	0
10	0	0	0	0

$K_{Q3} = XYZ$

WX \ YZ	00	01	11	10
00	0	0	**1**	0
01	X	X	**X**	X
11	X	X	**X**	X
10	0	0	**1**	0

$J_{Q2} = YZ$

WX \ YZ	00	01	11	10
00	X	X	**X**	X
01	0	0	**1**	0
11	0	0	**1**	0
10	X	X	**X**	X

$K_{Q2} = YZ$

WX \ YZ	00	01	11	10
00	0	**1**	**X**	X
01	0	**1**	**X**	X
11	0	**1**	**X**	X
10	0	**1**	**X**	X

$J_{Q1} = Z$

WX \ YZ	00	01	11	10
00	X	**X**	**1**	0
01	X	**X**	**1**	0
11	X	**X**	**1**	0
10	X	**X**	**1**	0

$K_{Q1} = Z$

WX \ YZ	00	01	11	10
00	**1**	**X**	**X**	**1**
01	**1**	**X**	**X**	**1**
11	**1**	**X**	**X**	**1**
10	**1**	**X**	**X**	**1**

$J_{Q0} = 1$

WX \ YZ	00	01	11	10
00	**X**	**1**	**1**	**X**
01	**X**	**1**	**1**	**X**
11	**X**	**1**	**1**	**X**
10	**X**	**1**	**1**	**X**

$K_{Q0} = 1$

K maps for control signal of multiplexer

WX \ YZ	00	01	11	10
00	X	X	**1**	**X**
01	X	0	**1**	**X**
11	X	0	**1**	**X**
10	X	0	**1**	**X**

A = Y

WX \ YZ	00	01	11	10
00	X	X	0	X
01	**X**	**1**	**1**	**X**
11	X	0	0	X
10	**X**	**1**	**1**	**X**

$B = \overline{W}X + W\overline{X}$

WX \ YZ	00	01	11	10
00	X	X	0	X
01	X	0	0	X
11	**X**	**1**	**1**	**X**
10	**X**	**1**	**1**	**X**

C = W

K maps for control signal of CMOS switches

WX \ YZ	00	01	11	10
00	**1**	0	0	**1**
01	**1**	0	0	**1**
11	**1**	0	0	**1**
10	**1**	0	0	**1**

$S_{1S} = S_{2G} = S_{3G} = S_{4G} = S_{5G} = S_{6G} = S_{7G} = S_{8G} = \overline{Z}$

WX \ YZ	00	01	11	10
00	0	**1**	**1**	0
01	0	**1**	**1**	0
11	0	**1**	**1**	0
10	0	**1**	**1**	0

$S_{1G} = S_{2M} = S_{3M} = S_{4M} = S_{5M} = S_{6M} = S_{7M} = S_{8M} = Z$

- $S_{2S} = S_{3S} = S_{4S} = S_{5S} = S_{6S} = S_{7S} = 0$

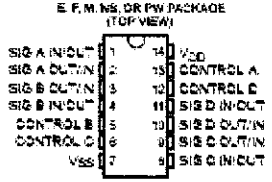
APPENDIX D

CMOS SWITCHES CD4066B DATA SHEET

SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

- 15-V Digital or ±7.5-V Peak-to-Peak Switching
- 125-Ω Typical On-State Resistance for 15-V Operation
- Switch On-State Resistance Matched to Within 5 Ω Over 15-V Signal-Input Range
- On-State Resistance Flat Over Full Peak-to-Peak Signal Range
- High On/Off Output-Voltage Ratio: 80 dB Typical at f_{is} = 10 kHz, R_L = 1 kΩ
- High Degree of Linearity: <0.5% Distortion Typical at f_{is} = 1 kHz, V_{is} = 5 V p-p, $V_{DD} – V_{SS} \geq 10$ V, R_L = 10 kΩ
- Extremely Low Off-State Switch Leakage, Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10 pA Typical at $V_{DD} – V_{SS}$ = 10 V, T_A = 25°C
- Extremely High Control Input Impedance (Control Circuit Isolated From Signal Circuit): 10^{12} Ω Typical
- Low Crosstalk Between Switches: –50 dB Typical at f_{is} = 8 MHz, R_L = 1 kΩ
- Matched Control-Input to Signal-Output Capacitance: Reduces Output Signal Transients
- Frequency Response, Switch On = 40 MHz Typical
- 100% Tested for Quiescent Current at 20 V
- 5-V, 10-V, and 15-V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13-B, *Standard Specifications for Description of "B" Series CMOS Devices*
- Applications:
  - Analog Signal Switching/Multiplexing: Signal Gating, Modulator, Squelch Control, Demodulator, Chopper, Commutating Switch
  - Digital Signal Switching/Multiplexing
  - Transmission-Gate Logic Implementation
  - Analog-to-Digital and Digital-to-Analog Conversion
  - Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain

D, F, M, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full signal-input range.

The CD4066B consists of four bilateral switches, each with independent controls. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 1, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to V_{SS} (when the switch is off). This configuration eliminates the variation of the switch-transistor threshold voltage with input signal and, thus, keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range. However, for sample-and-hold applications, the CD4016B is recommended.

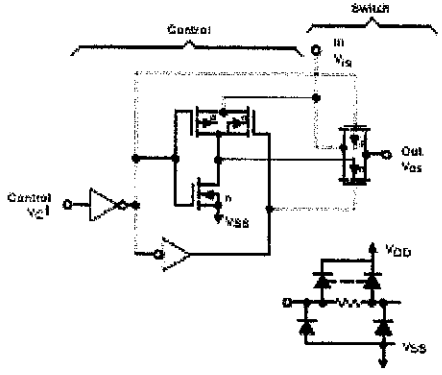
SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

description/ordering information (continued)

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – F	Tube of 25	CD4066BF3A	CD4066BF3A
	PDIP – E	Tube of 25	CD4066BE	CD4066BE
	SOIC – M	Tube of 55	CD4066BM	CD4066BM
		Reel of 2500	CD4066BM96	
		Reel of 250	CD4066BMT	
	SOP – NS	Reel of 2000	CD4066BNSR	CD4066B
	TSSOP – PW	Tube of 90	CD4066BPW	CM066B
		Reel of 2000	CD4066BPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



† All control inputs are protected by the CMOS protection network.

NOTES: A. All unused switches are connected to V_{DD}.
B. Normal operation control-line biasing: switch on (logic 1, VC = VDD), switch off (logic 0, VC = VSS).
C. Signal-level range: $V_{SS} \leq V_{is} \leq V_{DD}$

Figure 1. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry

SCHS057D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

DC supply-voltage range, V_{DD} (voltages referenced to V_{SS} terminal) ..... −0.5 V to 20 V
Input voltage range, V_{IN} (all inputs) ..... −0.5 V to V_{DD} + 0.5 V
DC input current, I_{IN} (any one input) ..... ±10 mA
Package thermal impedance, θ_{JA} (see Note 1): E package ..... 80°C/W
M package ..... 86°C/W
NS package ..... 76°C/W
PW package ..... 113°C/W
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max ..... 265°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	18	V
T_A	Operating free-air temperature	−55	125	°C

SCHS057D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

electrical characteristics

PARAMETER	TEST CONDITIONS	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES −55°C	−40°C	85°C	125°C	25°C TYP	25°C MAX	UNIT
I_{DD}	Quiescent device current	0, 5	5	0.25	0.25	7.5	7.5	0.01	0.25	µA
		0, 10	10	0.5	0.5	15	15	0.01	0.5	
		0, 15	15	1	1	30	30	0.01	1	
		0, 20	20	5	5	150	150	0.02	5	
Signal Inputs (V_{IS}) and Outputs (V_{OS})										
r_{on}	On-state resistance (max)	$V_C = V_{DD}$, $R_L = 10\ k\Omega$ returned to $\frac{(V_{DD} + V_{SS})}{2}$, $V_{IS} = V_{SS}$ to V_{DD}	5	900	850	1200	1300	470	1050	Ω
			10	310	290	500	550	160	400	
			15	200	210	300	320	120	240	
Δr_{on}	On-state resistance difference between any two switches	$R_L = 10\ k\Omega$, $V_C = V_{DD}$	5					15		Ω
			10					10		
			15					5		
THD	Total harmonic distortion	$V_C = V_{DD} = 5$ V, $V_{SS} = -5$ V, $V_{IS(p-p)} = 5$ V (sine wave centered on 0 V), $R_L = 10\ k\Omega$, $f_{IS} = 1$-kHz sine wave						0.4		%
	−3-dB cutoff frequency (switch on)	$V_C = V_{DD} = 5$ V, $V_{SS} = -5$ V, $V_{IS(p-p)} = 5$ V (sine wave centered on 0 V), $R_L = 1\ k\Omega$						40		MHz
	−50-dB feedthrough frequency (switch off)	$V_C = V_{SS} = -5$ V, $V_{IS(p-p)} = 5$ V (sine wave centered on 0 V), $R_L = 1\ k\Omega$						1		MHz
I_{IS}	Input/output leakage current (switch off) (max)	$V_C = 0$ V, $V_{IS} = 18$ V, $V_{OS} = 0$ V, and $V_C = 0$ V, $V_{IS} = 0$ V, $V_{OS} = 18$ V	18	±0.1	±0.1	±1	±1	±1.3×10⁻⁵	±0.1	µA
	−50-dB crosstalk frequency	$V_C(A) = V_{DD} = 5$ V, $V_C(B) = V_{SS} = -5$ V, $V_{IS}(A) = 5$ V_{p-p}, 50-Ω sections, $R_L = 1\ k\Omega$						5		MHz
t_{pd}	Propagation delay (signal input to signal output)	$R_L = 200\ k\Omega$, $V_C = V_{DD}$, $V_{SS} = GND$, $C_L = 50$ pF, $V_{IN} = 10$ V (square wave centered on 5 V), $t_r, t_f = 20$ ns	5					20	40	ns
			10					10	20	
			15					7	15	
C_{IS}	Input capacitance	$V_{DD} = 5$ V, $V_C = V_{SS} = -5$ V						8		pF
C_{OS}	Output capacitance	$V_{DD} = 5$ V, $V_C = V_{SS} = -5$ V						8		pF
C_{IOS}	Feedthrough	$V_{DD} = 5$ V, $V_C = V_{SS} = -5$ V						0.5		pF

electrical characteristics (continued)

CHARACTERISTIC		TEST CONDITIONS	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES						UNIT
				−55°C	−40°C	85°C	125°C	25°C		
								Typ.	Max.	
Control (V$_{IC}$)										
$V_{IL,C}$	Control input low voltage (max)	I_{SS} = 10 μA, V_{SS} = V_{EE}, V_{DS} = V_{DD}, and V_{SS} = VDD, V_{DS} = V_{SS}	5	1	1	1	1		1	V
			10	2	2	2	2		2	
			15	2	2	2	2		2	
$V_{IH,C}$	Control input high voltage	See Figure 6	5	3.5 (MIN.)						V
			10	7 (MIN.)						
			15	11 (MIN.)						
I_{IN}	Input current (max.)	V_{IS} = VDD, VDD − V_{SS} = 15 V, V_{DC} = VDD − V_{SS}	18	±0.1	±0.1	±1	±1	$±10^{-5}$	±0.1	μA
	Crosstalk (control input to signal output)	V_C = 10 V (square wave), t_r, t_f = 20 ns, R_L = 10 kΩ	10					50		mV
	Turn-on and turn-off propagation delay	V_{IN} = VDD, t_r, t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ	5					35	70	ns
			10					20	40	
			15					15	30	
	Maximum control input repetition rate	V_{IS} = VDD, V_{SS} = GND, R_L = 1 kΩ to GND, C_L = 50 pF, V_C = 10 V (square wave) centered on 5 V, t_r, t_f = 20 ns, V_{IS} = 1/2 V_{DD} at 1 kHz	5					8		MHz
			10					9		
			15					9.5		
C_I	Input capacitance							5	7.5	pF

switching characteristics

V_{DD} (V)	V_{IS} (V)	SWITCH INPUT I_{IS} (mA)					SWITCH OUTPUT, V_{OS} (V)	
		−55°C	−40°C	25°C	85°C	125°C	MIN.	MAX.
5	0	0.64	0.61	0.51	0.42	0.36		0.4
5	5	−0.64	−0.61	−0.51	−0.42	−0.36	4.6	
10	0	1.8	1.5	1.3	1.1	0.9		0.5
10	10	−1.8	−1.5	−1.3	−1.1	−0.9	9.5	
15	0	4.2	4	3.4	2.8	2.4		1.5
15	15	−4.2	−4	−3.4	−2.8	−2.4	13.5	

TYPICAL CHARACTERISTICS

TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

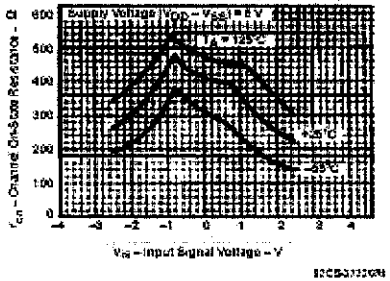


Figure 2

TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

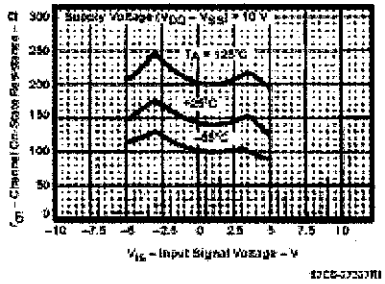


Figure 3

TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

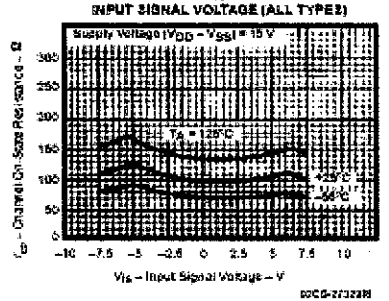


Figure 4

TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

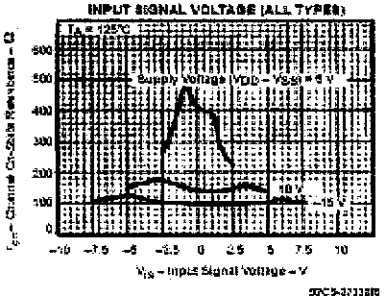


Figure 5

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TYPICAL CHARACTERISTICS

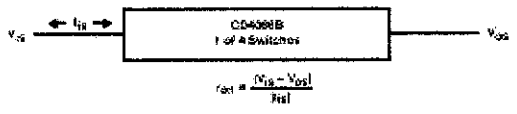

Figure 6. Determination of r_{on} as a Test Condition for Control-Input High-Voltage (V_{IHC}) Specification

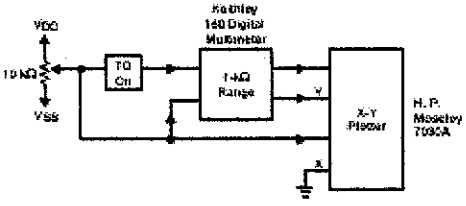

Figure 7. Channel On-State Resistance Measurement Circuit

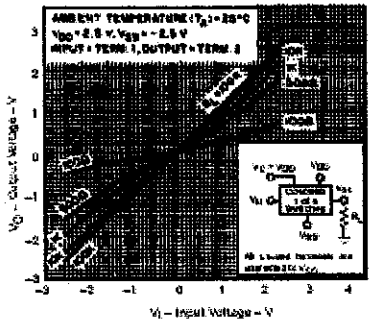

Figure 8

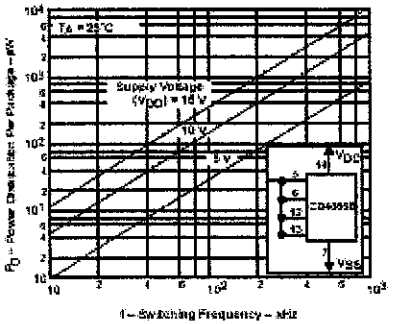

Figure 9

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TYPICAL CHARACTERISTICS

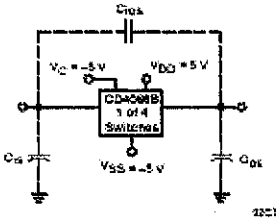


Figure 10. Typical On Characteristics for One of Four Channels

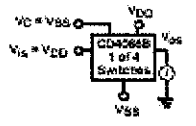


Figure 11. Off-Switch Input or Output Leakage

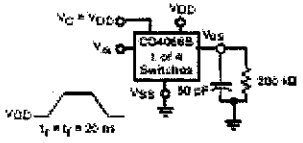


Figure 12. Propagation Delay Time Signal Input (V_{IS}) to Signal Output (V_{OS})

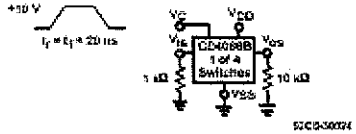
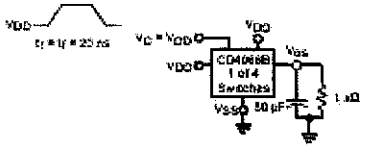


Figure 13. Crosstalk-Control Input to Signal Output

SCHS009J – NOVEMBER 1998 – REVISED SEPTEMBER 2003

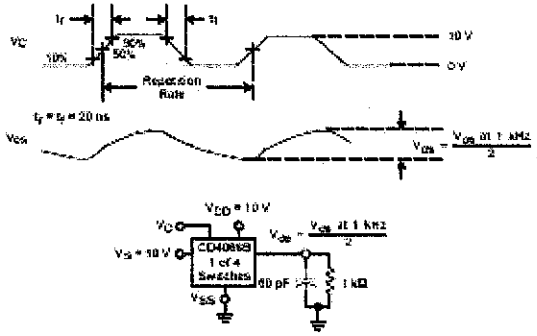
TYPICAL CHARACTERISTICS



NOTES: A. All unused inputs are connected to V_{SS}.
B. Delay is measured at V_{OS} level of ±10% from ground (balanced) or quiescent output level (turnoff).

92CS-30935

Figure 14. Propagation Delay, t_{PLH}, t_{PHL} Control-Signal Output



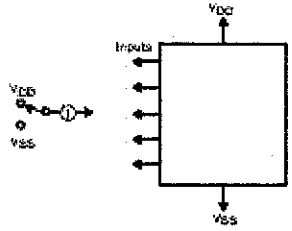
All unused inputs are connected to V_{SS}.

92CS-33925

Figure 15. Maximum Allowable Control-Input Repetition Rate

SCHS009J – NOVEMBER 1998 – REVISED SEPTEMBER 2003

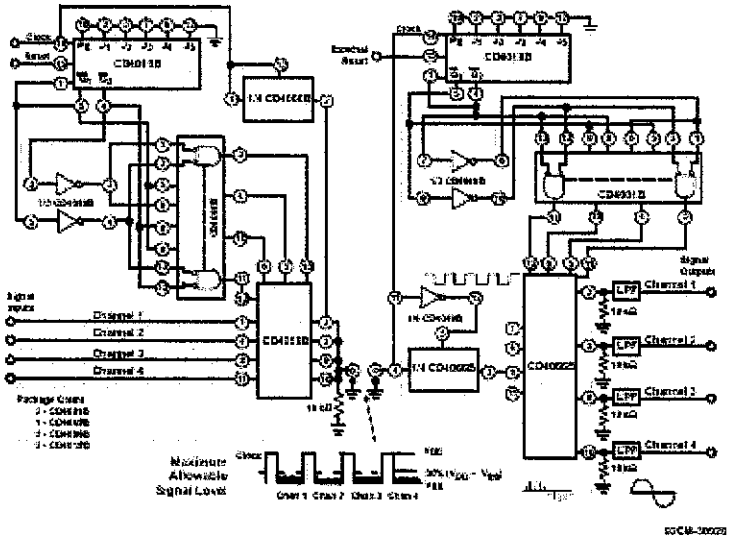
TYPICAL CHARACTERISTICS



92CS-37556

Measure inputs sequentially to both V_{DD} and V_{SS}. Connect all unused inputs to either V_{DD} or V_{SS}. Measure control inputs only.

Figure 16. Input Leakage-Current Test Circuit

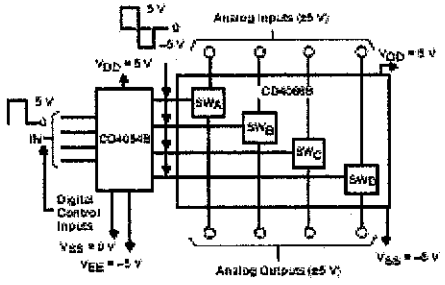


92CM-38029

Figure 17. Four-Channel PAM Multiplex System Diagram

SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

TYPICAL CHARACTERISTICS



SCES-33337

Figure 18. Bidirectional Signal Transmission Via Digital Control Logic

APPENDIX E

OPERATIONAL AMPLIFIER LF353 DATA SHEET

National Semiconductor

August 2000

LF353
Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

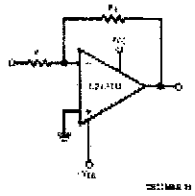
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

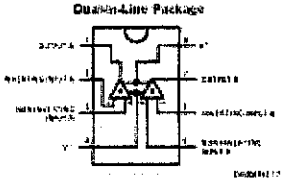
Internally trimmed offset voltage:	10 mV
Low input bias current:	50pA
Low input noise voltage:	25 nV/√Hz
Low input noise current:	0.01 pA/√Hz
Wide gain bandwidth:	4 MHz
High slew rate:	13 V/µs
Low supply current:	3.6 mA
High input impedance:	$10^{12}\Omega$
Low total harmonic distortion:	≤0.02%
Low 1/f noise corner:	50 Hz
Fast settling time to 0.01%:	2 µs

Typical Connection



Connection Diagram

Dual-In-Line Package



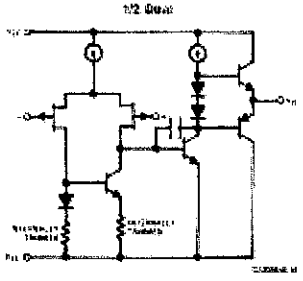
Top View

Order Number LF353M, LF353MX or LF353N

See NS Package Number M08A or N08E

Simplified Schematic

1/2 Dual



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 2)
Operating Temperature Range	0°C to +70°C
T_j(MAX)	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 4)	1700V
θ_{jA} M Package	TBD

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no test is given. However, the typical value is a good indication of device performance.

DC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353 Min	LF353 Typ	LF353 Max	Units
V_{OS}	Input Offset Voltage	R_S=10kΩ, T_A=25°C Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j=25°C. (Notes 5, 6) T_j≤70°C		25	100 4	pA nA
I_B	Input Bias Current	T_j=25°C. (Notes 5, 6) T_j≤70°C		50	200 8	pA nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C V_O=±10V, R_L=2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	R_S≤ 10kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	70	100		dB
I_D	Supply Current			3.6	6.5	mA

AC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353 Min	LF353 Typ	LF353 Max	Units
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz–20 kHz (Input Referred)		−120		dB
SR	Slew Rate	V_S=±15V, T_A=25°C	8.0	13		V/µs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25°C	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω, f=1000 Hz		15		nV/√Hz
i_n	Equivalent Input Noise Current	T_j=25°C, f=1000 Hz		0.01		pA/√Hz

AC Electrical Characteristics (Continued)

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
THD	Total Harmonic Distortion	A_V = +10, R_L = 10k, V_O = 20Vp-p, BW = 20 Hz-20 kHz		≤0.02		%

Note 2: For operating at elevated temperature, the device must be derated based on a thermal resistance of 115°C/W typ (junction to ambient) for the N package, and 150°C/W typ (junction to ambient) for the M package.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: The power dissipation limit, however, cannot be exceeded.

Note 5: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

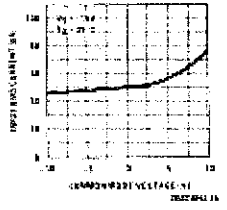
Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias currents are to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±5V to ±15V.

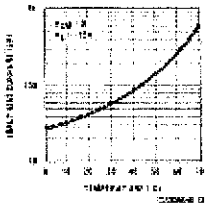
Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

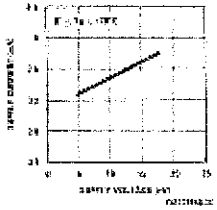
Input Bias Current



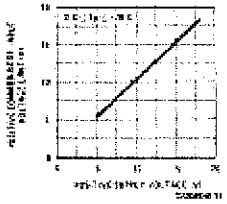
Input Bias Current



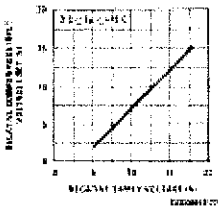
Supply Current



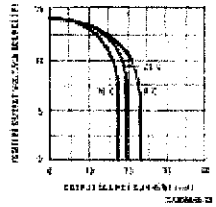
Positive Common-Mode Input Voltage Limit



Negative Common-Mode Input Voltage Limit

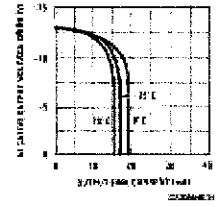


Positive Current Limit

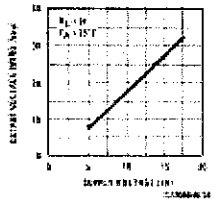


Typical Performance Characteristics (Continued)

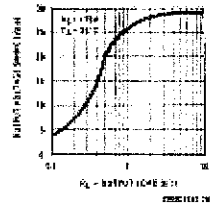
Negative Current Limit



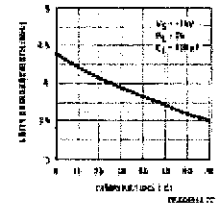
Voltage Swing



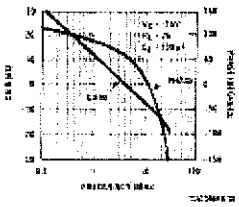
Output Voltage Swing



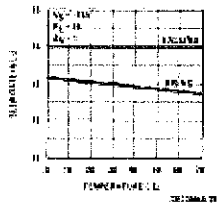
Gain Bandwidth



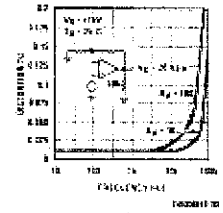
Bode Plot



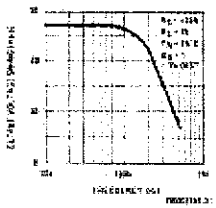
Slew Rate



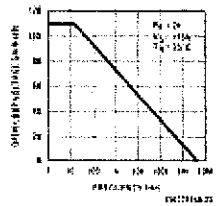
Distortion vs Frequency



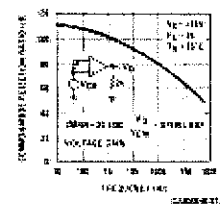
Undistorted Output Voltage Swing



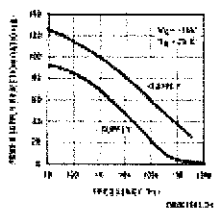
Open Loop Frequency Response



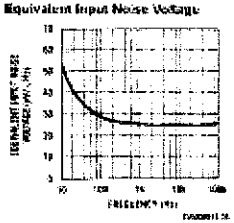
Common-Mode Rejection Ratio



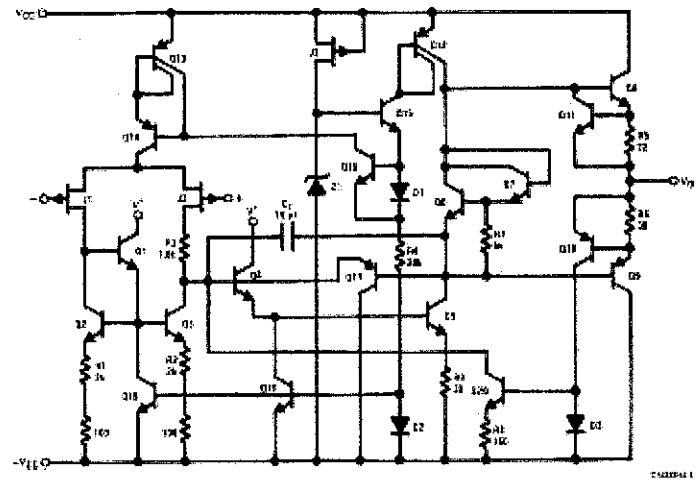
Power Supply Rejection Ratio



Equivalent Input Noise Voltage

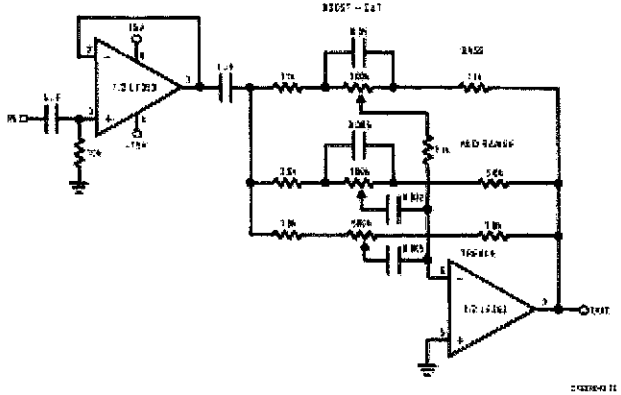


Detailed Schematic

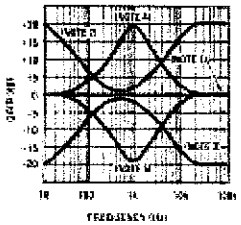


Typical Applications

Three-Band Active Tone Control

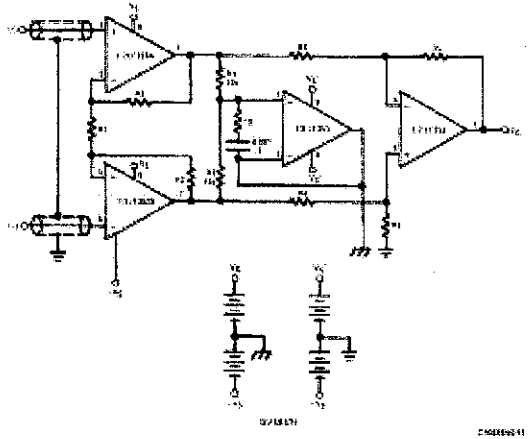


Typical Applications (Continued)



Note 1: All channels flat.
Note 2: Bass and treble boost, max flat.
Note 3: Bass and treble cut, mid flat.
Note 4: Mid boost, bass and treble flat.
Note 5: Mid cut, bass and treble flat.
- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Improved CMRR Instrumentation Amplifier



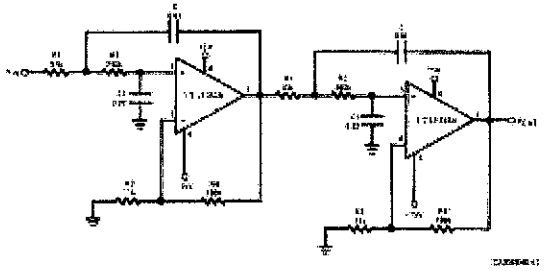
$$A_V = \left(\frac{2R2}{R1} + 1\right)\frac{R5}{R4}$$

Matching of R2's, R4's and R5's controls CMRR.
For $A_V = 1000$, resistor matching = 0.01%, CMRR = 110 dB.

- Very high input impedance
- Super high CMRR

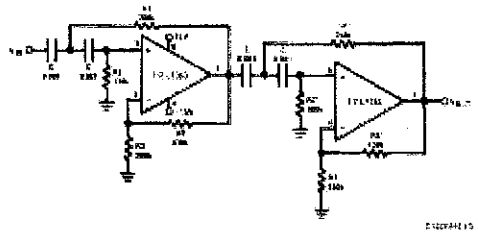
Typical Applications (Continued)

Fourth Order Low Pass Butterworth Filter



- Corner frequency (f_c) = $\frac{\sqrt{\frac{1}{R1R2C1C2}}}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{1}{R1R2C1C2}} = \frac{1}{2\pi}$
- Passband gain (H_0) = 1 + R4/R3 (1 + R6/R5)
- First stage Q = 1.23
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a Butterworth response filter with a corner frequency of 100 Hz and a passband gain of 100.
- Offset nulling necessary for accurate DC performance.

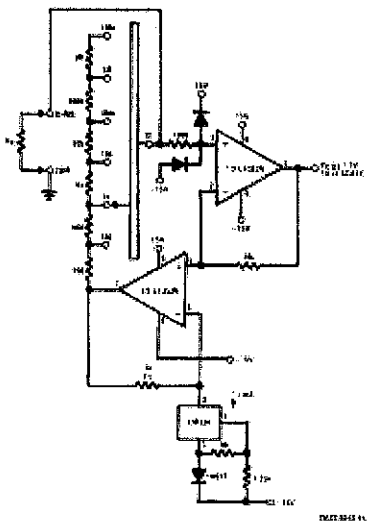
Fourth Order High Pass Butterworth Filter



- Corner frequency (f_c) = $\frac{\sqrt{\frac{1}{R1R2C1C2}}}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{1}{R1R2C1C2}} = \frac{1}{2\pi}$
- Passband gain (H_0) = 1 + R4/R3 (1 + R6/R5)
- First stage Q = 1.23
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10.

Typical Applications (Continued)

Ohms to Volts Converter



$V_O = \frac{1V}{R_{UNKNOWN}} = \Omega_K$

Where $R_{UNKNOWN}$ is the resistance from pin 2 to pin 3 of the LF353.

APPENDIX F

MULTIPLEXER CD4051 DATA SHEET

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS047D

August 1998 - Revised March 2003

CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V_{p-p} can be achieved by digital signal amplitudes of 4.5V to 20V (if V_{DD}-V_{SS} = 5V, a V_{DD}-V_{EE} of up to 13V can be controlled; for V_{DD}-V_{EE} level differences above 13V, a V_{DD}-V_{SS} of at least 4.5V is required). For example, if V_{DD} = +4.5V, V_{SS} = 0V, and V_{EE} = -13.5V, analog signals from +13.5V to -4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD4051BF, CD4052BF, CD4053BF	-55 to 125	16 Ld CERAMIC DIP
CD4051BE, CD4052BE, CD4053BE	-55 to 125	16 Ld PDIP
CD4051BM, CD4051BNS	-55 to 125	16 Ld SOIC
CD4051BPW, CD4052BPW, CD4053BPW	-55 to 125	16 Ld TSSOP

Features

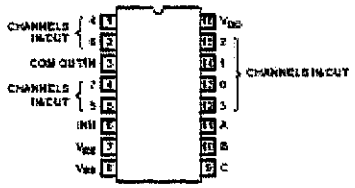
- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . . 3V to 20V
  - Analog . . . . . 20V_{p-p}
- Low ON Resistance, 125Ω (Typ) Over 15V_{p-p} Signal-Input Range for V_{DD}-V_{EE} = 15V
- High OFF Resistance, Channel Leakage of ±100pA (Typ) at V_{DD}-V_{EE} = 15V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V_{DD}-V_{SS} = 3V to 20V) to Switch Analog Signals to 20V_{p-p} (V_{DD}-V_{EE} = 20V)
- Matched Switch Characteristics, r_{ON} = 5Ω (Typ) for V_{DD}-V_{EE} = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2µW (Typ) at V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1µA at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

Applications

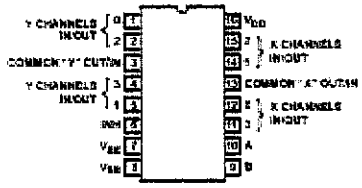
- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

Pinouts

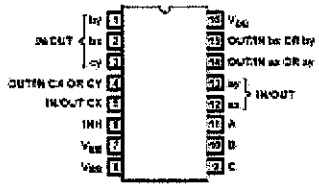
CD4051B (PDIP, CDIP, SOIC, TSSOP)
TOP VIEW



CD4052B (PDIP, CDIP, TSSOP)
TOP VIEW

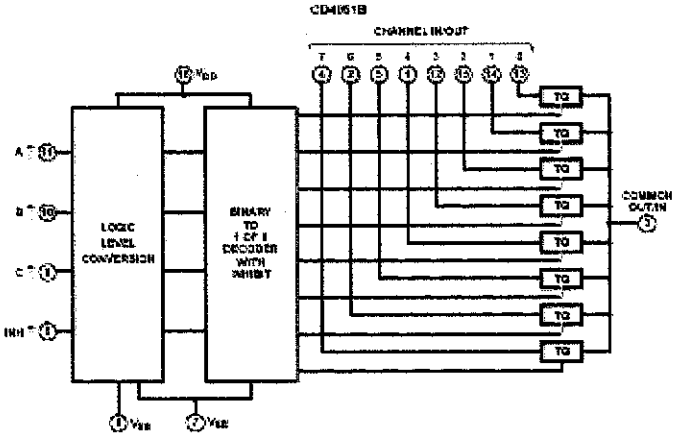


CD4053B (PDIP, CDIP, TSSOP)
TOP VIEW



Functional Block Diagrams

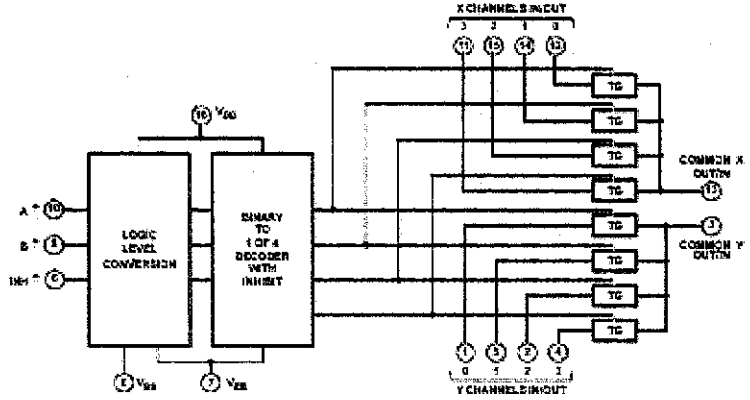
CD4051B



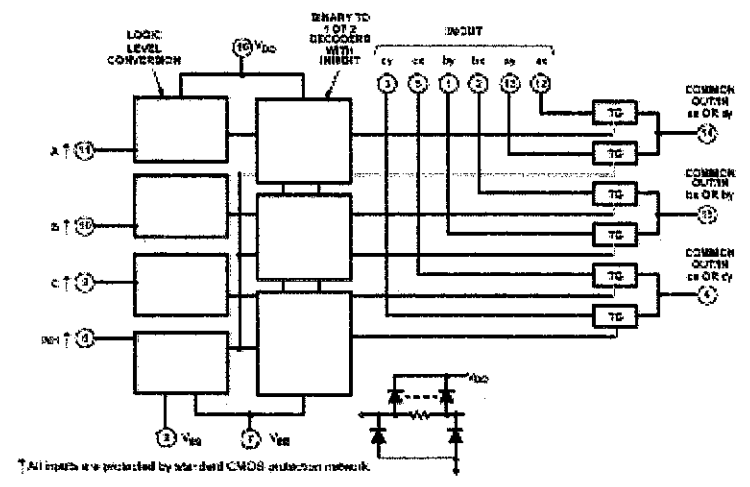
†All inputs are protected by standard CMOS protection network.

Functional Block Diagrams (Continued)

CD4051B



CD4053B



†All inputs are protected by standard CMOS protection network.

TRUTH TABLES

INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
CD4052B				
INHIBIT	B	A		
0	0	0		0x, 0y
0	0	1		1x, 1y
0	1	0		2x, 2y
0	1	1		3x, 3y
1	X	X		None
CD4053B				
INHIBIT	A OR B OR C			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			None

X = Don't Care

Absolute Maximum Ratings

Supply Voltage (V_{++} to V_{--})
Voltages Referenced to V_{SS} Terminal ..... -0.5V to 20V
DC Input Voltage Range ..... -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input ..... ±10mA

Operating Conditions

Temperature Range ..... -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
E Package	67	N/A
F Package	115	45
D Package	73	N/A
NS Package	64	N/A
PW Package	108	N/A

Maximum Junction Temperature (Ceramic Package) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 265°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD51.

Electrical Specifications

Common Conditions Unless Otherwise Specified in Table is For the Full Temp. Range, $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_L = 10k\Omega$, Unless Otherwise Specified (Note 3)

PARAMETER	CONDITIONS V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) -55	-40	85	125	25 MIN	25 TYP	25 MAX	UNITS
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})												
Quiescent Device Current, I_{DD} Max	-	-	-	5	5	5	150	150	-	0.04	5	µA
	-	-	-	10	10	10	300	300	-	0.04	10	µA
	-	-	-	15	20	20	600	600	-	0.04	20	µA
	-	-	-	20	100	100	3000	3000	-	0.06	100	µA
Drain to Source ON Resistance $r_{DS(ON)}$ Max (Note 2) $V_{IS} = V_{DD}$	-	0	0	5	600	650	1300	1300	-	470	1050	Ω
	-	0	0	10	310	330	520	550	-	160	400	Ω
	-	0	0	15	200	210	360	520	-	125	240	Ω
Change in ON Resistance (Between Any Two Channels), Δr_{ON}	-	0	0	5	-	-	-	-	-	15	-	Ω
	-	0	0	10	-	-	-	-	-	10	-	Ω
	-	0	0	15	-	-	-	-	-	5	-	Ω
OFF Channel Leakage Current, Any Channel OFF (Max) or ALL Channels OFF) Common OUT/IN, (Max)	-	0	0	18	±100 (Note 2)		±300 (Note 2)		-	±0.01	±100 (Note 2)	nA
Capacitance, Input, C_{IS}	-	+5	5-	5	-	-	-	-	-	5	-	pF
Output, C_{OS} CD4051					-	-	-	-	-	30	-	pF
CD4052					-	-	-	-	-	18	-	pF
CD4053					-	-	-	-	-	9	-	pF
Feedthrough C_{IOS}					-	-	-	-	-	0.2	-	pF
Propagation Delay Time (Signal Input to Output)	V_{IS}	$R_L = 200k\Omega$, $C_L = 50pF$, $t_r, t_f = 20ns$		5	-	-	-	-	-	30	60	ns
				10	-	-	-	-	-	15	30	ns
				15	-	-	-	-	-	10	20	ns

Electrical Specifications

Common Conditions Unless Otherwise Specified in Table is For the Full Temp. Range, $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_L = 10k\Omega$, Unless Otherwise Specified (Continued) (Note 3)

PARAMETER	CONDITIONS V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) -55	-40	85	125	25 MIN	25 TYP	25 MAX	UNITS
CONTROL (ADDRESS OR INHIBIT), V_C												
Input Low Voltage, V_{IL}, Max	$V_{IS} = V_{DD}$ through 1kΩ; $V_{IS} = V_{SS}$ through 1kΩ	$V_{EE} = V_{SS}$, $R_L = 1k\Omega$ to V_{SS}, $I_{IS} = 2\mu A$ on All OFF Channels		5	1.5	1.5	1.5	1.5	-	-	1.5	V
				10	3	3	3	3	-	-	3	V
				15	4	4	4	4	-	-	4	V
Input High Voltage, V_{IH}, Min				5	3.5	3.5	3.5	3.5	3.5	-	-	V
				10	7	7	7	7	7	-	-	V
				15	11	11	11	11	11	-	-	V
Input Current, I_{IN} (Max)	$V_{IN} = 0, 18$			18	±0.1	±0.1	±1	±1	-	$\pm 10^{-5}$	±0.1	µA
Propagation Delay Time Address-to-Signal OUT (Channel ON or OFF) See Figure 10, 11, 14	$t_r, t_f = 20ns$, $C_L = 50pF$, $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	460	720	ns
		0	0	10	-	-	-	-	-	180	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-5	0	5	-	-	-	-	-	225	450	ns
Propagation Delay Time Inhibit-to-Signal OUT (Channel Turning ON) See Figure 11	$t_r, t_f = 20ns$, $C_L = 50pF$, $R_L = 1k\Omega$	0	0	5	-	-	-	-	-	460	720	ns
		0	0	10	-	-	-	-	-	180	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-10	0	5	-	-	-	-	-	200	400	ns
Propagation Delay Time Inhibit-to-Signal OUT (Channel Turning OFF) See Figure 15	$t_r, t_f = 20ns$, $C_L = 50pF$, $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	350	450	ns
		0	0	10	-	-	-	-	-	90	210	ns
		0	0	15	-	-	-	-	-	70	180	ns
		-10	0	5	-	-	-	-	-	130	300	ns
Input Capacitance, C_{IN} (Any Address or Inhibit Input)					-	-	-	-	-	5	7.5	pF

NOTE:

2. Determined by the minimum leakage measurements for automatic testing.

Electrical Specifications

PARAMETER	TEST CONDITIONS V_{IS} (V)	V_{DD} (V)	R_L (kΩ)			LIMITS TYP	UNITS
Cutoff (-3dB) Frequency Channel ON (Sine Wave Input)	5 (Note 3)	10	1	V_{OS} at Common OUT/IN	CD4051	50	MHz
	$V_{EE} = V_{SS}$, $20\log\frac{V_{OS}}{V_{IS}} = -3dB$				CD4052	25	MHz
					CD4053	20	MHz
				V_{OS} at Any Channel		60	MHz

Electrical Specifications

PARAMETER	TEST CONDITIONS					LIMITS	UNITS
	V_{IS} (V)	V_{DD} (V)	R_L (kΩ)			TYP	
Total Harmonic Distortion, THD	2 (Note 3)	5	10			0.4	%
	5 (Note 3)	10				0.2	%
	8 (Note 3)	15				0.12	%
	$V_{EE} = V_{SS}$, f_{IS} = 1kHz Sine Wave						%
-40dB Feedthrough Frequency (All Channels OFF)	5 (Note 3)	10	1	V_{OS} at Common OUT/IN	CD4051	6	MHz
	$V_{EE} = V_{SS}$, $20\log\frac{V_{OS}}{V_{IS}} = -40dB$				CD4052	10	MHz
					CD4053	12	MHz
				V_{OS} at Any Channel		6	MHz
-40dB Signal Crosstalk Frequency	5 (Note 3)	10	1	Between Any 2 Channels		3	MHz
	$V_{EE} = V_{SS}$, $20\log\frac{V_{OS}}{V_{IS}} = -40dB$			Between Sections, CD4052 Only	Measured on Common	6	MHz
					Measured on Any Channel	10	MHz
				Between Any Two Sections, CD4053 Only	In Pin 2, Out Pin 14	2.5	MHz
					In Pin 15, Out Pin 14	6	MHz
Address-to-Inhibit Pin Signal Crosstalk	-	10	10 (Note 4)			65	mV_{PEAK}
	V_{EE} = 0, V_{SS} = 0, t_r, t_f = 20ns, V_{CC} = V_{DD} - V_{SS} (Square Wave)					65	mV_{PEAK}

NOTES:

3. Peak-to-Peak voltage symmetrical about $\frac{V_{DD} - V_{EE}}{2}$
4. Both sides of channel.

Typical Performance Curves

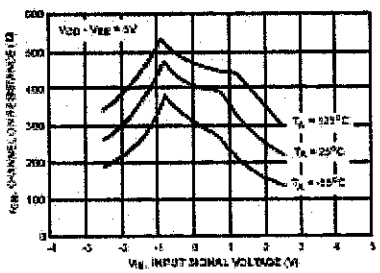


FIGURE 1. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

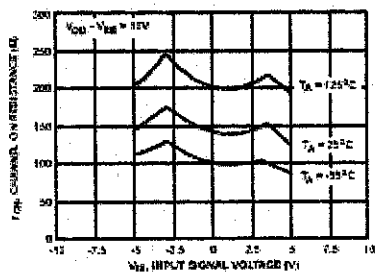
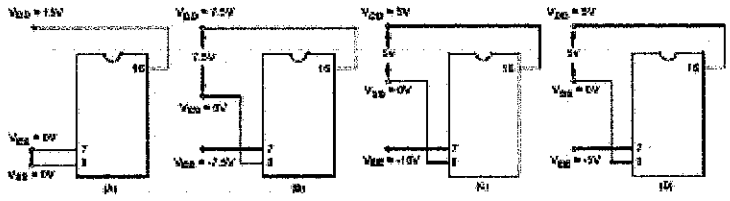


FIGURE 2. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Test Circuits and Waveforms



NOTE: The ADDRESS (digital-control inputs) and INHIBIT logic levels are "0" = V_{SS} and "1" = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

FIGURE 9. TYPICAL BIAS VOLTAGES

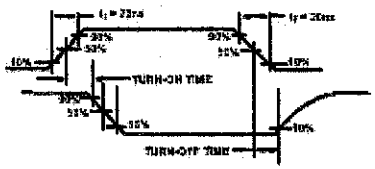


FIGURE 10. WAVEFORMS, CHANNEL BEING TURNED ON (R_L = 1kΩ)

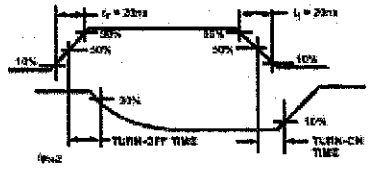


FIGURE 11. WAVEFORMS, CHANNEL BEING TURNED OFF (R_L = 1kΩ)

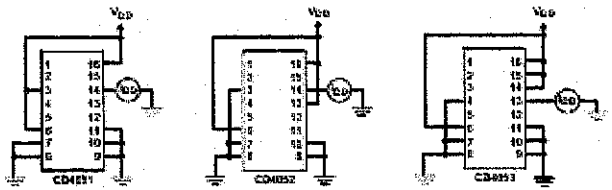


FIGURE 12. OFF CHANNEL LEAKAGE CURRENT - ANY CHANNEL OFF

APPENDIX G

PIC16F877 (ADC CONVERSION)

MICROCHIP

PIC16F87X

28/40-Pin 8-Bit CMOS FLASH Microcontrollers

Devices Included in this Data Sheet:

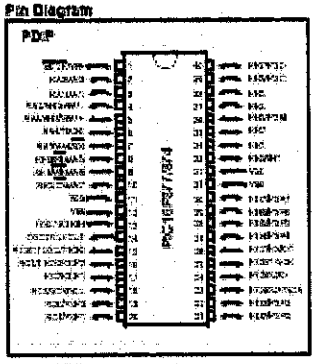
- PIC16F873
- PIC16F874
- PIC16F876
- PIC16F877

Microcontroller Core Features:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of FLASH Program Memory, Up to 368 x 8 bytes of Data Memory (RAM)
  Up to 256 x 8 bytes of EEPROM Data Memory
- Pinout compatible to the PIC16C73B/74B/76/77
- Interrupt capability (up to 14 sources)
- Eight level deep hardware stack
- Direct, indirect and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS FLASH/EEPROM technology
- Fully static design
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Single 5V In-Circuit Serial Programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.0V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial, Industrial and Extended temperature ranges
- Low-power consumption:
  - < 0.6 mA typical @ 3V, 4 MHz
  - 20 µA typical @ 3V, 32 kHz
  - < 1 µA typical standby current

Pin Diagram

PDIP



Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during SLEEP via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI™ (Master mode) and I²C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls (40/44-pin only)
- Brown-out detect circuitry for Brown-out Reset (BOR)

11.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has five inputs for the 28-pin devices and eight for the other devices.

The analog input charges a sample and hold capacitor. The output of the sample and hold capacitor is the input into the converter. The converter then generates a digital result of this analog level via successive approximation. The A/D conversion of the analog input signal results in a corresponding 10-bit digital number. The A/D module has high and low voltage reference input that is software selectable to some combination of VDD, VSS, RA2, or RA3.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in SLEEP, the A/D clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register0 (ADCON0)
- A/D Control Register1 (ADCON1)

The ADCON0 register, shown in Register 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 11-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be the voltage reference), or as digital I/O.

Additional information on using the A/D module can be found in the Microchip™ Mid-Range MCU Family Reference Manual (DS33023).

REGISTER 11-1: ADCON0 REGISTER (ADDRESS: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits
00 = Fosc/2
01 = Fosc/8
10 = Fosc/32
11 = FRC (clock derived from the internal A/D module RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits
000 = channel 0, (RA0/AN0)
001 = channel 1, (RA1/AN1)
010 = channel 2, (RA2/AN2)
011 = channel 3, (RA3/AN3)
100 = channel 4, (RA5/AN4)
101 = channel 5, (RE0/AN5)(1)
110 = channel 6, (RE1/AN6)(1)
111 = channel 7, (RE2/AN7)(1)

bit 2 **GO/DONE:** A/D Conversion Status bit
If ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (this bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1 Unimplemented: Read as '0'

bit 0 **ADON:** A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shut-off and consumes no operating current

Note 1: These channels are not available on PIC16F873/876 devices.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 11-2: ADCON1 REGISTER (ADDRESS 9Fh)

U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified. 6 Most Significant bits of ADRESH are read as '0'.
0 = Left justified. 6 Least Significant bits of ADRESL are read as '0'.

bit 6-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG3: PCFG0	AN7[1] RE2	AN6[1] RE1	AN5[1] RE0	AN4 RA5	AN3 RA3	AN2 RA2	AN1 RA1	AN0 RA0	VREF+	VREF-	CHAN/ REFS[2]
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	RA3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	RA3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	RA3	VSS	2/1
0110	D	D	D	D	D	D	D	D	VDD	VSS	0/0
0111	A	A	A	A	VREF+	VREF-	A	A	RA3	RA2	6/2
1000	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1001	D	D	A	A	VREF+	A	A	A	RA3	VSS	5/1
1010	D	D	A	A	VREF+	VREF-	A	A	RA3	RA2	4/2
1011	D	D	D	A	VREF+	VREF-	A	A	RA3	RA2	3/2
1100	D	D	D	D	VREF+	VREF-	A	A	RA3	RA2	2/2
1101	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1110	D	D	D	D	VREF+	VREF-	D	A	RA3	RA2	1/2

A = Analog input D = Digital I/O

Note 1: These channels are not available on PIC16F873/876 devices.
2: This column indicates the number of analog channels available as A/D inputs and the number of analog channels used as voltage reference inputs.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D result register pair, the GO/DONE bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 11-1.

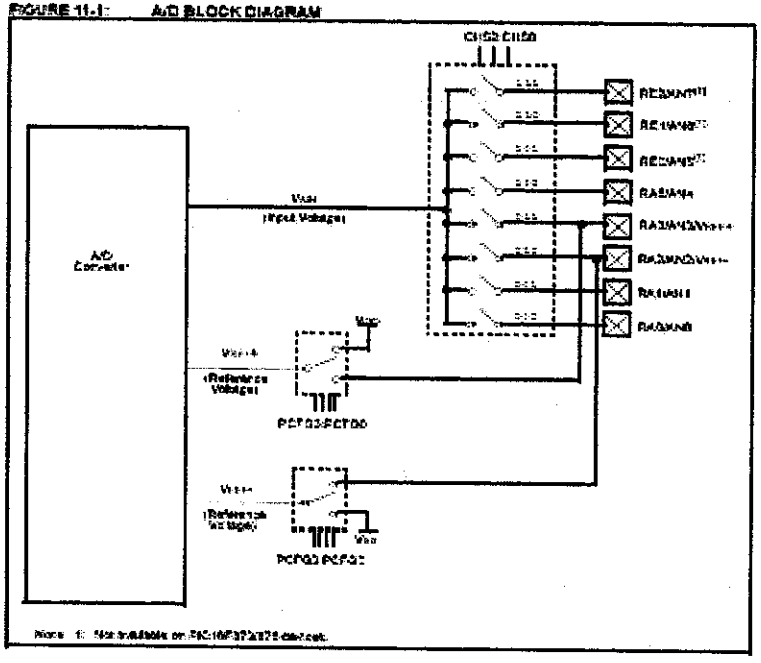
After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To determine acquisition time, see Section 11.1. After the acquisition time has elapsed, the A/D conversion can be started.

These steps should be followed for doing an A/D Conversion:

1. Configure the A/D module:
   - Configure analog pin/voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set PEIE bit
   - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
   - Set GO/DONE bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/DONE bit to be cleared (with interrupts enabled), OR
   - Waiting for the A/D interrupt
6. Read A/D result register pair (ADRESH:ADRESL), clear bit ADIF if required.
7. For the next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before the next acquisition starts.

FIGURE 11-1: A/D BLOCK DIAGRAM



Note 1: Not available on PIC16F872/876 devices.

APPENDIX H

MAX232 DATA SHEET

19-4323; Rev 10; 8/03

MAXIM

+5V-Powered, Multichannel RS-232 Drivers/Receivers

General Description

The MAX220–MAX249 family of line drivers/receivers is intended for all EIA/TIA-232E and V.28/V.24 communications interfaces, particularly applications where ±12V is not available.

These parts are especially useful in battery-powered systems, since their low-power shutdown mode reduces power dissipation to less than 5µW. The MAX225, MAX233, MAX235, and MAX245/MAX246/MAX247 use no external components and are recommended for applications where printed circuit board space is critical.

Applications

Portable Computers
Low-Power Modems
Interface Translation
Battery-Powered RS-232 Systems
Multidrop RS-232 Networks

Features

Superior to Bipolar

- Operate from Single +5V Power Supply (+5V and +12V—MAX231/MAX239)
- Low-Power Receive Mode in Shutdown (MAX223/MAX242)
- Meet All EIA/TIA-232E and V.28 Specifications
- Multiple Drivers and Receivers
- 3-State Driver and Receiver Outputs
- Open-Line Detection (MAX249)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic DIP
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220C/D	0°C to +70°C	Dice*
MAX220EPE	-40°C to +85°C	16 Plastic DIP
MAX220ESE	-40°C to +85°C	16 Narrow SO
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220EJE	-40°C to +85°C	16 CERDIP
MAX220MJE	-55°C to +125°C	16 CERDIP

Ordering information continued at end of data sheet.
Contact factory for dice specifications.

Selection Table

Part Number	Power Supply (V)	No. of RS-232 Drivers/Rx	No. of Ext. Caps	Nominal Cap. Value (µF)	SHDN & Three-State	Rx Active-in SHDN	Data Rate (kbps)	Features
MAX220	+5	2/2	4	0.1	No	—	120	Ultra-low-power, industry-standard pinouts
MAX222	+5	2/2	4	0.1	Yes	—	200	Low-power shutdown
MAX223 (MAX213)	+5	4/5	4	1.0 (0.1)	Yes	●	120	MAX241 and receivers active in shutdown
MAX225	+5	5/5	0	—	Yes	●	120	Available in SO
MAX230 (MAX200)	+5	5/0	4	1.0 (0.1)	Yes	—	120	5 drivers with shutdown
MAX231 (MAX201)	+5 and +7.5 to +13.2	2/2	4	1.0 (0.1)	No	—	120	Standard +5V or battery supplies; same functions as MAX232
MAX232 (MAX202)	+5	2/2	4	1.0 (0.1)	No	—	120 (154)	Industry standard
MAX232A	+5	2/2	4	0.1	No	—	200	Higher slew rate, small caps
MAX233 (MAX203)	+5	2/2	0	—	No	—	120	No external caps
MAX233A	+5	2/2	0	—	No	—	200	No external caps, high slew rate
MAX234 (MAX204)	+5	4/0	4	1.0 (0.1)	No	—	120	Replaces 1488
MAX235 (MAX205)	+5	5/5	0	—	Yes	—	120	No external caps
MAX236 (MAX206)	+5	4/3	4	1.0 (0.1)	Yes	—	120	Shutdown, three caps
MAX237 (MAX207)	+5	5/3	4	1.0 (0.1)	No	—	120	Complements IBM PC serial port
MAX238 (MAX208)	+5	4/4	4	1.0 (0.1)	No	—	120	Replaces 1488 and 1489
MAX239 (MAX209)	+5 and +7.5 to +13.2	4/5	4	1.0 (0.1)	No	—	120	Standard +5V or 12V or battery supplies; single-package solution for IBM PC serial port
MAX240	+5	5/5	4	1.0	Yes	—	120	DIP or flatpack package
MAX241 (MAX211)	+5	4/5	4	1.0 (0.1)	Yes	—	120	Complete IBM PC serial port
MAX242	+5	2/2	4	0.1	Yes	●	200	Separate shutdown and enable
MAX245	+5	8/0	4	0.1	Yes	—	200	Open-line detection simplifies cabling
MAX244	+5	8/10	4	1.0	No	—	120	High slew rate
MAX245	+5	8/10	0	—	Yes	●	120	High slew rate, int. caps, not-shutdown modes
MAX246	+5	8/10	0	—	Yes	●	120	High slew rate, int. caps, three-shutdown modes
MAX247	+5	8/9	0	—	Yes	●	120	High slew rate, int. caps, nine operating modes
MAX248	+5	8/8	4	1.0	Yes	●	120	High slew rate, selective half-chip enables
MAX249	+5	6/10	4	1.0	Yes	●	120	Available in quad flatpack package

ABSOLUTE MAXIMUM RATINGS—MAX223/MAX230–MAX241

V+ ..... (Vcc + 0.3V) to +14V
V- ..... +0.3V to -14V
Input Voltages
TIN ..... -0.3V to (Vcc + 0.3V)
RIN ..... ±30V
Output Voltages
TOUT ..... (V+ + 0.3V) to (V- - 0.3V)
ROUT ..... -0.3V to (Vcc + 0.3V)
Short-Circuit Duration, TOUT ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
24-Pin Narrow Plastic DIP (derate 13.33mW/°C above +70°C) 1.07W
24-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 600mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) 800mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C) 941mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) 1W
44-Pin Plastic FP (derate 11.11mW/°C above +70°C) 889mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) 889mW
24-Pin Narrow CERDIP (derate 12.90mW/°C above +70°C) 1W
24-Pin Sidebraze (derate 20.00mW/°C above +70°C) 1.6W
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX2__C_ _ ..... 0°C to +70°C
MAX2__E_ _ ..... -40°C to +85°C
MAX2__M_ _ ..... -55°C to +125°C
Storage Temperature Ranges ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX223/MAX230–MAX241

(MAX223/230/232/234/235/237/238/240/241, Vcc = +5V ±10; MAX233/MAX235, Vcc = 5V ±5%, C1–C4 = 1.0µF; MAX231/MAX239, Vcc = 5V ±10%; V+ = 7.5V to 13.2V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±7.5		V
Vcc Power-Supply Current	No load, T_A = +25°C	MAX232/233		6	10	mA
		MAX223/230/234–235/240/241		7	15	
		MAX231/239		0.4	1	
V+ Power-Supply Current		MAX231		1.8	5	mA
		MAX239		3	10	
Shutdown Supply Current	T_A = +25°C	MAX223		15	50	µA
		MAX230/235/236/240/241		1	10	
Input Logic Threshold Low	TIN; EN, SHDN (MAX233); EN, SHDN (MAX230/235–241)				0.8	V
Input Logic Threshold High	TIN		2.0			V
	EN, SHDN (MAX223); EN, SHDN (MAX230/235/240/241)		2.4			
Logic Pull-Up Current	TIN = 0V			1.5	20.0	µA
Receiver Input Voltage Operating Range			-30		30	V

ELECTRICAL CHARACTERISTICS—MAX223/MAX230–MAX241 (continued)

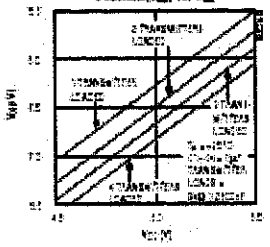
(MAX223/230/232/234/235/237/238/240/241, V_{CC} = +5V ±10; MAX223/MAX235, V_{CC} = 5V ±5%; C1–C4 = 1.0µF; MAX231/MAX239, V_{CC} = 5V ±10%; V_+ = 7.5V to 13.2V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
RS-232 Input Threshold Low	T_A = +25°C, V_{CC} = 5V	Normal operation ($\overline{SHDN}$ = 5V (MAX223); $\overline{SHDN}$ = 0V (MAX225/235/236/240/241))		0.8	1.2		V
		Shutdown (MAX223) ($\overline{SHDN}$ = 0V, $\overline{EN}$ = 5V (R_{IN}, R_{SD}))		0.6	1.5		
RS-232 Input Threshold High	T_A = +25°C, V_{CC} = 5V	Normal operation ($\overline{SHDN}$ = 5V (MAX223); $\overline{SHDN}$ = 0V (MAX225/235/240/241))			1.7	2.4	V
		Shutdown (MAX223) ($\overline{SHDN}$ = 0V, $\overline{EN}$ = 5V (R_{IN}, R_{SD}))			1.5	2.4	
RS-232 Input Hysteresis	V_{CC} = 5V, no hysteresis in shutdown			0.2	0.5	1.0	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 1.6mA (MAX231/232/233), I_{OUT} = 3.2mA)					0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1mA			3.5	V_{CC} - 0.4		V
TTL/CMOS Output Leakage Current	0V ≤ R_{OUT} ≤ V_{CC}; $\overline{EN}$ = 0V (MAX223); $\overline{EN}$ = V_{CC} (MAX236–241)				0.05	±10	µA
Receiver Output Enable Time	Normal operation	MAX223			600		ns
		MAX225/235/239/240/241			400		
Receiver Output Disable Time	Normal operation	MAX223			500		ns
		MAX225/235/239/240/241			250		
Propagation Delay	RS-232 IN to TTL/CMOS OUT, C_L = 150pF	Normal operation			0.5	10	µs
		$\overline{SHDN}$ = 0V (MAX223)	t_{PHL}		4	40	
			t_{PLH}		6	40	
Transition Region Slew Rate	MAX223/MAX230/MAX234–241, T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V			3	5.1	30	V/µs
	MAX231/MAX232/MAX233, T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V				4	30	
Transmitter Output Resistance	V_{CC} = V_+ = V_- = 0V, V_{OUT} = ±2V			300			Ω
Transmitter Output Short-Circuit Current					±10		mA

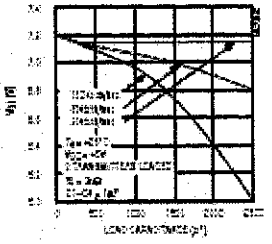
Typical Operating Characteristics

MAX223/MAX230–MAX241

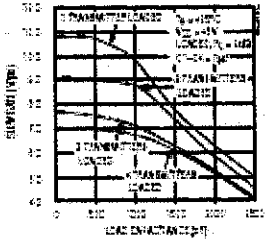
TRANSMITTER OUTPUT VOLTAGE (V_{OUT}) vs. V_{CC}



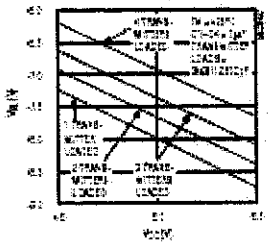
TRANSMITTER OUTPUT VOLTAGE (V_{OUT}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



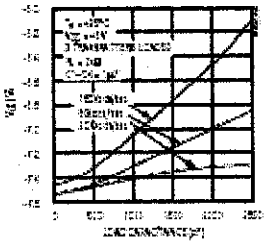
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



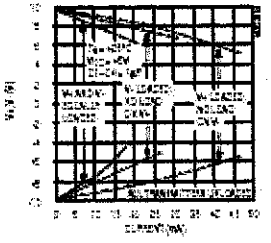
TRANSMITTER OUTPUT VOLTAGE (V_{OUT}) vs. V_{CC}



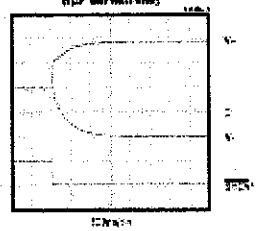
TRANSMITTER OUTPUT VOLTAGE (V_{OUT}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



TRANSMITTER OUTPUT VOLTAGE (V_+, V_-) vs. LOAD CURRENT



V_+, V_- vs. CHARGE-PUMP CAPACITANCE



Tables 1a–1d define the control states. The MAX244 has no control pins and is not included in these tables.

The MAX245 has ten receivers and eight drivers with two control pins, each controlling one side of the device. A logic high at the A-side control input ($\overline{ENA}$) causes the four A-side receivers and drivers to go into a three-state mode. Similarly, the B-side control input ($\overline{ENB}$) causes the four B-side drivers and receivers to go into a three-state mode. As in the MAX245, one A-side and one B-side receiver (RA5 and RB5) remain active at all times. The entire device is put into shutdown mode when both the A and B sides are disabled ($\overline{ENA}$ = $\overline{ENB}$ = +5V).

The MAX247 provides nine receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs each control four drivers. The ninth receiver (RB5) is always active. The device enters shutdown mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX248 provides eight receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control four drivers each. This part does not have an always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX249 provides ten receivers and six drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control five receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control three drivers each. There is no always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$. In shutdown mode, active receivers operate in a low-power receive mode at data rates up to 20kbits/sec.

Applications Information

Figures 5 through 25 show pin configurations and typical operating circuits. In applications that are sensitive to power-supply noise, VCC should be decoupled to ground with a capacitor of the same value as C1 and C2 connected as close as possible to the device.

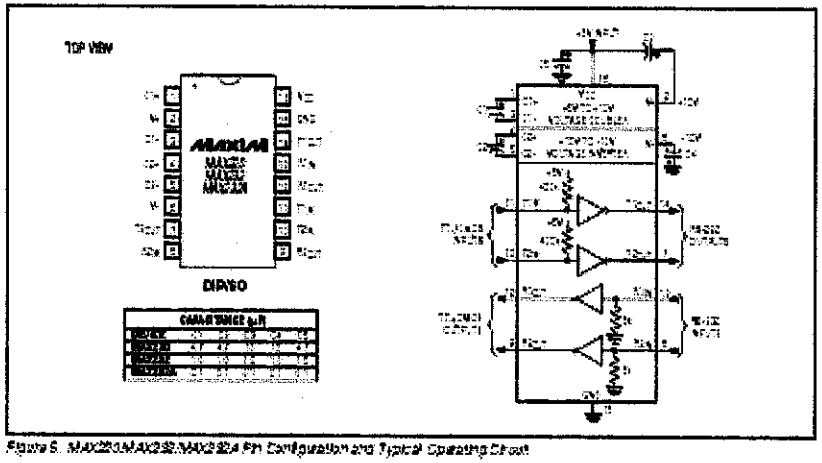


Figure 5. MAX220/MAX232/MAX232A Pin Configuration and Typical Operating Circuit

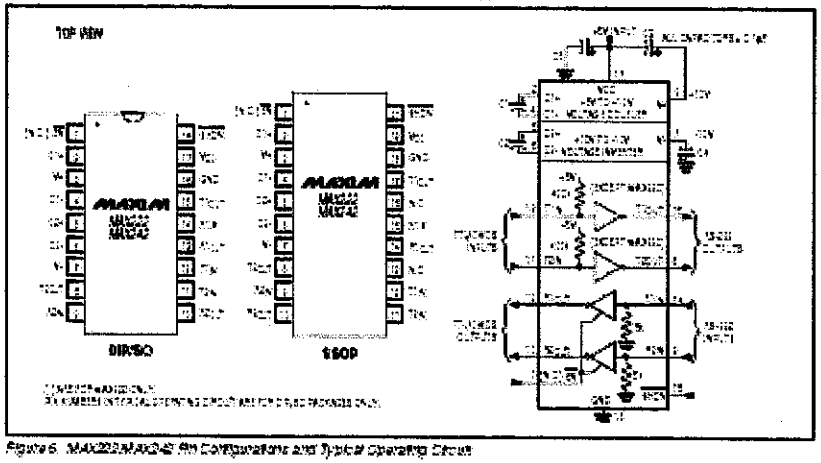


Figure 6. MAX222/MAX242 Pin Configurations and Typical Operating Circuit