NMOS DEVICE OPTIMIZATION AND FABRICATION USING ATHENA & ATLAS SIMULATION SOFTWARE

by

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Dissertation submitted in partial fulfilment of
the requirements for the
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CERTIFICATION OF APPROVAL

FABRICATION AND OPTIMIZATION OF NMOS DEVICE USING ATHENA & ATLAS PROCESS AND DEVICE SIMULATION

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A project dissertation submitted to the
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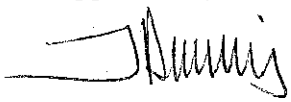

(Dr John Ojur Dennis)

UNIVERSITI TEKNOLOGI PETRONAS

TRONOH, PERAK

DECEMBER 2004

CERTIFICATION OF ORIGINALITY

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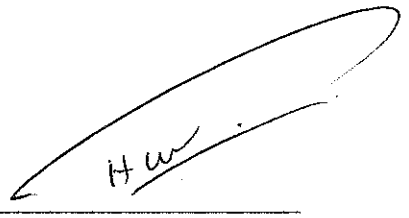

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ABSTRACT

Experiment has proven that NMOS performs better than PMOS due to higher drive current, higher mobility, easier to implement scaling technology and low power consumption. However, there is still room for further optimization as the technology trend for the miniaturization of NMOS and integrated devices continue to grow. In this project, several objectives have been outlined to be completed within 2 semester period. These include detailed understanding of fabrication aspect and NMOS properties, optimizing NMOS by reducing threshold voltage, minimizing off-stage leakage, reducing gate length, increasing switching speed and designing a mixed mode circuit.

However, the cost required to perform experimental analysis and optimization of semiconductor devices using fabrication process can be very expensive especially when involving purchase of expensive electrical testing equipment. Thus, it is recommended to perform optimization and analysis using simulation. One of the best device process and simulation tool is Silvaco ATHENA & ATLAS simulation software. It provides user with various capability in process and electrical testing.

After manipulating and improving process parameters, the optimized device has recorded significant improvement over the predecessor. Optimizations include better threshold voltage extraction (0.2v), drain current rise beyond pinch off, better drain current extraction, higher switching speed at 2Ghz, better device structure after ion implantation due to tilted implantation, lower off-stage leakage current **(1.2589×10^{-12} A/um)** and minimization of junction breakdown effect.

ACKNOWLEDGEMENT

Completion of this project would not have been possible without the assistance and guidance of certain individuals. Their contribution both technically and mentally is highly appreciated.

First and most importantly, I would like to express my sincere and utmost appreciation to my project supervisor Dr John Ojur Dennis for his guidance and advice throughout the period of this project work. His patient to guide me throughout every part of project phase and commitment to ensure the best quality of report and findings from this project has enabled me to complete a very excellent final year project.

Special credit also goes to AP Dr Norani Muti Mohamad on her kindness in lending all the necessary lab equipments in order to complete this project. Thanks are extended to Mr Rosli and Mrs Noraini for their technical assistance while conducting virtual lab experiment. Their presence is really helpful and meaningful.

Also a special thanks to final year project committee in their approval and support to allow me to conduct this final year project. Process optimization of semiconductor using ATHENA & ATLAS tools is designed especially for Master Degree students. However, FYP committee has given me a precious opportunity to learn expensive software and utilize available tools.

Last but not least, I would like to thank all persons who have contributed to this project but have been inadvertently not mentioned.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND OF STUDY

The MOSFET (Metal-oxide Semiconductor Field Effect Transistor) is of paramount importance in semiconductor device physics because this device is extremely useful in the study of semiconductor surfaces. Throughout a few decades, it has been the most important device for advanced integrated circuits. It has been replacing many other semiconductor devices due to its outstanding performance in switching speed, low power consumption, more room for expansion of design and layout, as well as low gate turn-on voltage.

In this project, n-channel depletion MOSFET (NMOS) has been chosen as the core device for further optimization. Experiment has proven that NMOS performs better than PMOS due to higher drive current, higher mobility, easier to implement scaling technology and low power consumption. However, there is still room for further optimization as the technology trend for the miniaturization of NMOS and integrated devices continue to grow. Most of the optimization can be done by improving the fabrication process like improving the doping concentration through tilt angle ion implantation, selection of optimum gate oxide thickness, selection of doping material that contains maximum solubility to ensure best conductivity and reduce resistivity. Another major concern will be reduction of device size to improve switching speed and developing compact IC layout.

1.2 PROBLEM STATEMENT

The cost required to perform experimental analysis and optimization of semiconductor devices using fabrication process can be very expensive especially when involving purchase of expensive electrical testing equipment. Thus, it is recommended to perform optimization and analysis using simulation. One of the best device process and simulation tool is Silvaco ATHENA & ATLAS simulation software. It provides user with various capability in process and electrical testing.

This project has utilized ATHENA & ATLAS to perform optimization on the NMOS based on several parameters like channel length, P-well impurities concentration, appropriate drain and gate voltage, gate oxide thickness and so forth.

Most of the current NMOS has been fabricated with threshold gate voltage of 0.7V to trigger on the device. However, this threshold voltage should be minimized to utilize less power to trigger the device to ON/OFF state. Another consideration will be to fabricate a device capable of delivering as much drain current as possible and reduce power loss when switching. This includes reduction of leakage current, resistance across Vgs, gate oxide thickness, doping concentration and channel length.

1.3 OBJECTIVES

Several specific objectives have been outline to meet with the **finalization of project** device apart from general objectives set earlier. This includes:

- ✓ To have detailed and sound understanding on the device fabrication technology via VLSI especially theory with direct relevancy to NMOS fabrication process steps.

- ✓ To understand various capability of ATHENA & ATLAS. This includes perfect understanding on how to write source code, how to simulate device using given electrical testing models.
- ✓ To compare and suggest any improvement possible from the experimental work of other researchers. This involves study of international journal performing similar device optimization.
- ✓ To select best gate oxide thickness, channel doping and gate scaling combination that delivers best electrical characteristic.
- ✓ To reduce threshold voltage, improve drive current, minimize power loss, increase switching speed, minimize break down effect and test device functionality in a circuit.
- ✓ To design a mixed mode circuit (timer, inverter) using the fabricated device.
- ✓ To defend findings by including valid theoretical statements and mathematical calculations.

1.4 SCOPE OF STUDY

1.4.1 The Relevancy Of The Project

This project directly guides us to study on VLSI fabrication aspect, semiconductor theory and analogue electronics theory especially in the MOSFET application. We get to know current wafer fabrication technology and the required parameters in each fabrication steps (Example in diffusion: temperature, doping concentration, maximum solubility, and extrinsic carrier are critical parameters).

In analogue concepts, we get to know in depth the relationship between Vds, Vgs, darin current, gate voltage, PN junction, Q-point, Beta, and its respective function as an amplifier and switch. **Note** that switching capability of NMOS can be used to build a timer or inverter in ATLAS mixed-mode command.

1.4.2. Feasibility of the Project within Scope and Time Frame

Throughout the second half of the semester, various optimization like breakdown voltage, leakage current, gate length reduction, switching speed optimization, and advance fabrication study like rapid thermal annealing, control doping and gate oxide thickness have been studied.

Some optimization on the concentration doping level of P-well, gate oxide thickness, which affects the Vgs threshold voltage, has also been done. This has enabled the shifting of on-gate voltage from 0.7V to approximately 0.2V. Optimization was performed by taking a series of data and obtaining simulated output. This minimization of threshold voltage enables the device to be triggered by using less power. Further discussion will be carried out in **Results and Discussion Chapter**.

CHAPTER 2

LITERATURE REVIEW AND THEORY

This project concentrates on simulating and optimizing NMOS based on existing theory and findings in journals, comparing and suggesting better steps out of the existing optimizations. This section will cover all relevant theories behind the simulation aspect, facts and data to support all the findings in the next chapter, results and discussion. Basically, the following concepts and theories are addressed:

- Typical NMOS and its optimization points
- Oxidation process and its relationship to gate oxide thickness
- Relationship between gate oxide thickness and off-state leakage current.
- Concept for reducing gate length and its advantages.
- Relationship between threshold voltage and channel doping.
- Ion Implantation: Tilt Angle
- Total device resistance calculation.

2.1 NMOS OPTIMISATION CONCERN

The optimization of NMOS has been performed extensively in all areas of concern including threshold voltage reduction, off-state leakage control, switching speed, low power consumption, tunneling effect minimization, gate scaling and drive current improvement. In general, most of the optimization concentrates on variation of gate oxide thickness, channel doping concentration, total internal resistance, channel length and substrate thickness. Figure 2.1 shows optimization points in a typical NMOS structure.

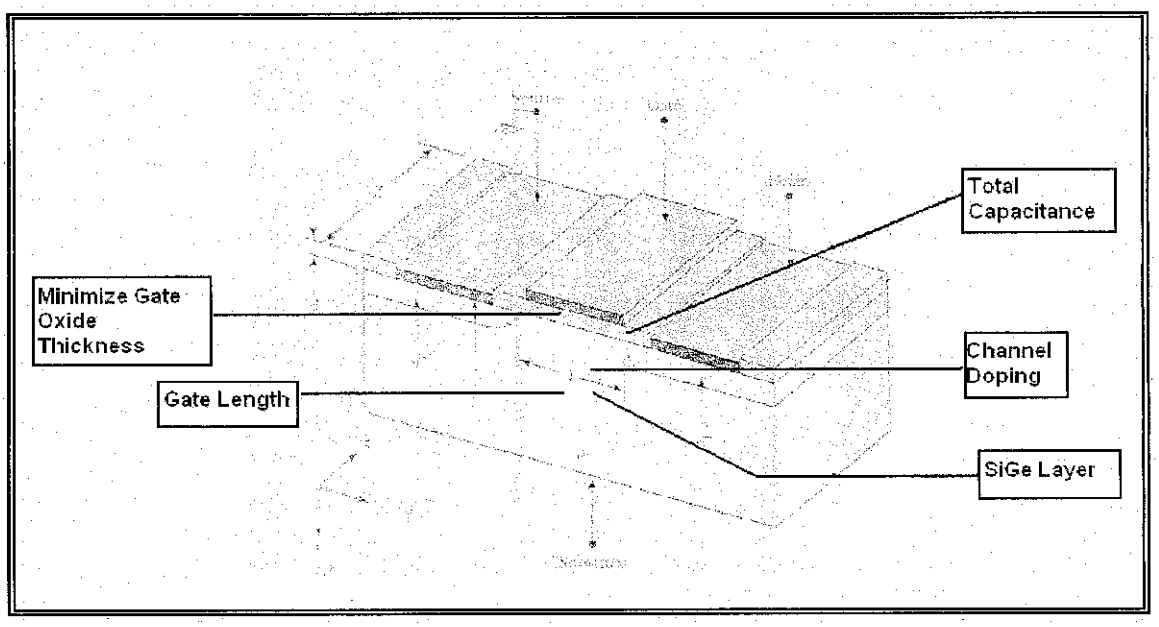


Figure 2.1: Optimization Points in a Typical NMOS

2.2 OXIDATION PROCESS

Oxidation has been termed as the ability of a silicon surface to form silicon dioxide. In general term, silicon dioxide has been used in the formation of window glass, but the purer and higher quality of silicon dioxide has been used in producing dielectric layer in semiconductor field. This dielectric layer has various thicknesses that serve different functions at different active regions. Table 2.1 shows the silicon dioxide thickness for various applications. Notice that Gate Oxide thickness is relatively thin compared to other oxide regions like field oxide and masking oxide. Gate oxide thickness affects a lot of electrical properties like threshold voltage reduction, off-state leakage and tunneling effect.

Table 2.1 Silicon Dioxide Thickness and Its Application

Silicon Dioxide Thickness, A	Application
60 –100	Tunneling Gates
100 – 500 (typical)	GateOxides,Capacitor dielectrics
200 – 500	LOCOS Pad Oxides
2000 – 5000	Masking Oxides
3000 - 10000	Field Oxides

In the silicon oxidation process, we have to consider the concentration of oxidation, diffusion, tube furnace, heat treatment and chemical vapor deposition process. As the thickness grows, the linear growth with time decays to parabolic form due to transport-limited reaction and diffusion-limited reaction. The linear growth of oxide layer follows the equation 2.1 while parabolic form follows equation 2.2 [3, 8, 10]

$$X = \frac{B}{A}t \tag{2.1}$$

$$X = (Bt)^{0.5} \tag{2.2}$$

The X parameter stands for oxide thickness, B represents parabolic rate constant, $\frac{B}{A}$ represents linear rate constant and t stands for oxidation rate. Even though silicon dioxide is grown by performing oxidation onto silicon surface, the growth rate is slightly different from normal oxidation growth rate. Equation 2.3 shows silicon dioxide growth rate.

$$R = \frac{X^2}{t} \tag{2.3}$$

R stands for silicon dioxide growth rate, X is the expected oxide thickness to grow on silicon surface and t is the oxidation time.

2.3 RELATIONSHIP BETWEEN LEAKAGE CURRENT AND GATE OXIDE

Gate oxide thickness has reverse relationship with threshold voltage reduction. The gate oxide thickness is a reverse proportion to the gate capacitance. With the gate oxide thickness increasing, the gate oxide capacitance goes down, which means that the gate has less control on the channel and threshold voltage will increase [1,4]. Thus, making thinner gate oxide will reduce the **overall threshold voltage significantly**. However, this

will lead to another problem of off-state leakage. As proven, lowering the threshold voltage will lead to increment of leakage current.

As the thickness of the dielectric material decreases, direct tunneling of carriers through the potential barrier can occur. Tunneling is caused by carriers penetrating through SiO_2 when electric field is sufficiently high enough to drift the electrons or holes. Because of the differences in height of barriers for electrons and holes, and because holes have a much lower tunneling probability in oxide than electrons, the tunneling leakage limit will be reached earlier for NMOS than PMOS devices. The SiO_2 thickness limit will be reached approximately when the gate to channel tunneling current becomes equal to the off-state source to drain sub-threshold leakage (currently ~1nA/mm) [2, 11]. Figure 2.2 shows tunneling effect due to thin SiO_2.

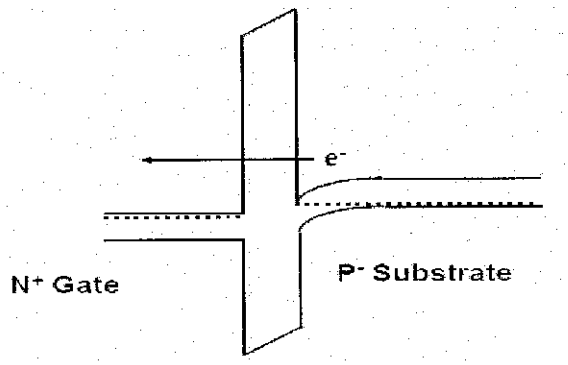


Figure 2.2: Direct tunneling leakage mechanism for thin SiO_2

2.4 LEAKAGE MECHANISM

The following are some of the leakage mechanisms that are of concern in this project:

Subthreshold leakage in MOS transistors, which occurs when the gate voltage is below the threshold voltage and mainly consists of diffusion current. Off-state leakage in present-day devices is usually dominated by this type of leakage. Shorter channel length results in lower threshold voltages and increases subthreshold leakage. As temperature

increases, subthreshold leakage is also increased. On the other hand, when the well-to-source junction of a MOSFET is reverse-biased, there is a body effect that increases the threshold voltage and decreases subthreshold leakage.

Gate oxide tunneling of electrons that can result in leakage when there is a high electric field across a thin gate oxide layer. Electrons may tunnel into the conduction band of the oxide layer; this is called Fowler-Nordheim tunneling. In oxide layers less than 3–4 nm thick, there can also be direct tunneling through the silicon oxide layer. Mechanisms for direct tunneling include electron tunneling in the conduction band, electron tunneling in the valence band, and hole tunneling in the valence band.

Punchthrough leakage, which occurs when there is decreased separation between depletion regions at the drain-substrate and the source-substrate junctions. This occurs in short-channel devices, where this separation is relatively small. Increased reverse bias across the junctions further decreases the separation. When the depletion regions merge, majority carriers in the source enter into the substrate and get collected by the drain, and punchthrough takes place [5,6].

2.5 CHANNEL DOPING VERSUS THRESHOLD VOLTAGE

Channel doping affects Fermi potential directly. With the channel doping concentration increasing, the Fermi potential increases. Fermi potential is the energy at which the probability of occupation by an electron is exactly one-half. Also with the channel doping increasing, more effort is needed to invert the channel. Therefore, with higher channel doping, higher threshold voltage is formed [1, 4].

Threshold voltage can be further improved from the process of channel doping through halo implant. The short channel behavior of both NMOS and PMOS transistors was further enhanced by the introduction of halo implants. The halo implant is a high-angle implant. Since the halo implant uses a high angle it must be done in four 90-degree

rotations in the implant tool to ensure both sides of the channel are doped and that transistors oriented in both X and Y directions get doped.

2.6 REDUCING GATE LENGTH

Switching speed of a typical NMOS has been controlled by the total capacitance available. Since time constant, τ ,is related to the total resistance, R, and capacitance, C, by the expression $\tau = RC$, increasing the device speed can be achieved by minimizing its resistive and capacitive components [3]. Here, the approach is to increase the switching speed by reducing capacitance. The capacitance has direct relationship with area which is **width multiplied by length**:

$$C_{area} = L.W.C_1 \tag{2.4}$$

L is the device length, W is the device width, C_1 stands for device dielectric constant. As the actual dimension of finished devices might be slightly larger or slightly smaller than the expected length, a variation is introduced on the length and width. Equation 2.4 is complicated by addition of δ to improve capacitance value accuracy and is shown in equation 2.5.

$$C_{area} = (L + \delta) \times (W + \delta) \times C_1 \tag{2.5}$$

It is know that, **width of device** cannot be simply changed since it affects the total resistance and device properties. We do not want to complicate device optimization. Thus, minimizing length by reducing gate length is the best solution.

2.6.1 Periphery capacitance

Periphery capacitance, which is also called fringing capacitance, exist at the poly-silicon side of the device. The expression for the periphery capacitance is given by:

$$C_{periphery} = [\,2\,(l + \delta l) + 2(w + \delta w)].C_2 \qquad (2.6)$$

C_2 is the dielectric constant obtained by referring to the material used to build poly-silicon layer. Figure 2.3 shows the location of the periphery capacitance in an NMOS device.

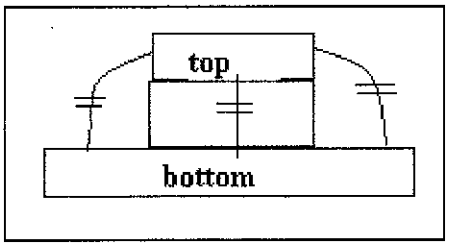


Figure 2.3: Fringing capacitance sneaking out the edges [2]

2.6.2 Parasitic capacitance

N well and the P substrate underneath form more parallel plates, effectively creating another capacitance below the N well between the N and the P. This PN junction is the dielectric barrier. However, the capacitance recorded parasitic capacitance is very small and it has always been ignored when calculating total capacitance of a device. Normally, industries try to remove parasitic capacitance within fabricated device. Figure 2.4 shows parasitic capacitance layout in NMOS.

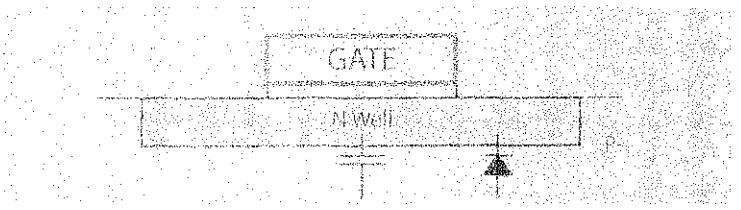


Figure 2.4: Parasitic Capacitance

Thus total capacitance must take into consideration area capacitance and periphery capacitance. To be exact:

$$C = [(L + \delta) \times (W + \delta) \,.\, C_1] \quad + [2\,(l + \delta l) + 2(w + \delta w)].C_2 \qquad (2.7)$$

2.7 CHANNEL DOPING, GATE OXIDE AND CHANNEL LENGTH

The important principle in MOSFET scaling is that channel length and gate oxide thickness must decrease together. Scaling one without the other does not yield adequate performance improvement [7]. Experiment shows that gate oxide thickness and channel length must be scaled together to achieve adequate performance. Normally, for a submicron device gate length of less than 0.5 micron, the gate oxide thickness featuring silicon dioxide should be fabricated well below 10 nm. Normally, scaling of gate oxide thickness must take into consideration numerous factors like leakage current, breakdown voltage and punch through effect. Thus, thicker oxide might bring performance degradation in one factor but improve other parameters. Minimal gate oxide might encourage tunneling effect unless better gate material is used like silicon nitride. However, use of silicon nitride in fabrication is far more costly than conventionally growing oxide in silicon.

2.8 ION IMPLANTATION PROCESS ADVANTAGE

In normal diffusion we encounter lateral diffusion. Thus, designer must leave enough room between adjacent regions to prevent the laterally diffused regions from touching and shorting. This greatly hampers the commitment of fabricating smaller device. Normal diffusion will require high temperature which of course will damage the single crystal due to dislocation. This dislocation will cause leakage as well. Furthermore, one ultimate objective of an advanced process is to decrease thermal effect. Thus, introduction of impurities to particular sensitive region like channel doping and poly-silicon must be

performed via ion implantation which can be operated under relatively less thermal temperature and smaller device size.

From figure 2.5, it can be seen that the maximum solubility of phosphorus, arsenic and boron was near 10^{21} cm^3. High concentration of impurities in the intrinsic semiconductor will reduce the resistivity of a device significantly. However, high channel doping will cause right shift or increment of threshold voltage. High channel doping will cause increment of Fermi potential and depletion charge. This will require more energy or threshold voltage to invert the channel. Thus, minimum doping concentration might affect channel conductivity but encourage reduction of threshold voltage.

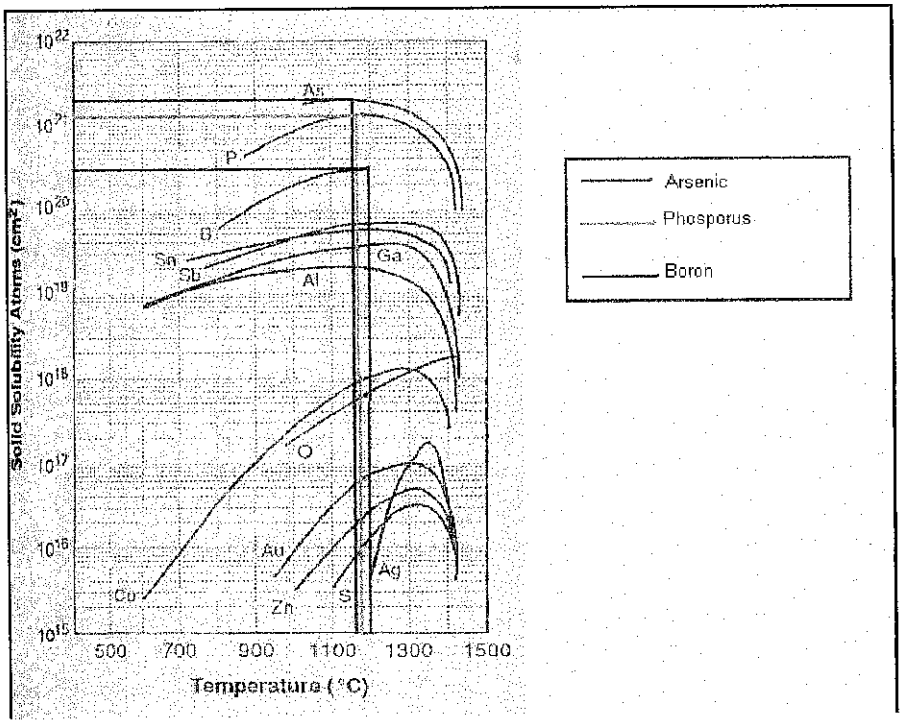


Figure 2.5: Maximum solubility levels for various dopants in silicon

Gate regions of NMOS must be doped below 10^{15} atoms/cm^3 to produce ultra-thin junctions. However, this is hardly built using normal diffusion steps. Scaling down the device length to 0.18 micron will require 40 nm range of junction which is almost impossible to get done using diffusion. Ion implantation overcomes these problems since

the process can be achieved at lower temperatures as well as enabling greater control of dopants and number of dopants. Ion implantation use bombardment technology to penetrate into the surface wafer, thus removing the lateral effect allowing us to build a smaller device.

2.8.1 Tilt Angle Ion Implantation

The channeling effect causes some ions to penetrate deeper into the single-crystal substrate. This can form a "tail" on the normal dopant distribution curve. It is an undesirable dopant profile, which could affect microelectronic device performance. Therefore several methods have been used to minimize this effect.

One way to minimize the channeling effect is ion implantation on a tilted wafer, typically with a tilt angle of 7 degrees. By tilting the wafer, the ions impact with the wafer at an angle and cannot reach the channel. The incident ions will have nuclear collisions right away and effectively reduce channeling effect.

Tilting the wafer can cause a shadowing effect by the Photo resist. This can be solved by rotating the wafer while performing ion implantation. Normally, rapid thermal annealing is performed in a furnace consisting of dopant impurities right after ion implantation.

Another way to solve channeling effect is to diffuse a layer of thin silicon dioxide. Thermally grown silicon dioxide is an amorphous material. The passing implantation ions collide and scatter silicon and oxygen atoms in the screen layer before they enter the single-crystal silicon substrate.

2.8.2 Ion Implantation Energy

Energetic ions penetrate the target, gradually lose their energy through collision with the atoms in the substrate and eventually rest inside the substrate. Figure 2.6 shows ion trajectory and projected range.

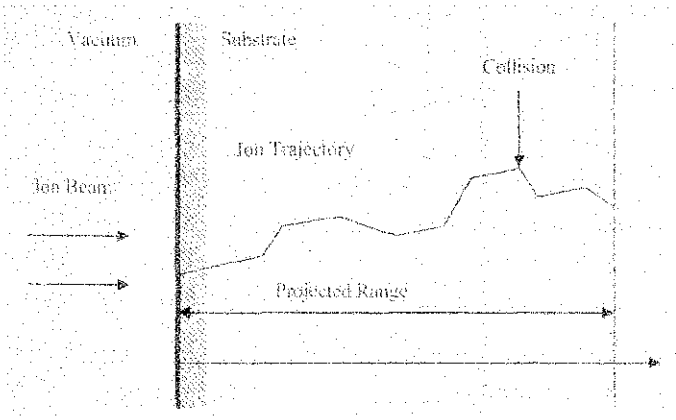


Figure 2.6: Ion trajectory and projected range

Generally, the higher the ion energy, the deeper it can penetrate into the substrate. However, even with the same implantation energy, ions do not stop exactly at the same depth in the substrate, because each ion has different collisions with different atoms.

Higher-energy ion beam can penetrate deeper into substrate, and therefore have a longer projected ion range. Since smaller ions have smaller collision cross sections, smaller ions at the same energy can penetrate deeper into substrate and the mask materials.

Projected ion range is an important parameter for ion implantation, because it indicates the ion energy needed for certain dopant junction depth. It also gives information on the required implantation barrier thickness for ion implantation process. 100keV is the best recommend implantation energy to deal with device having 0.1 to 1.0 micron depth [5]. Figure 2.7 shows projected range of dopant ions in silicon.

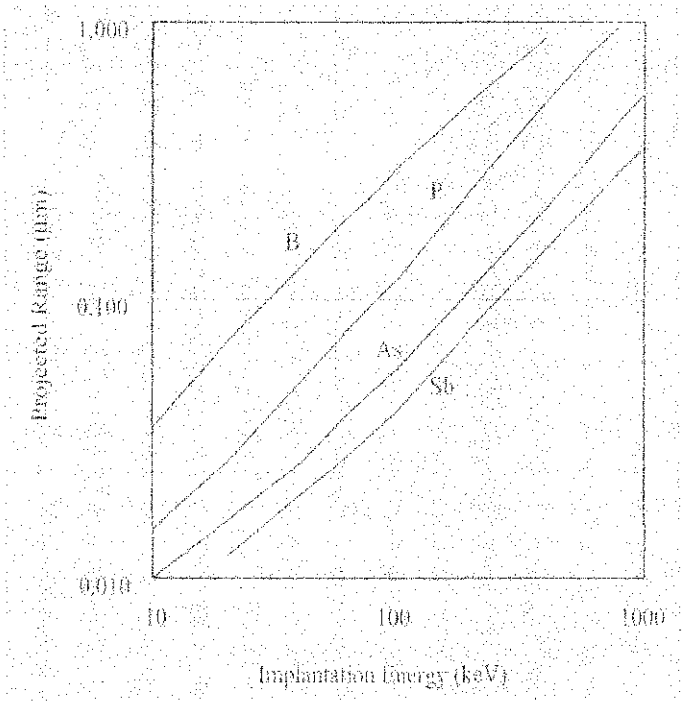


Figure 2.7: Projected Range of Dopant Ions in Silicon

2.9 TOTAL INTERNAL RESISTANCE

The total resistance in a MOSFET can be categorized into three major parts as shown in figure 2.8 [6]. Equation 2.8 gives the expression for total internal resistance calculation for a typical NMOS structure.

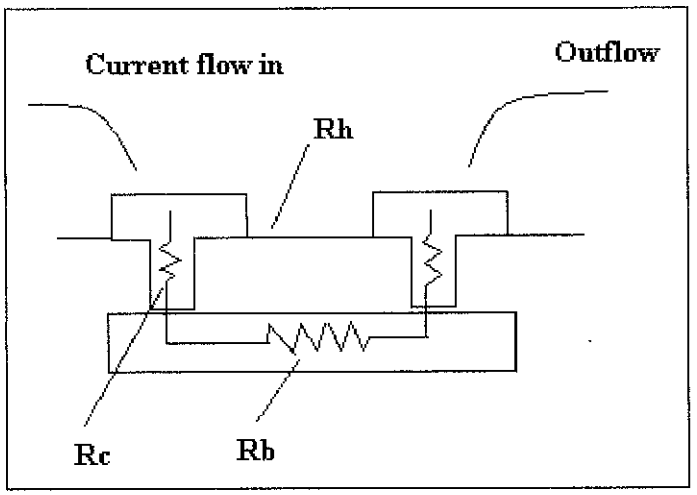


Figure 2.8: Total Resistance in a Device Structure

$$R = Rb + Rh + Rc \tag{2.8}$$

$$R = \frac{Lb}{Wb} Pb + 2\frac{Lh}{Wh} Ph + 2\frac{Rc}{Wc} \tag{2.9}$$

$$R = \frac{Lb + \delta Lb}{Wb + \delta Wb} Pb + 2\frac{Lh + \delta Lh}{Wh + \delta Wh} Ph + 2\frac{Rc}{Wc + \delta Wc} \tag{2.10}$$

R is the total resistance, Lb and Wb is the length and width of device body, Lh and Wh is the length and width of device head, Pb and Ph is the sheet resistivity of device body and head, Rc is the resistance factor of the contact and Wc is the width of contact.

2.10 SEMICONDUCTOR PROPERTIES

2.10.1 Carrier Density

When perform doping, we have to follow following formula guide:

$$n = n_i \exp\left(\frac{E_f - E_i}{kT}\right) \tag{2.11}$$

$$p = n_i \exp\left(\frac{E_i - E_f}{kT}\right) \tag{2.12}$$

Where *ni* is the intrinsic concentration of semiconductor, E_f is the Fermi potential, E_i is the intrinsic energy potential, k is the Boltzmann constant and T is the operating temperature in Kelvin.

If n >p for Ef > Ei, then the semiconductor is the n-type and

If p > n for Ef < Ei, then it is definitely p type.

2.10.2 Build –in Voltage

Because a voltage difference is formed, an energy difference exist between them. Thus an energy hill is formed across the depletion region. Consequently, the energy bands are bent and Fermi levels are aligned.

$$|Vbi| = \frac{kT}{q} In \frac{NaNd}{ni^2} \tag{2.13}$$

Where V_{bi} is the built in voltage, k is the boltzmann constant, q is the charge value in Coulomb, Na is the acceptor concentration, Nd is the donor concentration and ni is the intrinsic concentration.

Figure 2.9 shows built in voltage in N-region. No built in voltage can occur in P-region.

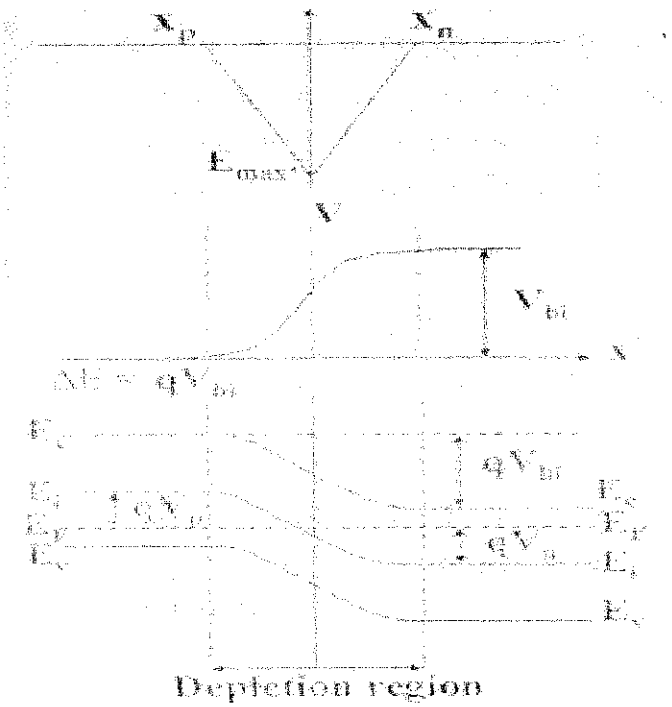


Figure 2.9: Massive Built In Voltage in N-Region

2.10.3 Threshold Voltage Calculations

The analysis provided here is for NMOS, with its extension to PMOS device being straightforward. The threshold voltage of an n-channel MOSFET is classically given by [9]:

$$Vth = \Phi_{MS} - \frac{\Phi ss}{\Phi ox} + 2\Phi_F + \frac{qN_a x_{d\max}}{C_{ox}} \tag{2.14}$$

Where, Φ_{MS} is the work function between the gate and the channel and equal to Φ_m – ($\Phi_{SI} - \Phi_F$). Q_{ss} is the surface state charge of the channel. C_{ox} is the gate capacitance and is equal to

$$\frac{\varepsilon_{ox}\varepsilon_0}{t_{0x}} \tag{2.15}$$

t_{ox} is the gate oxide thickness and $\varepsilon_{ox}\varepsilon_0$ is the permeability constant . Φ_F is the Fermi potential is given by

$$\Phi_F = \frac{kT}{q} Ln\left[\frac{Na}{ni}\right] \tag{2.16}$$

From the threshold voltage equation, it is observed that there are several factors that control the threshold voltage. The first one is the channel doping. The channel doping effects the Fermi potential Φ_F directly. With the channel doping increasing, the Fermi potential increases. Also with the channel doping concentration increasing, the depletion charge in the channel also increases. It is to be noted that when channel doping is increasing, more effort is needed to invert the channel. Therefore, with adjusting the channel doping, different threshold voltages can be achieved. In normal technology, the ion implantation can increase or decrease the channel doping. This is a very effective way to adjust the threshold voltage in CMOS technology.

The second factor is the gate oxide thickness. The gate oxide thickness is in reverse proportion to the gate capacitance. With the gate oxide thickness increasing, the gate oxide capacitance goes down, which means that the gate has less control on the channel and threshold voltage will increase.

2.11 ANALYSIS ON DEPLETION LAYER & SATURATION POINT

This saturation point will guide us to select desired Vgs and Drain voltage.

2.11.1 Linear region:

$$Vgs > V_T > 0$$
$$0 < Vds < Vgs - V_T \tag{2.17}$$

The drain current increases with increasing Vds for a constant Vgs. However, Vgs shouldn't be so large that it destroys the MOSFET itself. Figure 4.11 shows NMOS inversion layer build up when switched on in linear region.

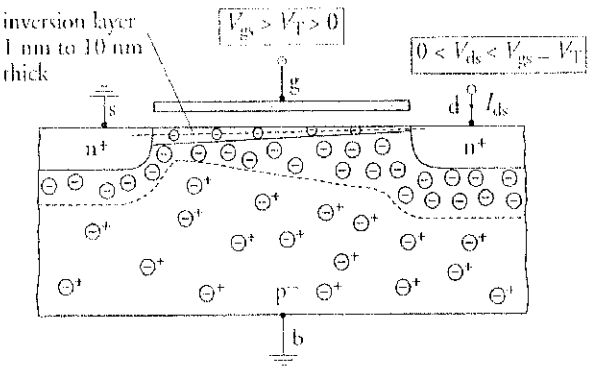


Figure 4.11: Linear Region

2.11.2 The Transition Region

An increase in Vds with Vgs constant decreases the voltage difference between the gate and channel. The inversion layer disappears when Vgs = V_T. This tells us that Ids will not increase anymore if Vds is equal to the VT. We can view and study the characteristic of junction voltage through junction gate extraction. Figure 4.12 shows transition region in a NMOS structure.

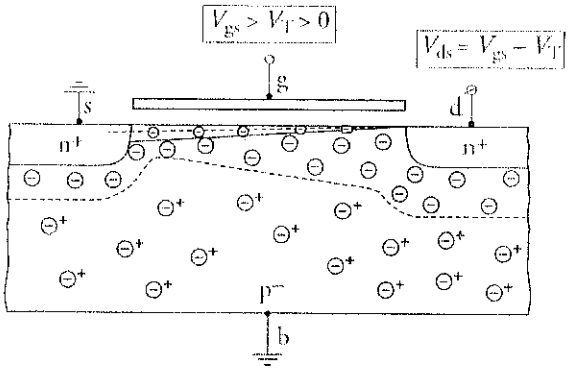


Figure 4.12: Transition region

2.11.3 The Saturation Region

The channel end no longer coincides with the drain when Vds is larger than Vgs- V_T. The current Ids increases to the saturation when Vds = Vgs – V_T. Thus, the point is Id wont increase after Vds > Vgs – Vt

Main point Vds should less than Vgs – V_T , or best at Vds = Vgs – V_T . In order to tap more Vds, we can improve Vgs. Figure 4.13 shows saturated region.

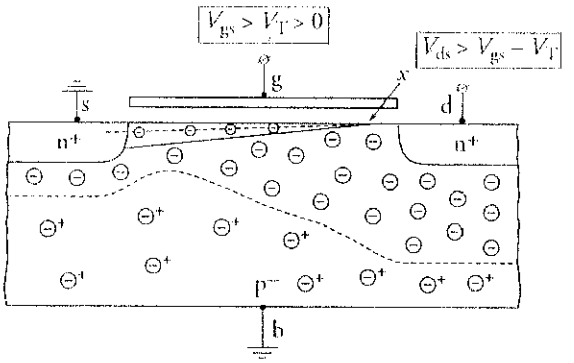


Figure 4.13: Saturated region

CHAPTER 3

PROJECT OVERWIEW/METHODOLOGY/ PROJECT WORK

3.1 PROCEDURE IDENTIFICATION

This section will describe the procedure and methods used to reach stated objectives which include reducing gate length, reducing power loss, reducing off-stage leakage, improving drive current and verifying circuit testing of an inverter using the optimized device.

3.1.1 Literature Review and Device Identification

Before starting to simulate a device, detailed understanding of the fabrication and semiconductor characteristics which include in depth understanding of crystal growth, wafer preparation, fabrication theory (Photolithography, Oxidation, Deposition, Doping, ion implantation, diffusion, chemical etching and so forth), is required.

First, information is gathered and analyzed in order to choose a device to develop on. This device must meet certain requirements like industry demand, future design requirement, currently still in the optimization stage and has large scale utilization in wafer technology. Here, NMOS is selected since it is part of the CMOS structure. CMOS structure is widely used in fabrication industry typically used in the design of chipsets, microprocessors, memory, flash memory, digital counters, switches and many more. Even though industry has claimed to reach the minimum possible device size (90nm) [1], there is still room for optimization for bigger device size.

3.1.2 Understanding Optimization Point

Before optimizing any device, identifying the optimization point is vital. Any steps taken to modify the existing structure or properties must bring significant effect on its electrical characteristics. Thus, considerable amount of study must be carried out. For instances, optimization of NMOS must bring significant impact when performing electrical testing like Id –Vgs Curves, Sub-Threshold Slope Extraction, breakdown voltage extraction, drain current, transient response, RF parameters and so forth.

Detailed study of semiconductor properties like Fermi levels in semiconductor, band-structure of semiconductor, carriers' properties in extrinsic semiconductor, P-N junction, crystal growth and dielectric,and fabrication technology is required. This will provide the basis required to perform device fabrication using ATHENA and simulate the electrical characteristic using ATLAS.

From the study, it is observed that the major optimization points of NMOS will be channel doping, channel length, gate oxide thickness and ion implantation tilted angle. Figure 3.1 shows optimization points of NMOS described and labeled in the structure.

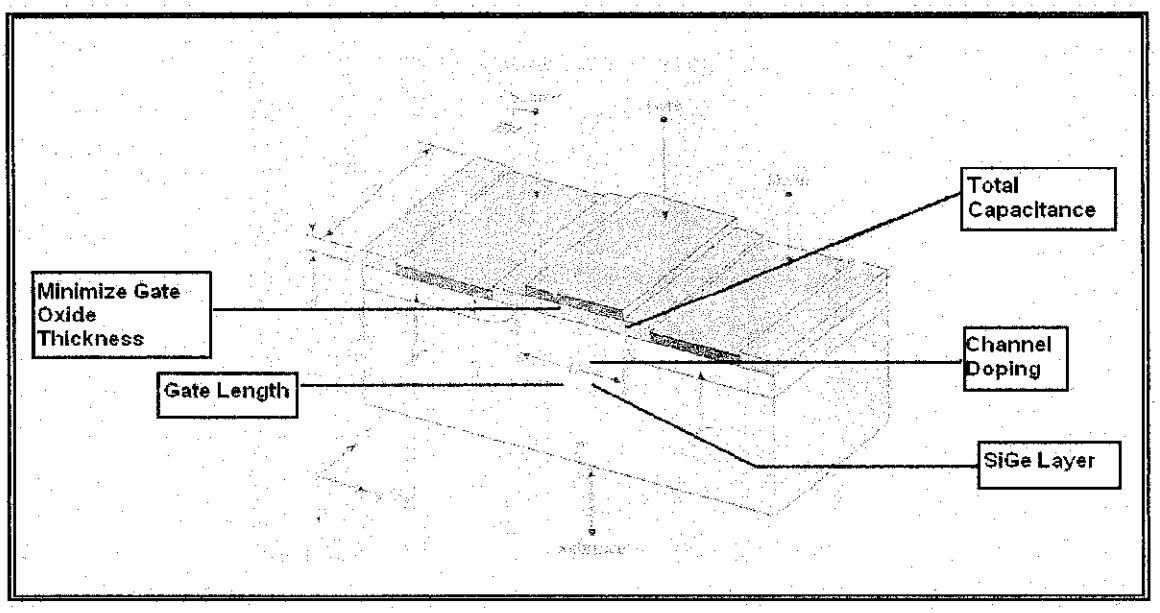


Figure 3.1: Optimization Points of a Typical NMOS Structure

3.1.3 Device Fabrication

Before any optimization can take place, a working prototype is a must. Thus, the first step of this project is to develop a rough NMOS structure to optimize on. Figure 3.2 shows a simplified NMOS fabrication procedure. It only describes a few important steps necessary to fabricate a NMOS.

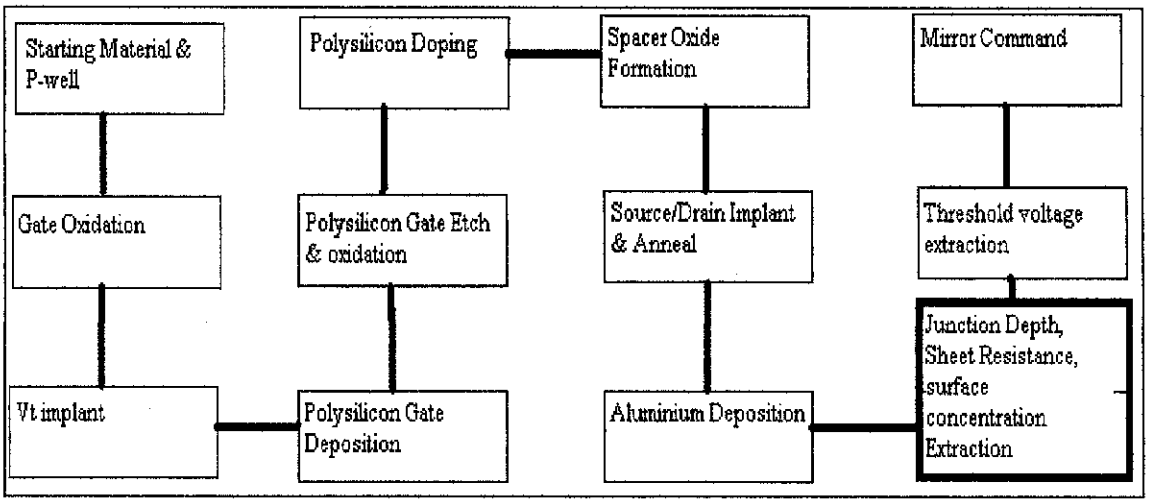


Figure 3.2: Simplified NMOS Fabrication Steps

Since ATHENA is a physical experimental simulation software, steps performed to fabricate a device is very similar to the real industry practice. It starts from selection of wafer type to deposition of metal contact.

I. **Mesh definition** – To specify initial x and y location in micron and spacing of the device to be simulated on wafer. User is able to view the resulting grid of the set parameters.
II. **Initial substrate** – In this command menu, user is required to key in semiconductor properties to be used in wafer preparation including types of semiconductor (silicon or germanium), orientation of the crystallized semiconductor, types of impurities introduced, concentration of doping material and dimensionality.

III. **Ion Implantation** – Which includes specifying impurity, dose or concentration in ions/cm^2 , energy of implantation, tilt angle and rotation angle. We also have to specify implantation models to suit with our design like Gauss model, Dual Pearson, Full Lateral, Monte Carlo etc.

IV. **Oxidation and Diffusion** –After implantation, it is required to perform diffusion to move the dopant into substrate and to repair damage.

V. In the diffusion command, oxidation model such as vertical, compress and viscous is specified. Next, types of diffusion model like Fermi, two.dim and full.cpl are specified. Later, we need to key in diffusion parameters including time and temperature of diffusion, chemical used and gas pressure.

VI. **Simple Geometrical Etching** – To completely remove resulting oxide after multi-stage diffusion.

VII. Gate Oxidation – In this command, Gate Oxide thickness, temperature and pressure optimizer are specified. In order to obtain the exact gate oxide thickness, an optimizer window is used to change the entire oxidation parameters that were previously set **to suit with very accurate oxide thickness.**

VIII. Threshold Voltage Adjust Implant – series of implantation that allows us to adjust threshold voltage.

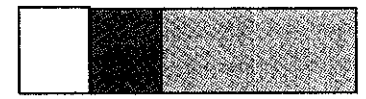
IX. **Polysilicon** Gate Deposition, Polysilicon gate pattern, Polysilicon gate oxidation – aims to grow oxide on top of the Polysilicon gate, poly silicon gate doping.

X. Spacer Oxide Deposition -> Spacer Oxide Etch

XI. **Source/Drain Implant:** This command is utilized to build source and drain gate of the NMOS. In this command, the impurities in the source/drain is defined, In other words it select the concentration of impurities and the implantation model to be used and the material type (amorphous or crystalline).

XII. **Source/Drain Anneal** is used to remove oxidation from implantation, which is similar to the Oxidation/Diffusion steps.

XIII. **Aluminum deposition -> Aluminum etching.** To deposit a thin layer of aluminum on both source and drain. This is done to initiate metal oxide junction.



metal oxide semiconducotr

This architecture is metal oxide semiconductor, very useful in integrated chipset, and construction of circuitry like timer.

XIV. Extraction command is performed as the follows:

- **Junction depth Extraction**
- **Sheet Resistance Extraction**
- **Surface Concentration Extraction**
- **Threshold Voltage Extraction**

XV. Finally, the mirror command is invoked to get a complete NMOS gate. The purpose of mirror command is to save processing and rendering time when simulating a process.

3.1.4 Performing Optimization

This optimization is done through trial and error as well as on theoretical basis. Few analogue parameters have been optimized and the results are compared with the previous given syntax.

The optimization has been subsequently categorized into two subsequent categories. First, optimization is done on the existing 0.5 micron gate length structure by changing extrinsic semiconductor properties and re-meshing existing structure. These are performed mainly to reduce the overall threshold voltage while minimizing leakage current.

Second stage of the optimization will be to reduce the channel length to 0.3 micron while retaining the previous optimized structure. In other words, this second stage will allow us to obtain a smaller gate length device, faster switching and smaller threshold voltage. All

the optimization structure will be retest with analogue parameters like breakdown voltage extraction, drain current and Id/Vgs curve.

3.1.5 Finalizing Procedure

This part of the project will finalize all parameters used in the device fabrication ranging from fabrication process to material used. This will start with drawing out conclusion parameters that bring to the similar outcome. Example, to minimize threshold voltage, channel doping, gate oxide thickness and channel length must be optimized together. All fabrication aspect like ion implantation tilt angle, optimizer used and oxidation rate and temperature are recorded. Finally, clear steps to fabricate the device with specific parameters and process steps are written.

3.1.6 Mixed Mode Command

Mixed Mode Circuit will be the last part of the project work before minor optimization and advance theoretical studying are conducted. Mixed mode is a circuit simulator that can include elements simulated using device simulation, as well as compact circuit models. It combines different levels of abstraction to simulate small circuits. Mixed mode uses advanced numerical analyses that are efficient and robust for DC, transient, small signal AC and small signal network analysis. Mixed mode can include up to 100 nodes, 300 elements and up to ten numerical simulated ATLAS devices.

3.2 IDENTIFICATION OF REQUIRED APPARATUS/TOOLS

3.2.1 ATHENA Process Simulation

ATHENA Process Simulation Framework enables process and integration engineers to develop and optimize semiconductor manufacturing processes. ATHENA provides an easy to use, modular, and extensible platform for simulating ion implantation, diffusion, etching, deposition, lithography and oxidation of semiconductor materials. It replaces costly wafer experiments with simulations to deliver shorter development cycles and higher yields.

Key Features [10]

1. Fast and accurate simulation of all critical fabrication steps used in CMOS, bipolar, SiGe/SiGeC, SiC, SOI, optoelectronic, and power device technologies
2. Accurately predicts geometry, dopant distributions, and stresses in the device structure
3. Easy to use software and integrates plotting capabilities, automatic mesh generation, graphical input of process steps, and easy import of legacy TMA process decks
4. Enables foundries and fab-less companies to optimize semiconductor processes for the right combination of speed, yield, breakdown, leakage current, and reliability

Deckbuild

The interactive runtime environment is the central environment for interactively using process and device simulators. It provides many important capabilities. A command interface for input deck allows user to manipulate syntax and develop a very detailed process simulation steps. However, user can opt for graphical window interface with various parameters to avoid simulator-specific input syntax. When specification is complete, DECKBUILD automatically produces a syntactically correct input deck. Decks

can be edited by user at any time. Multiple decks are produced if input parameters are looped and parameters can be extracted from calculated results.

Tonyplot

TONYPLOT (version 2) is a graphical post processing tool for use with all Silvaco simulators, and is an integral part of the VWF INTERACTIVE TOOLS. It can operate stand-alone, or along with other VWF INTERACTIVE TOOLS such as DECKBUILD and VWF.

TONYPLOT may be used to examine several data files all at once, each in its own plot window. These plot windows can be combined, effectively "overlaying" the data sets so that direct comparisons can be made. Plots can be interactively added, deleted and duplicated, overlaid and separated. Not only does TONYPLOT allow the user to display any data file produced by Silvaco tools, but it also provides extensive "tools" for examining these plots and the associated data. For example, it is possible to take cut-line slices through 2D structures, or to integrate a curve to calculate area, or even perform simple electrical simulations on 1D devices.

TONYPLOT allows plots to be rescaled, zoomed and panned. Grids can be added, axes customized, andarbitrary labels drawn on the data. All titles, marks, labels, ranges and so on are automatically set to useful defaults but can all be explicitly set whenever necessary. The appearance of all plots in TonyPlot can be totally customized, and there are many "properties" that can be tailored to suit either a certain user, or the requirements of a particular set of data. Figure 3.3 shows Tonyplot interface and figure 3.4 shows cut-line slices through 2D structure.

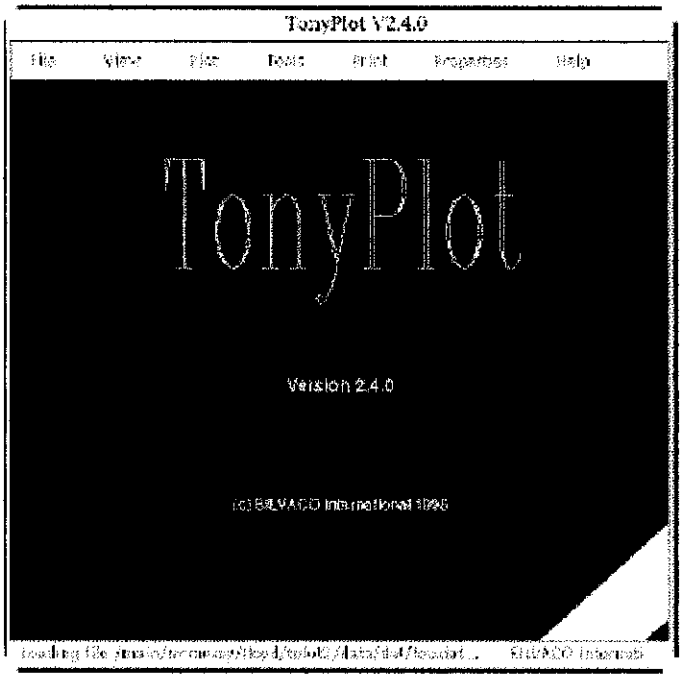


Figure 3.3: Tonyplot Interface

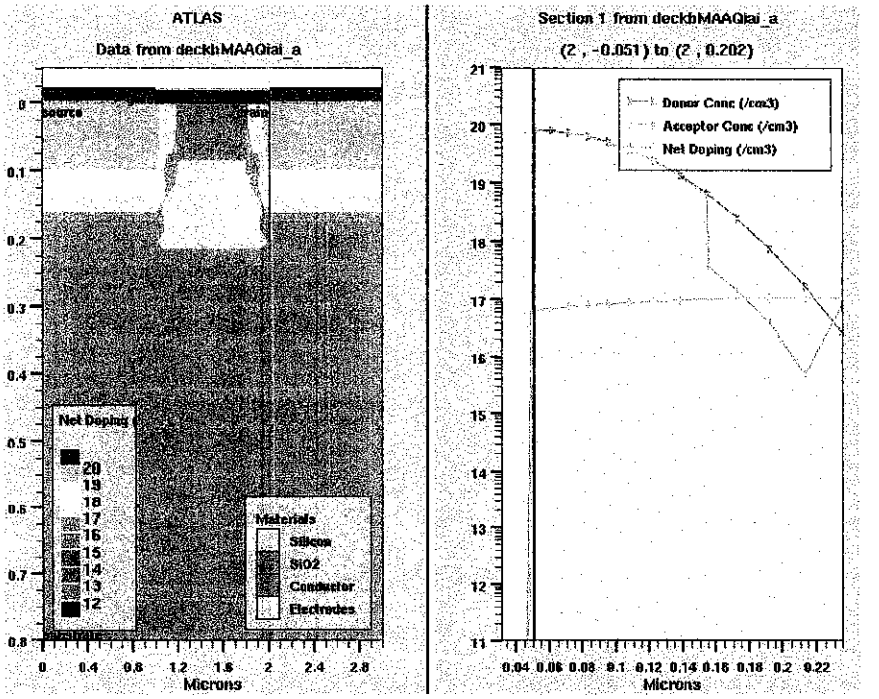


Figure 3.4: Cut-line Slices Through 2D Structure

3.2.2 ATLAS Device Simulation

ATLAS Device Simulation Framework enables device technology engineers to simulate the electrical, optical, and thermal behavior of semiconductor devices. ATLAS provides a physics-based, easy to use, modular, and extensible platform to analyze DC, AC, and time domain responses for all semiconductor based technologies in 2 and 3 dimensions.

Key Features

1. Accurately characterize physics-based devices for electrical, optical, and thermal performance without costly split-lot experiments
2. Solve yield and process variation problems for optimal combination of speed, power, density, breakdown, leakage, luminosity, or reliability
3. Fully integrated with ATHENA process simulation software, comprehensive visualization package, extensive database of examples, and simple device entry
4. Selection of raw material from the largest selection of silicon, III-V, II-VI, IV-IV, or polymer/organic technologies including CMOS, bipolar, high voltage power device, VCSEL, TFT, optoelectronic, LASER, LED, CCD, sensor, fuse, NVM, ferro-electric, SOI, Fin-FET, HEMT, and HBT

3.2.3 Dev-Edit

DEVEDIT is a device structure editor. It can be used to generate a new mesh on an existing structure, modify a device or create a device from scratch. These devices can then be used by Silvaco 2-D and 3-D simulators. DEVEDIT can be used through a Graphical User Interface (GUI) or as a simulator under DECKBUILD.

Dev-Edit can re-mesh a device structure between process simulation and device test simulations, when the process simulator does not create a good grid for the device simulator. It can re-mesh a device structure during a process or device simulation, when the mesh is no longer adequate for the next simulation step.

CHAPTER 4

RESULTS AND DISCUSSION

(SYSTEM DESCRIPTION/ FUNCTIONALITY/SYSTEM DESIGN)

4.1 ATHENA OUTPUT STRUCTURE

Figure 4.1 shows the final output of the fabricated NMOS on which some optimization has been performed. Optimization has been performed to improve and compare with initial sampled NMOS structure given in Silvaco IC MIRCOSYSTEM June 2003 booklet. The whole lists of optimization values compared with existing figures are shown in table 4.1. However, justification over the changes of optimized parameters will be discussed in the following sections.

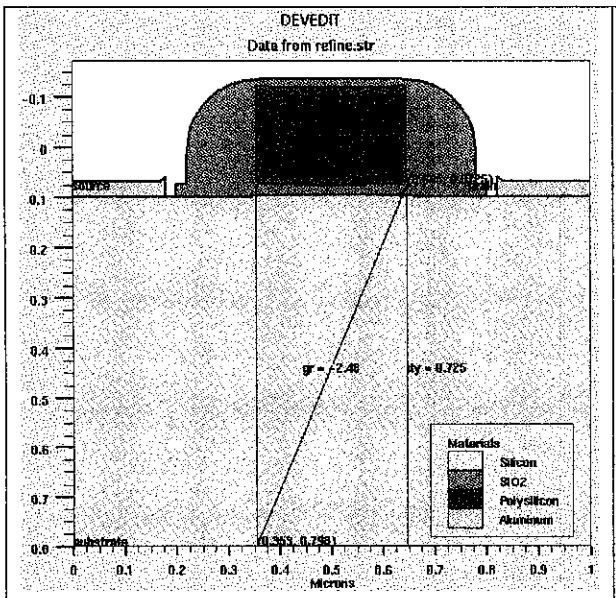


Figure 4.1: Optimized 0.3 Micron Structure

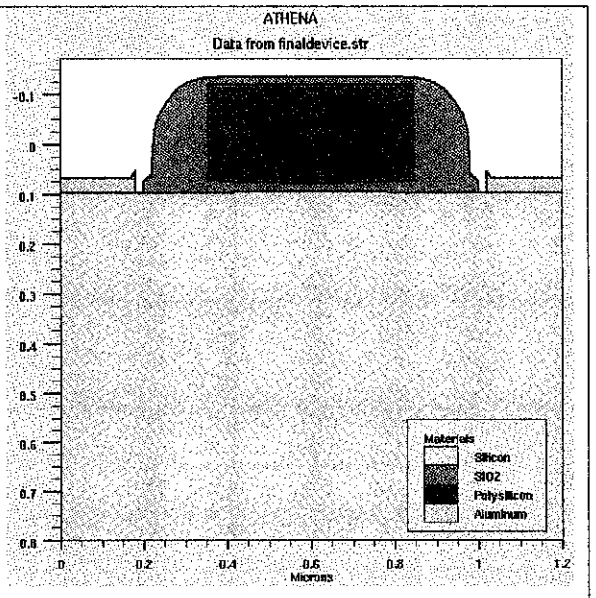


Figure 4.2: Un-optimized Structure as Sample Given in Silvaco IC MIRCOSYSTEM June 2003

This device is generated using real industry standard simulation parameters available in ATHENA software. This includes rapid oxidation, rapid thermal annealing, tilted angle ion implantation process with very detailed required parameters like impurities concentration, implantation energy, and angle implantation and simulation model. Program files and source code to render and generate the required optimized structure is attached in Appendix 7.1.

Table 4.1: Amendments to Existing Fabrication Steps

	Sample from Silvaco IC Microsystem	Optimized Structure
P-well Implant – Channel Doping	8×10^{12} cm^3 boron impurities	8×10^{10} cm^3 boron impurities
Gate length	0.5 micron length	0.3 micron length
Gate Oxide Thickness	130nm	100nm
Threshold Voltage Implant – After gate Oxidation	9.5×10^{11} cm^3	8×10^{11} cm^3
SiGe Layer	Not Applied	Applied as additional progress

4.2 DEVEDIT- STRUCTURE REMESH

Figure 4.3 and 4.4 show a comparison of the mesh structure between post mesh-improvement and the existing structure. Notice the extra fine structure for detail analysis and calculation after re-meshing. This is particularly important when the sub-micron device is put under electrical testing. Coarse structure will not allow detail analysis and will generate inappropriate data. Improving mesh structure can be performed using

ATHENA sub-components, DEVEDIT. By specifying required x and y coordinate mesh concentration, simulation is performed to match the nearest demanded structure.

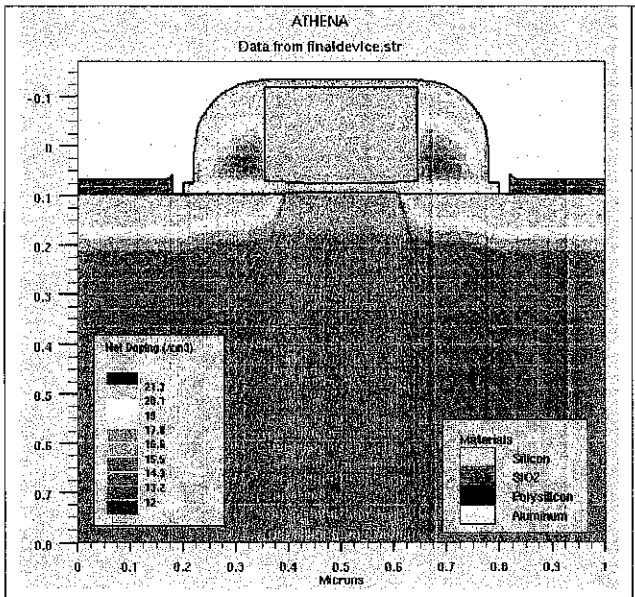


Figure 4.3: Extra Fine Mesh Concentration of 0.3 Micron (Optimized Structure)

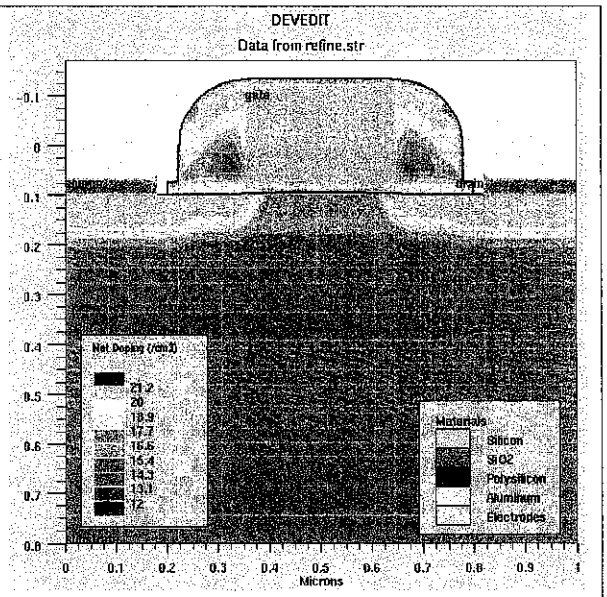


Figure 4.4: Coarse structure Before Mesh Improvement.

4.3 ATLAS ELECTRICAL TESTING

Various electrical testing have been obtained using Atlas device simulation to support the outcome of the optimization process. Majority of the testing is performed using finalized structure with **several testing** carried out by varying process parameters to obtain optimum value. When, varying one fabrication parameter, the other parameters and steps remain unchanged.

4.3.1 Threshold Voltage Reduction

From the formula shown in equation 2.19, it is observed that there are several factors that control the threshold voltage. The first one is channel doping which affects the Fermi potential. With channel doping increasing, the Fermi potential increases (Refer to

Equation 2.21). Also, with channel doping increasing, the depletion charge in the channel increases. Thus, more effort is needed to invert the channel. Therefore, by adjusting the channel doping to minimum concentration, the threshold voltage required to deplete the entire channel will be reduced. Thus, we reduce channel doping from 8E12 cm^3 to 8E10 cm^3.

The second factor is the gate oxide thickness. The gate oxide thickness is in reverse proportion to gate capacitance. With the gate oxide thickness increasing, the gate oxide capacitance goes down, which means the gate has less control on the channel and threshold voltage will increase. Thus, the reverse process is performed by reducing gate oxide thickness to minimize threshold voltage but limit the total off-stage leakage accumulated. Figure 4.5 and 4.6 show comparison of gate turn-on voltage before and after optimization. Significant improvement has been achieved from the standard 0.7 v diode turn-on.

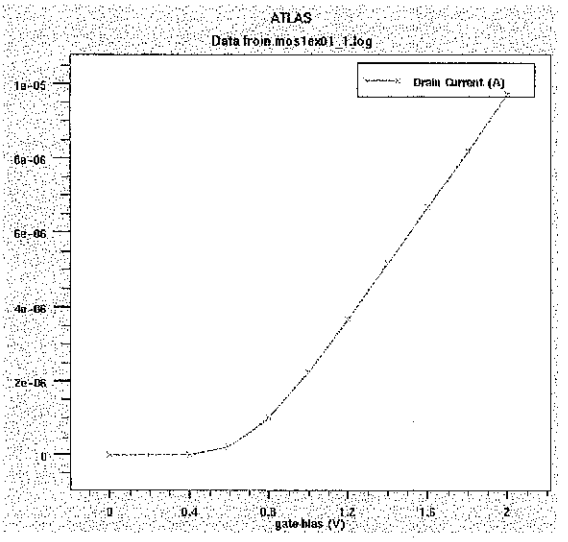


Figure 4.5: Threshold voltage at approximately 0.7V before optimization

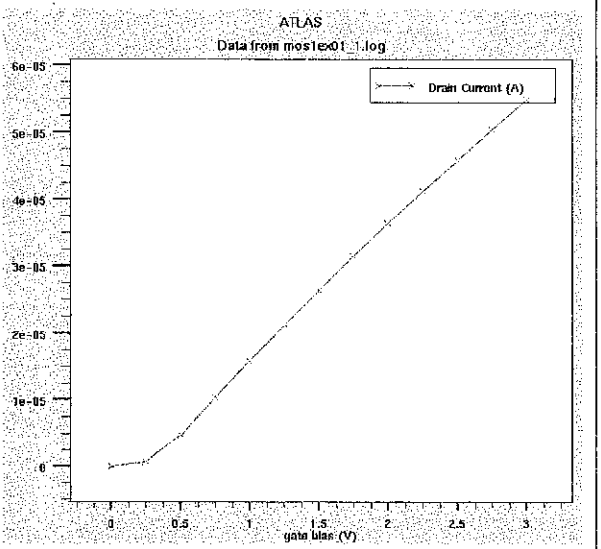


Figure 4.6: Gate turn on stand at 0.2V after optimization (Westwood 2)

Some adjustment has been performed on the doping concentration of P-well. It is observed that the gate voltage droped substantially when P-well doping concentration of boron is reduced **to 8e10cm**^{3} from an initial value of 8e12cm^3.

The initial program is as follows:

```
# P-well implant
implant boron dose=8e12 energy=100 tilt=0 rotation=0 crystal
lat.ratio1=1.0 \
        lat.ratio2=1.0
```

The modified program is:

```
# P-well implant
implant boron dose=8e10 energy=100 tilt=0 rotation=0 crystal
lat.ratio1=1.0 \
        lat.ratio2=1.0
```

4.3.2 Drain Current Extraction

When the dimension of an MOS transistor is reduced, three distinct features are seen in the device's characteristic. First, the drain current is found to increase with the drain voltage beyond pinch off [1]. This is in contrast with the I-V curves of a long channel transistor, where the drain current becomes constant after the pinch off condition is reached. The drain current tends to exhibit soft breakdown that is not seen in long channel. Furthermore, the drain current is not zero at zero gate voltage.

The second distinct short-channel characteristic is seen in the sub-threshold regime. When the gate length minimizes to submicron, the basic shape of the long channel device remains unchanged. However, in the extreme case, where gate length is in nano scale, the output current might not be able to turn off, and the transistor might not be able to

function as a switch. However, to date, INTEL has managed to produce efficient MOSFET switching device down to 90nm length [2].

The third feature is the shift of the threshold voltage with the channel length. The threshold voltage decreases with the channel length. Figure 4.7 and 4.8 show drain current extraction for general MOSFET and the optimized structure, respectively. The optimized structure experiences both left shift in threshold and exponential increment of drain current.

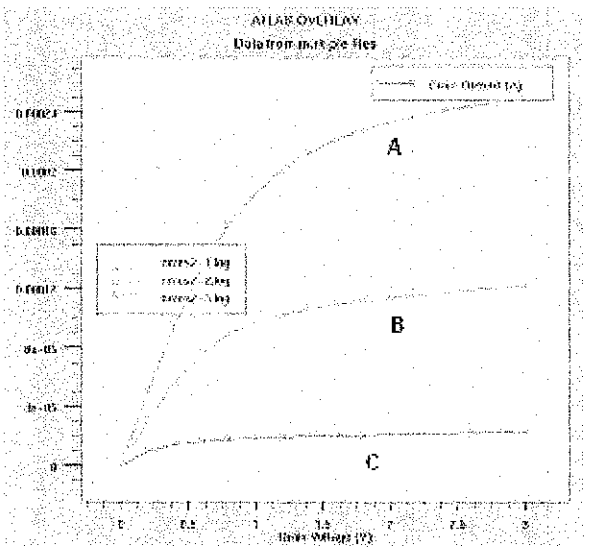


Figure 4.7: Drain Current Extraction Before Optimization

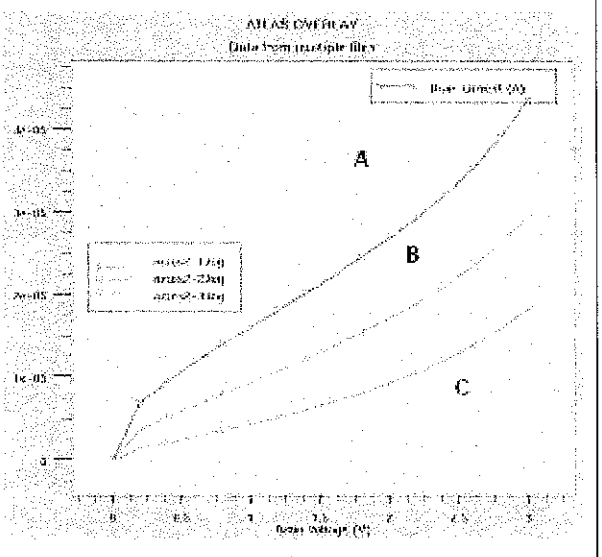


Figure 4.8: Drain Current Extraction After Optimization (Westwood)

To show that drain current can only be extracted when Vgs is larger than V_T, we perform drain current ramping with various given Vgs. The output verifies such that only Vgs higher than 0.2V can turn the device on, as shown in figure 4.9.

```
solve vgate=0.05  outf=solve1  (nmos2-1.log)
solve vgate=0.08  outf=solve2  (nmos2-2.log)
solve vgate=0.1   outf=solve3  (nmos2-3.log)
solve vgate=0.15  outf=solve4  (nmos2-4.log)
solve vgate=0.5   outf=solve5  (nmos2-5.log)
```

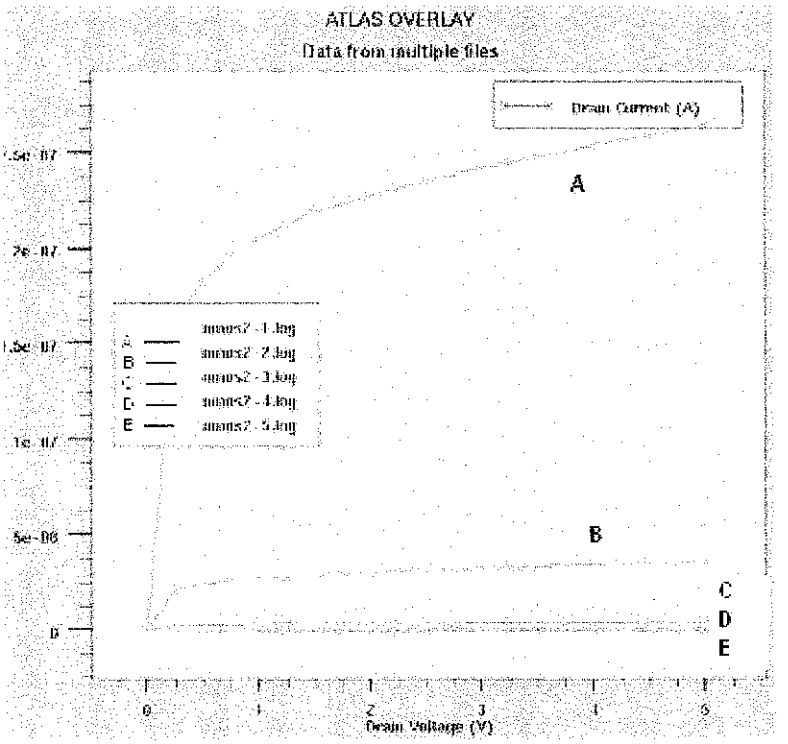


Figure 4.9: Various Vgs to Turn the Device to On-State

4.3.3 Optimization of Drain Current

The ideal drain voltage to be used is 0.5v because it delivers high current while still in the **ohmic zone (V=IR).** When the curve converges, power loss is very high due to more voltage needed to deliver minimal current. Figure 4.10 shows optimized drain voltage. If the graph is extrapolated further, the drain current should increase beyond pinch off but at lower rate. This is the characteristic of short-channel transistor. It also exhibit soft breakdown that is not seen in long-channel devices. The characteristic and explanation of soft breakdown in short-channel device is further explained in section 4.3.10.

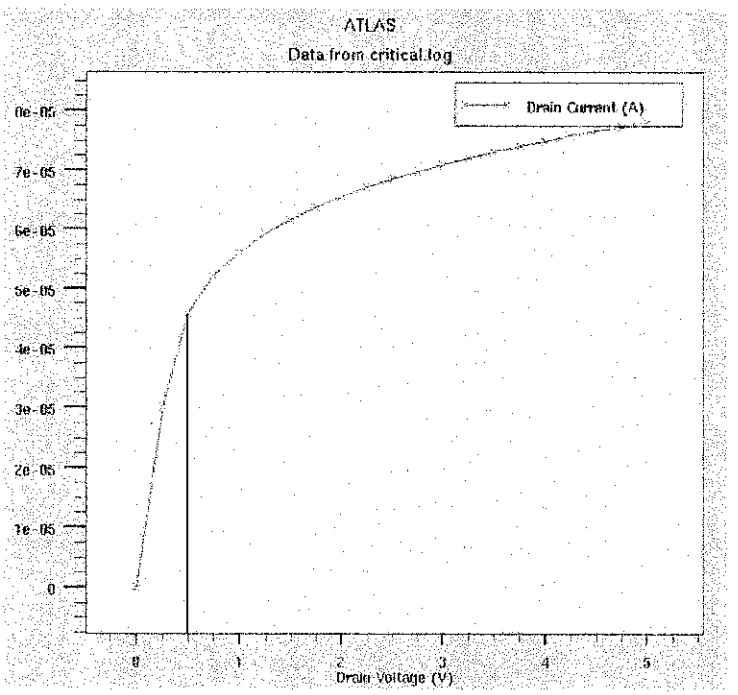


Figure 4.10: Recommended Drain Voltage Stood at 0.5V

The reason why $V_D = 0.5V$ is chosen is due to the stated theory that if $V_D \geq V_{DSAT}$, the drain current remains almost constant or converge [3]. It can be seen that V_{DSAT} in our fabricated device should stand at 0.5V before the **curve bends down significantly**.

Figure 4.11 gives some brief explanation on the expected optimum current and voltage near saturation point. Notice that the dotted line shows saturated V_{DSAT}. Optimum V_D and Drain current can be achieved by fixing our drain voltage in the intersection between dotted line and drain current curve. In figure 4.10 it intersects at V=0.5V.

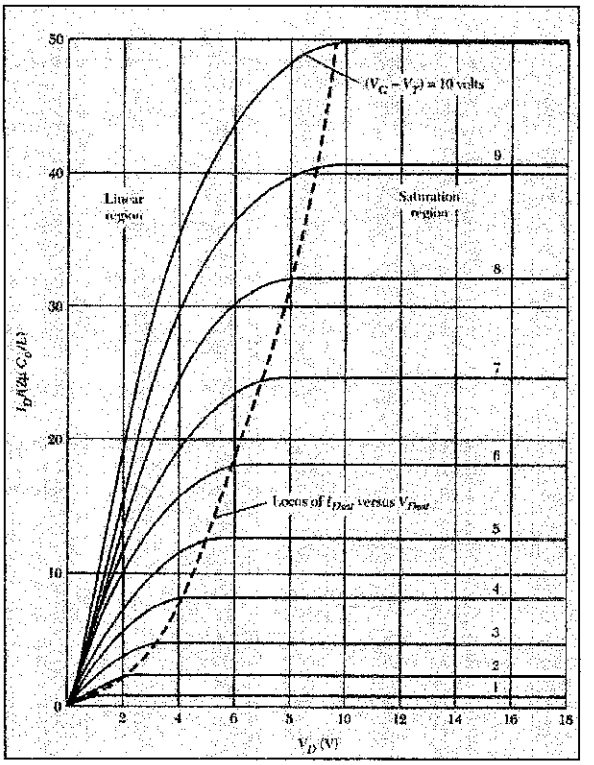


Figure 4.11: Optimum Drain Voltage and Drain Current Extraction

4.3.4 Leakage Current Extraction

As stated previously, less threshold voltage will lead to higher off-state leakage current. This theory is also valid to the optimized device where significant leakage current is collected when threshold voltage is minimized. However, the main concern over here is to ensure that the accumulated leakage current does not exceed the maximum acceptable leakage.

According to the theory, as long as [2]:

$$\frac{Ion}{Ioff \times leakage} > 10^6 \tag{4.1}$$

Then, the device leakage current is deemed acceptable. Here, it's noticed that the turn-off leakage current for the optimized 0.3micron (0.3V threshold voltage) device is

1.2589 x 10^{-12} A/um. The recorded leakage current proves to be much better than the one recorded by the primitive 0.5micron with 0.7v threshold voltage. The 0.5 micron structure recorded **1.258 x 10^{-9} A/um.** The drain current extracted at Vds=0.5V stood at 4.5 x 10^{-5} ampere. Thus, $\frac{4.5 \times 10^{-5}\ (\mathrm{ID})}{1.2589 \times 10 - 12\ \mathrm{A/um}} = 36x10^{6}$ which exceed 10^{6}.As mentioned previously, as long as $\frac{Ion}{Ioff, leakage} > 10^{6}$, the fabricated device is considered as passing minimal leakage tolerance level. Figure 4.12 and 4.13 show the collected leakage current extraction on logarithm scale for both optimized and un-optimized structure.

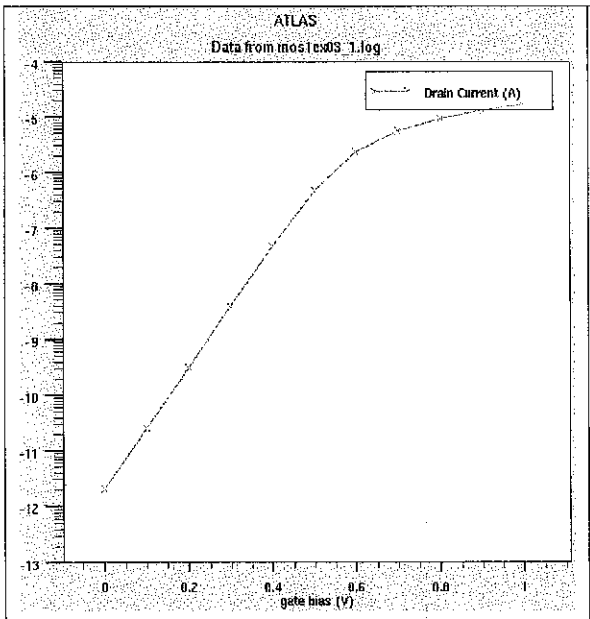


Figure 4.12 : Leakage current, Ioff, for 0.3micron structure is 1.2589 x 10^{-12} A/um (Westwood)

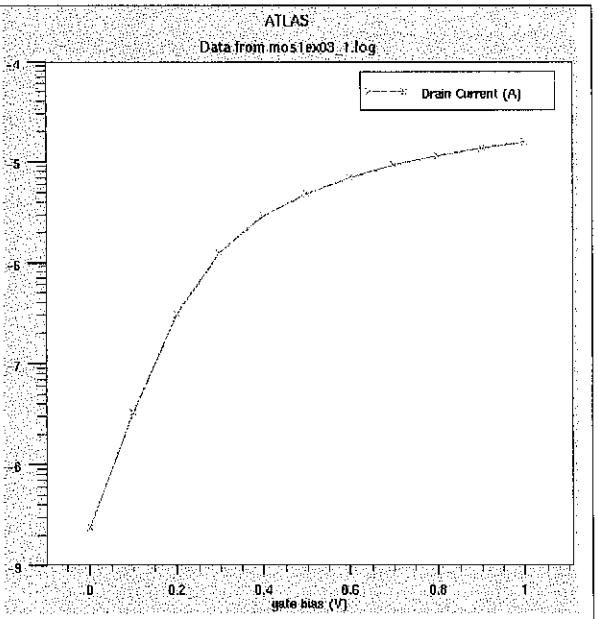


Figure 4.13: Leakage current for 0.5micron structure is 1.258 x 10^{-9} A/um

4.3.5 Leakage Current Extraction & Comparison Using Gate Oxide

Few gate oxide thicknesses have been fabricated and optimized through ATHENA. The exact gate oxide thickness is extracted using optimizer. Figure 4.14 and 4.15 show the optimization process to extract 20nm and 100nm gate oxide thickness, respectively.

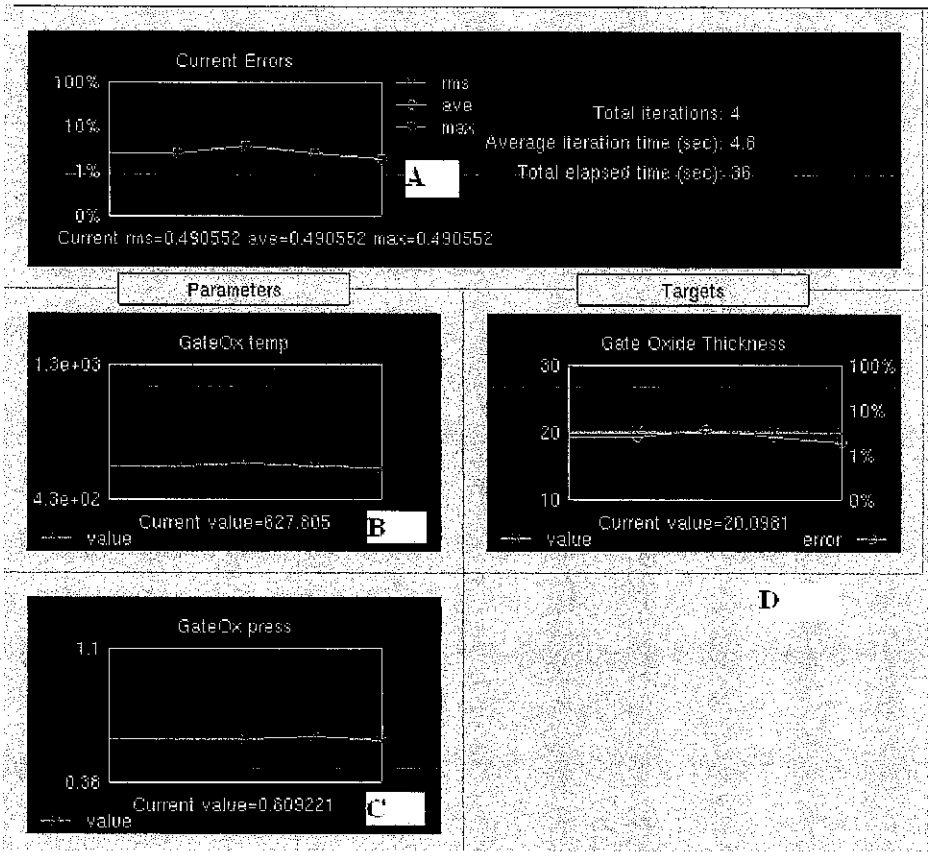


Figure 4.14: Gate Thickness Optimizer: 20nm

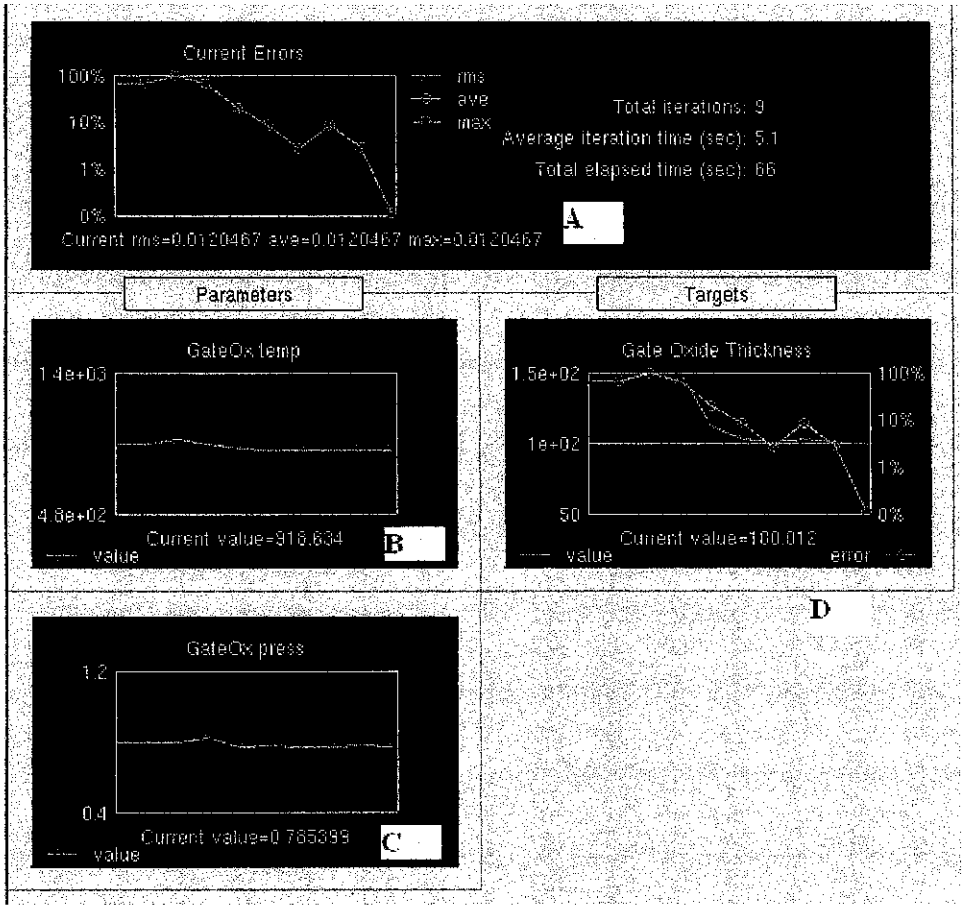


Figure 4.15: Gate Thickness Optimizer: 100nm

Column A shows maximum allowable error that might vary final oxide thickness from expected value. Since target thickness is obtained from varying temperature and pressure, there will be variation or deviation from the finalized thickness. ATHENA software takes into consideration fabrication process in the real world entity. Column B and C show the expected furnace temperature and pressure required to grow the expected oxide thickness. Column D shows final gate oxide obtained.

Off-state leakage is obtained from ATLAS parameter. From the analysis, off-state current increases with reduction of gate oxide thickness. Table 4.2 shows required recipe to obtain particular gate oxide thickness and the off-state leakage drawn.

Table 4.2: Gate Oxide Growth Recipe and Off-Stage Leakage Recorded

Gate Oxide Thickness	Recipe	Off-stage Leakage
200nm	Temperature: 981.847 Pressure: 0.826826 Time: 15 minutes HCI pressure: 3	0.03 micro ampere
130nm	Temperature: 960.106 Pressure: 0.81588 Time: 15 minutes HCI pressure: 3	0.0199 micro ampere
100nm	Temperature: 919.298 Pressure: 0.785952 Time: 15 minutes HCI pressure: 3	0.125 micron ampere
50nm	Temperature: 859.848 Pressure: 0.755641 Time: 15 minutes HCI pressure: 3	1.58 micron ampere
20nm	Temperature: 627.805 Pressure: 0.60921 Time: 15 minutes HCI pressure: 3	6.3 micron ampere

The oxidation time and HCI pressure has been kept constant since it's easier to manipulate overall furnace temperature and pressure than varying HCI acidic concentration or time. Figure 4.16 shows relationship of Gate Oxide Thickness to off-stage leakage. Notice that the leakage current ramp up when oxide thickness is minimized to less than 100nm. Most probably, tunneling effect will occur when sufficient electric field is present to excite carriers passing through the gate oxide.

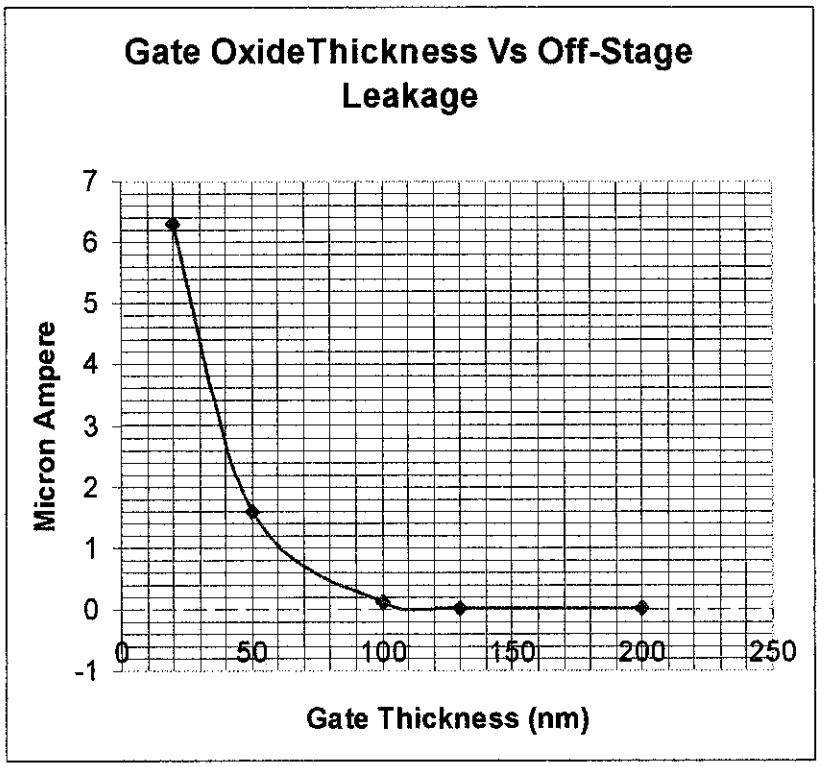


Figure 4.16: Gate Oxide Thickness Versus Off-Stage Leakage

Minimization of gate oxide thickness will reduce the overall threshold voltage and indirectly power required to run this device. However, enormous leakage current has been recorded once oxide thickness is reduced to less than 100nm. Thus, it's best to maintain gate oxide thickness at 100nm unless other better dielectric materials like silicon nitride is utilized. The exact thickness limit varies for each device and fabrication components.

4.3.6 Analysis of Best Channel Doping Concentration

This experiment validates the relationship between channel doping and threshold voltage. Various concentration of channel doping is obtained through ion implantation. After this, threshold voltage is extracted from the Atlas simulation. At the end of the experiment, a finalized channel doping backed with theoretical explanation is chosen as the finalized device process parameters. Table 4.2 shows experimented channel doping versus acquired threshold voltage.

Table 4.2: Channel Doping versus Threshold Voltage

Channel Doping	Threshold Voltage (v)
8e13 cm^3	1.14603
8e12 cm^3	0.477319
8e11 cm^3	0.263273
5e11 cm^3	0.23712
8e10 cm^3	0.075V – 0.2V

From the analysis, it's obvious that the threshold voltage reduces to less than 0.2V once channel doping drops to **8e10 cm^3 and below**. This analysis is valid based on previous discussion that Fermi potential drops as channel doping reduces. However, anything lower than that might cause our NMOS to lose its extrinsic properties, thus failing to act as a switching device. With very minimum channel doping, MOSFET cannot create appropriate inversion layer when field effect is excited from gate. Furthermore, very low threshold voltage might cause off-stage leakage to rise exponentially. In other words, it is best not to have low channel doping but end up having very thick gate oxide just to overcome leakage problem.

4.3.7 Analysis of Best Tilt Angle for Ion Implantation on the Substrate

The channeling effect causes some ions to penetrate deeply into the single-crystal substrate. This can form a "tail" on the normal dopant distribution curve. It is an undesirable dopant profile, which could affect microelectronic device performance. Therefore several methods have been used to minimize this effect.

One way to minimize the channeling effect is ion implantation on a tilted wafer, typically with a tilt angle of 7 degrees. By tilting the wafer, the ions impact with the wafer at an angle and cannot reach the channel. The incident ions will have nuclear collisions right away, and effectively reduce channeling effect.

Another way to solve channeling effect is to diffuse a layer of thin silicon dioxide. Thermally grown silicon dioxide is an amorphous material. The passing implantation ions collide and scatter silicon and oxygen atoms in the screen layer before they enter the single-crystal silicon substrate.

4.3.8 Analysis of Best Ion Implantation Energy

Energetic ions penetrate the target, gradually lose their energy through collision with the atoms in the substrate, and eventually rest inside the substrate. Figure 4.17 shows ion trajectory and projected range.

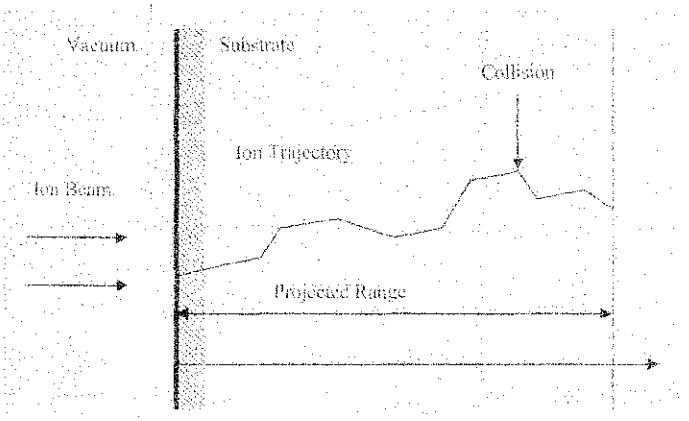


Figure 4.17: Ion trajectory and projected range

Generally, the higher the ion energy, the deeper it can penetrate into the substrate. However, even with the same implantation energy, ions do not stop exactly at the same depth in the substrate, because each ion has different collisions with different atoms.

Higher-energy ion beam can penetrate deeper into substrate, and therefore have a longer projected ion range. Since smaller ions have smaller collision cross sections, smaller ions at the same energy can penetrate deeper into substrate and the mask materials.

Projected ion range is an important parameter for ion implantation, because it indicates the ion energy needed for certain dopant junction depth. It also gives information on the required implantation barrier thickness for ion implantation process. Since our substrate thickness is 0.8 micron and effective thickness required could be only 0.5 micron, we use **100 keV** energy to bombard boron into the substrate.

4.3.9 Junction Breakdown

When a sufficiently large reverse voltage is applied to a p-n junction, the junction breaks down and conducts a very large current. Although the breakdown process is not inherently destructive, the maximum current must be limited by an external circuit to avoid excessive junction heating. Figure 4.18 shows damage after avalanche effect in the optimized structure. Figure 4.19 is the avalanche effect caused by existing normal MOSFET structure. One of the reason optimized device experience less impact is due to the soft breakdown characteristic owned by short-channel device.

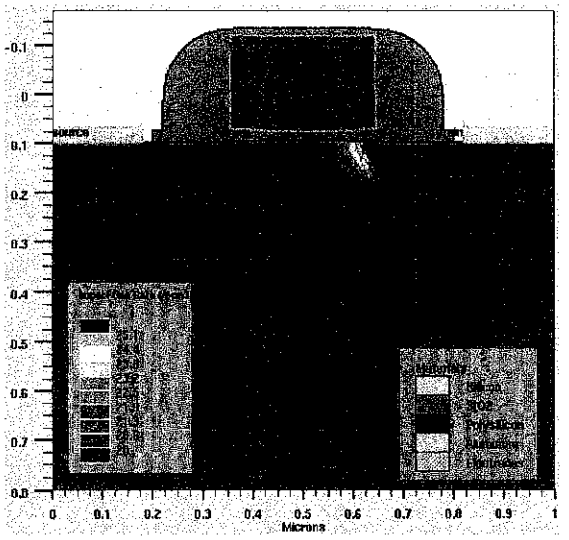


Figure 4.18: Junction Breakdown Extraction, 0.3 micron

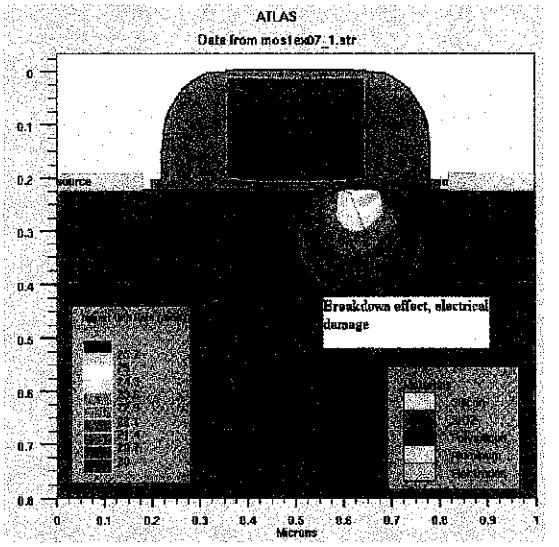


Figure 4.19: The non-optimized MOSFET shows weak defend against excess of current

4.3.10 Transient Response

An experiment has been conducted to test the capability of single device's reaction over a single pulse. The device under test has shown rise time and fall time within a pulse size of 1000ps. The fall time from peak 5v until reaching steady state off-voltage is 1.0 e-9 second or equivalent to 1Ghz switching speed when going from high to low voltage. The rise time is recorded at much significant higher speed at 2 e-10 second or 5Ghz.

From the code:

```
#      NMOS inverters - transient simulation
#
#      Circuit description
#
vin 1 0 0. PULSE 0 5 0 50ps 50ps 1000ps 10
an 2=drain 1=gate 0=source 0=substrate infile=mos2ex01_0.str width=15.
mn 3 2 0 0 simple L=2.0u W=5u
r1 2 4 10k
r2 3 4 10k
vcc 4 0 5.
c1 3 0 3ff
#
#      End of circuit description
```

We specify pulse input with voltage ramp from low of 0 V to 5 V. There is no time delay, and initial rise and fall time of pulse to be 50 ps. The pulse length is 1000 ps.

PULSE V1 V2 TD RT FT LT P

Keyword PULSE is the heading or main function call to initiate pulse generation. V1 and V2 stand for low voltage and high voltage of the pulse. It is quite similar to logic 1 and logic 0 in digital system. TD is the delay implemented before next start. RT and FT is the initial ramp up time and fall time of the pulse. IT can be as small as few picoseconds. Period is the period or length of pulse width.

Thus, when performing transient analysis to monitor switching characteristic, we have to ensure total time under transient is greater than rise time + fall time + pulse length, to view entire switching graph. In this case, since pulse length and propagation delay time is approximately 1100 ps, we set transient to 3000 ps. Figure 4.20 shows the extracted transient analysis simulation performed on optimized device, given a pulse time of 1000 picoseconds and negligible rise and fall time.

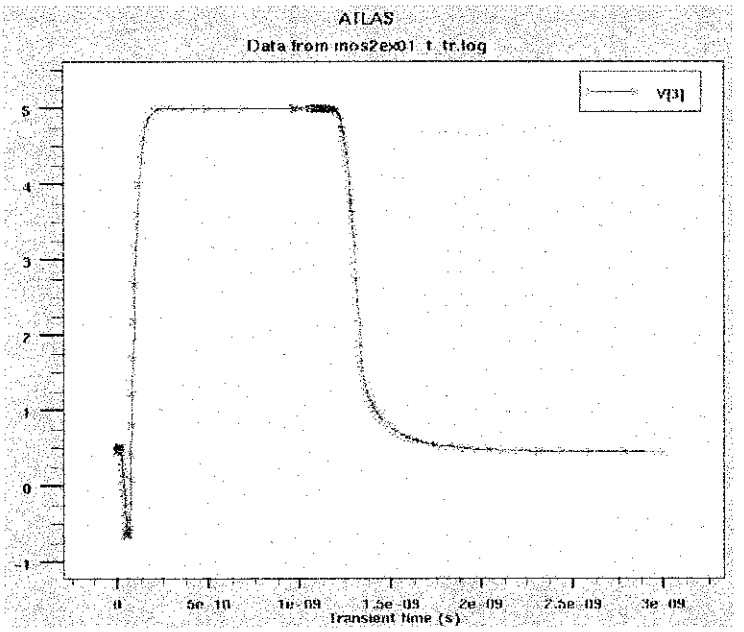


Figure 4.20: Pulse Generated With Response Time

4.3.11 Resistance Calculation

Gate Poly is only about 2 to 3 ohms per square. This low value of resistance works well for gates but useful range of resistance is much more than that. One way of making a region of higher resistance is to implant extra stuff in the poly, discouraging electrons flow or making the poly thinner. Thus, thickness of poly does make a significant role in controlling the overall resistivity. Total resistance calculated theoretically:

$$R = \frac{Lb + \delta Lb}{Wb + \delta Wb} Pb + 2\frac{Lh + \delta Lh}{Wh + \delta Wh} Ph + 2\frac{Rc}{Wc + \delta Wc}$$

$$R = \left(\frac{\left(1.2x10^{-6}\right) + \left(0.05x1.2x10^{-6}\right)}{\left(0.6x10^{-6}\right) + \left(0.05x0.6x10^{-6}\right)} x3.3x10^{3}\Omega - m \right) + 2\left(\frac{23\Omega - micron}{0.03micron} \right)$$

$$R = \left(\frac{1.26x10^{-6}}{0.63x10^{-6}} \right) x3.3x10^{3}\Omega - m + \left(1533.33\Omega\right)$$

$$R = 6600\ \Omega + 1533.33\Omega$$

$$R = 8133.33 \text{ ohm}$$

Here we assume that contact resistance will be the depth of source and drain, body resistance covers entire channel length and head resistance to be ignored since we didn't implant additional chunk of poly on top of source/ drain region.

The sheet resistivity is taken from silicon properties of 3.3×10^3 ohm –meter. However, the exact value simulated using atlas electrical parameters might vary due to introduction of impurities.

4.3.12 Optimization Obtained

This project has successfully optimized several electrical characteristic of NMOS based on the improvement on the fabrication steps and material used. Table 4.3 gives a comparison of optimization achieved by comparing with existing structure given in sample NMOS recipe from Silvaco IC Microsystem

Table 4.3: Optimization Achieved Throughout the FYP Project

Electrical Parameters	**NMOS recipe from Silvaco IC Microsystem**	**Optimized Device**
Threshold Voltage	0.7V	0.2V
Drain Current Extraction	Pinch off at drain voltage 2V	Rise beyond pinch off, short channel characteristic.
Off-state Leakage	**1.258×10^{-9} A/um**	**1.2589×10^{-12} A/um**
Tilt-angle for Ion Implantation	No tilt angle perform, experienced channeling effect	Reduce channeling effect after tilt angle 7 degrees for ion implantation
Junction Breakdown	Weak against excessive current	Soft breakdown
Transient Response	Less than 1 Ghz Switching Speed	2Ghz Switching Speed, performed on simplified Inverter Circuit

CHAPTER 5

CONCLUSIONS & RECOMMENDATIONS

5.1 CONCLUSIONS

Athena & Atlas is a very useful simulation software for various optimization of different types of semiconductor devices. It is a good starting point for researchers and industry practitioners to actually fabricate a virtual device before transferring the design pattern into costly lab experiment. By using this software, user can minimize the production cost since the effect of varying all the necessary parameters can be analyzed by simulation.

Several objectives have been achieved throughout this project. This includes simulating fabrication of an NMOS device which follows industry fabrication standards ranging from mesh initialization to aluminum contact deposition. The final device output has been extracted as shown in figure 4.1. Various optimization and testing at the process simulation have been performed such as applying different doping concentration at the channel, varying gate oxide and device size, utilizing different substrate material and varying process parameters. The VLSI fabrication theory has been acquired up to a **sufficient depth level** to perform optimization on the NMOS device which leads to better threshold voltage reduction, drain current extraction, power loss minimization, break down effect reduction, minimization of resistivity, smaller leakage current and faster switching speed. In order to perform optimization, in depth understanding of various capabilities of ATHENA & ATLAS is a must. Most of the optimization is performed by editing the source code used to generate device structure and electrical testing output.

selection of appropriate combination ratio of silicon and germanium to obtain best mobility especially in NMOS. Many researches have been conducted to study only certain combination ratio of Si_XGe_y without considering its application on circuit like switching and inverter.

Thus, it's the next progress recommendation to apply SiGe layer and perform electrical testing. The objective of this project work is to verify the statement or conclusion drawn in the international journals. Furthermore, it can assist in the capability in researching and verifying new technology.

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APPENDIX 1

ATHENA SOURCE CODE TO FABRICATE NMOS DEVICE

```
go athena

# Non-uniform Grid
line x loc=0.00 spac=0.10
line x loc=0.30 spac=0.02
line x loc=0.40 spac=0.006
line x loc=0.50 spac=0.01

#
line y loc=0.00 spac=0.03
line y loc=0.2 spac=0.02
line y loc=0.8 spac=0.1

# Initial Substrate
init silicon c.phosphor=1.0e14 orientation=100 two.d

# struct outfile=substrate.str

# P-well implant
implant boron dose=8e10 energy=100 tilt=0 rotation=0 crystal
lat.ratio1=1.0 \
        lat.ratio2=1.0
#
diffus time=10 temp=950 weto2 press=1.00 hcl.pc=3

#
diffus time=62 temp=950 t.final=1200 dryo2 press=1.00 hcl.pc=3

#
diffus time=220 temp=1200 nitro press=1.00

#
diffus time=90 temp=1200 t.final=800 nitro press=1.00

#
etch oxide all

# Gate Oxidation, Target Thickness = 100nm
diffus time=15 temp=919.298 dryo2 press=0.785952 hcl.pc=3

#
extract name="Gate Oxide Thickness" thickness material="SiO~2"
mat.occno=1 \
        x.val=0.45



#
```

```
implant boron dose=8.0e11 energy=10 tilt=0 rotation=0 amorph
lat.ratio1=1.0 \
        lat.ratio2=1.0
#
deposit poly thick=0.2 divisions=10

#
etch poly left p1.x=0.35
#
method compress init.time=0.10 fermi
diffus time=3 temp=900 weto2 press=1.00 hcl.pc=3
#
implant phosphor dose=3e15 energy=20 tilt=0 rotation=0 amorph
lat.ratio1=1.0 \
        lat.ratio2=1.0
#
deposit oxide thick=0.12 divisions=8

#
etch oxide dry thick=0.12

#
implant arsenic dose=5.0e15 energy=50 tilt=0 rotation=0 amorph
lat.ratio1=1.0 \
        lat.ratio2=1.0

#
method compress init.time=0.10 fermi
diffus time=1 temp=900 nitro press=1.00

#
etch oxide left p1.x=0.2

#
deposit alumin thick=0.03 divisions=2

#
etch aluminum right p1.x=0.18

#
extract name="sdxj" xj material="Silicon" mat.occno=1 x.val=0.1
junc.occno=1

# extract the long chan Vt...
extract name="n1dvt" 1dvt ntype vb=0.0 qss=1e10 x.val=0.49

# extract a curve of conductance versus bias....
extract start material="Polysilicon" mat.occno=1 bias=0.0 bias.step=0.2
bias.stop=2 x.val=0.45
extract done name="sheet cond v bias" curve(bias,1dn.conduct
material="Silicon" mat.occno=1  region.occno=1) outfile="extract.dat"


# extract the N++ regions sheet resistance...
```

```
extract name="n++ sheet rho" sheet.res material="Silicon" mat.occno=1
x.val=0.05 region.occno=1

# extract the sheet rho under the spacer, of the LDD region...
extract name="ldd sheet rho" sheet.res material="Silicon" mat.occno=1
x.val=0.3 region.occno=1

#
extract name="channel surface conc." surf.conc impurity="Net Doping" \
        material="Silicon" mat.occno=1 x.val=0.45
#
extract name="Vt" 1dvt ntype qss=1e10 x.val=0.45
#
struct mirror right
#
electrode name=gate x=0.5 y=0.1
#
electrode name=source x=0.1
#
electrode name=drain  x=0.84
#
electrode name=substrate backside
structure outfile=finaldevice.str


########################refine the mesh###################################

go devedit
# Set Meshing Parameters
#
base.mesh height=0.1 width=0.1
#
bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
line.straightening=1 align.points when=automatic
#
imp.refine imp="NetDoping" sensitivity=1
imp.refine min.spacing=0.02
#
constr.mesh max.angle=90 max.ratio=300 max.height=1 \
      max.width=1 min.height=0.0001 min.width=0.0001
#
# Perform mesh operations
#
Mesh Mode=MeshBuild
refine mode=y x1=0.34 y1=0.22 x2=0.65 y2=0.24
refine mode=y x1=0.35 y1=0.22 x2=0.67 y2=0.23
refine mode=both x1=0.65 y1=0.26 x2=0.83 y2=0.34
refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.57
refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.53
refine mode=y x1=0.80 y1=0.34 x2=1.0 y2=0.38
structure outf=refine.str


tonyplot refine.str
```

APPENDIX 2

ATLAS – BREAKDOWN VOLTAGE EXTRACTION

```
go atlas

# Set workfunction for poly gate and interface charge
contact name=gate n.polysilicon
interf  qf=3E10

# Set models
models  print cvt consrh

impact selb


method  newton trap climit=1e-4

# open log file
log outf=moslex07.log

solve vdrain=0.025
solve vdrain=0.05
solve vdrain=0.1
solve vdrain=0.5

solve vstep=0.25 vfinal=12 name=drain compl=5e-9 cname=drain
save outf=moslex07_1.str


# Extract the design parameter, Vbd
extract name="NVbd" x.val from curve(abs(v."drain"),abs(i."drain"))
where y.val=1e-9

tonyplot  moslex07.log -set moslex07_log.set
tonyplot  moslex07_1.str -set moslex07_1.set

quit
```

APPENDIX 3

ATLAS – ID-VGS CURVE EXTRACTION

```
go atlas

# define the Gate workfunction
contact name=gate n.poly

# Define the Gate Qss
interface qf=3e10

# Use the cvt mobility model for MOS
models cvt srh print numcarr=2

# set gate biases with Vds=0.0
solve init
solve vgate=1.1 outf=solve_tmp1
solve vgate=2.2 outf=solve_tmp2
solve vgate=3.3 outf=solve_tmp3

#load in temporary files and ramp Vds
load infile=solve_tmp1
log outf=mos1ex02_1.log
solve name=drain vdrain=0 vfinal=3.3 vstep=0.3

load infile=solve_tmp2
log outf=mos1ex02_2.log
solve name=drain vdrain=0 vfinal=3.3 vstep=0.3

load infile=solve_tmp3
log outf=mos1ex02_3.log
solve name=drain vdrain=0 vfinal=3.3 vstep=0.3

# extract max current and saturation slope
extract name="nidsmax" max(i."drain")
extract name="sat_slope" slope(minslope(curve(v."drain",i."drain")))

tonyplot -overlay -st mos1ex02_1.log  mos1ex02_2.log mos1ex02_3.log -
set mos1ex02_1.set

quit
```

APPENDIX 4

ATLAS – THRESHOLD VOLTAGE EXTRACTION

```
go atlas

# set material models
models cvt srh print

contact name=gate n.poly
interface qf=3e10

method newton
solve init

# Bias the drain
solve vdrain=0.1

# Ramp the gate
log outf=mos1ex01_1.log master
solve vgate=0 vstep=0.25 vfinal=3.0 name=gate
save outf=mos1ex01_1.str

# plot results
tonyplot  mos1ex01_1.log -set mos1ex01_1_log.set

# extract device parameters
extract name="nvt"
(xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
      - abs(ave(v."drain"))/2.0)

quit
```

APPENDIX 5

ATLAS – LEAKAGE CURRENT EXTRACTION

```
go atlas


# set material models
models cvt srh print
contact name=gate n.poly
interface qf=3e10


# get initial solution

solve init

method  newton trap
solve prev


# Bias the drain a bit...
solve vdrain=0.025 vstep=0.025 vfinal=0.1 name=drain
# Ramp the gate to a volt...
log outf=mos1ex03_1.log master
solve vgate=0 vstep=0.1 vfinal=1.0 name=gate


# extract the device parameter SubVt...
extract init inf="mos1ex03_1.log"
extract name="nsubvt"
1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))
tonyplot mos1ex03_1.log -set mos1ex03_1_log.set

quit
```

APPENDIX 6

DECKBUILD OUTPUT – ATHENA NMOS FABRICATION

```
                                A T H E N A

                              Version 5.6.0.R

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   We acknowledge the contribution of the following collaborative
partners:

                                Stanford University
                            University of Texas at Austin
                    MCNC Center for Microelectronic Systems Technologies
                            University of California at Berkeley
                                  Harris Semiconductor
                              CNET-Grenoble (France Telecom)
                EPSRC supported Ion Beam Centre at the University of Surrey


 ============================================================
 ATHENA                                 :  Enabled
 SSUPREM4                               :  Enabled
   Silicide material                    :  Enabled
   BCA Ion Implant                      :  Enabled
 ELITE                                  :  Enabled
   Monte Carlo Deposit                  :  Enabled
 OPTOLITH                               :  Enabled
 FLASH                                  :  Enabled
 C Interpreter                          :  Enabled
 Adaptive Meshing                       :  Enabled
 ============================================================

                        It is now Mon Oct 25 10:34:39 2004

                      Athena 5.6.0.R is executing on "icfab1"


Loading model file 'athenamod'... done.
ATHENA>
ATHENA>
ATHENA> # Non-uniform Grid
ATHENA> line x loc=0.00 spac=0.10
ATHENA> line x loc=0.30 spac=0.02
ATHENA> line x loc=0.40 spac=0.006
ATHENA> line x loc=0.50 spac=0.01
ATHENA> #
```

```
ATHENA> line y loc=0.00 spac=0.03
ATHENA> line y loc=0.2 spac=0.02
ATHENA> line y loc=0.8 spac=0.1
ATHENA> # Initial Substrate
ATHENA> init silicon c.phosphor=1.0e14 orientation=100 two.d
ATHENA> struct outfile=.history05.str
ATHENA> #
ATHENA> struct outfile=substrate.str
ATHENA>
ATHENA> # P-well implant
ATHENA> implant boron dose=8e10 energy=100 tilt=0 rotation=0 crystal
lat.ratio1=1.0 \
>         lat.ratio2=1.0
ATHENA> struct outfile=.history06.str
ATHENA> #
ATHENA> diffus time=10 temp=950 weto2 press=1.00 hcl.pc=3
Solving time (hh:mm:ss.t)  00:00:00.0  + [1e-05  sec]  [100   %]  [np
825]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.0009 sec]  [9900  %]  [np
825]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.1    sec]  [10101.%]  [np
825]
Solving time (hh:mm:ss.t)  00:00:00.1  + [0.5767 sec]  [576.75%]  [np
825]
Solving time (hh:mm:ss.t)  00:00:00.6  + [2.0738 sec]  [359.57%]  [np
825]
Solving time (hh:mm:ss.t)  00:00:02.7  + [8.6739 sec]  [418.25%]  [np
825]
Solving time (hh:mm:ss.t)  00:00:11.4  + [57.789 sec]  [666.23%]  [np
825]
Solving time (hh:mm:ss.t)  00:01:09.2  + [150    sec]  [259.56%]  [np
825]
Solving time (hh:mm:ss.t)  00:03:39.2  + [150    sec]  [100   %]  [np
825]
Solving time (hh:mm:ss.t)  00:06:09.2  + [150    sec]  [100   %]  [np
825]
Solving time (hh:mm:ss.t)  00:08:39.2  + [40.392 sec]  [26.928%]  [np
792]
Solving time (hh:mm:ss.t)  00:09:19.6  + [40.392 sec]  [100   %]  [np
792] *
Solving time (hh:mm:ss.t)  00:10:00.0
ATHENA> struct outfile=.history07.str
ATHENA> #
ATHENA> diffus time=62 temp=950 t.final=1200 dryo2 press=1.00 hcl.pc=3
Solving time (hh:mm:ss.t)  00:00:00.0  + [1e-05  sec]  [100   %]  [np
792]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.0009 sec]  [9900  %]  [np
792]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.1    sec]  [10101.%]  [np
792]
Solving time (hh:mm:ss.t)  00:00:00.1  + [28.953 sec]  [28953.%]  [np
792]
Solving time (hh:mm:ss.t)  00:00:29.0  + [125.70 sec]  [434.15%]  [np
792]
```

```
Solving time (hh:mm:ss.t)  00:02:34.7  + [597.53 sec]  [475.34%]  [np
792]
Solving time (hh:mm:ss.t)  00:12:32.2  + [930    sec]  [155.63%]  [np
792]
Solving time (hh:mm:ss.t)  00:28:02.2  + [436.28 sec]  [46.912%]  [np
792]
Solving time (hh:mm:ss.t)  00:35:18.5  + [930    sec]  [213.16%]  [np
792]
Solving time (hh:mm:ss.t)  00:50:48.5  + [671.42 sec]  [72.195%]  [np
759]
Solving time (hh:mm:ss.t)  01:02:00.0
ATHENA> struct outfile=.history08.str
ATHENA> #
ATHENA> diffus time=220 temp=1200 nitro press=1.00
Solving time (hh:mm:ss.t)  00:00:00.0  + [1e-05  sec]  [100   %]  [np
759]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.0009 sec]  [9900  %]  [np
759]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.1    sec]  [10101.%]  [np
759]
Solving time (hh:mm:ss.t)  00:00:00.1  + [6.6677 sec]  [6667.7%]  [np
759]
Solving time (hh:mm:ss.t)  00:00:06.7  + [51.855 sec]  [777.70%]  [np
759]
Solving time (hh:mm:ss.t)  00:00:58.6  + [371.43 sec]  [716.29%]  [np
759]
Solving time (hh:mm:ss.t)  00:07:10.0  + [2783.7 sec]  [749.46%]  [np
759]
Solving time (hh:mm:ss.t)  00:53:33.8  + [3300   sec]  [118.54%]  [np
759]
Solving time (hh:mm:ss.t)  01:48:33.8  + [3300   sec]  [100   %]  [np
759]
Solving time (hh:mm:ss.t)  02:43:33.8  + [3300   sec]  [100   %]  [np
759]
Solving time (hh:mm:ss.t)  03:38:33.8  + [86.155 sec]  [2.6107%]  [np
759]
Solving time (hh:mm:ss.t)  03:40:00.0
ATHENA> struct outfile=.history09.str
ATHENA> #
ATHENA> diffus time=90 temp=1200 t.final=800 nitro press=1.00
Solving time (hh:mm:ss.t)  00:00:00.0  + [1e-05  sec]  [100   %]  [np
759]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.0009 sec]  [9900  %]  [np
759]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.1    sec]  [10101.%]  [np
759]
Solving time (hh:mm:ss.t)  00:00:00.1  + [131.54 sec]  [131541%]  [np
759]
Solving time (hh:mm:ss.t)  00:02:11.6  + [942.75 sec]  [716.70%]  [np
759]
Solving time (hh:mm:ss.t)  00:17:54.4  + [675    sec]  [71.598%]  [np
759]
Solving time (hh:mm:ss.t)  00:29:09.4  + [675    sec]  [100   %]  [np
759] *
```

```
Solving time (hh:mm:ss.t)  00:40:24.4  + [1350   sec]  [200   %]  [np
759]
Solving time (hh:mm:ss.t)  01:02:54.4  + [84.375 sec]  [6.25  %]  [np
759]
Solving time (hh:mm:ss.t)  01:04:18.7  + [84.375 sec]  [100   %]  [np
759] *
Solving time (hh:mm:ss.t)  01:05:43.1  + [212.42 sec]  [251.76%]  [np
759]
Solving time (hh:mm:ss.t)  01:09:15.5  + [733.56 sec]  [345.32%]  [np
759]
Solving time (hh:mm:ss.t)  01:21:29.1  + [510.85 sec]  [69.640%]  [np
759]
Solving time (hh:mm:ss.t)  01:30:00.0
ATHENA> struct outfile=.history10.str
ATHENA> #
ATHENA> etch oxide all
ATHENA> struct outfile=.history11.str
ATHENA> # Gate Oxidation, Target Thickness = 100nm
ATHENA> diffus time=15 temp=919.298 dryo2 press=0.785952 hcl.pc=3
Solving time (hh:mm:ss.t)  00:00:00.0  + [1e-05  sec]  [100   %]  [np
726]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.0009 sec]  [9900  %]  [np
726]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.05   sec]  [5050.5%]  [np
726]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.05   sec]  [100   %]  [np
726] *
Solving time (hh:mm:ss.t)  00:00:00.1  + [0.5702 sec]  [1140.5%]  [np
726]
Solving time (hh:mm:ss.t)  00:00:00.6  + [1.9843 sec]  [347.96%]  [np
726]
Solving time (hh:mm:ss.t)  00:00:02.6  + [7.2043 sec]  [363.05%]  [np
726]
Solving time (hh:mm:ss.t)  00:00:09.8  + [42.537 sec]  [590.44%]  [np
726]
Solving time (hh:mm:ss.t)  00:00:52.3  + [225    sec]  [528.94%]  [np
726]
Solving time (hh:mm:ss.t)  00:04:37.3  + [225    sec]  [100   %]  [np
726]
Solving time (hh:mm:ss.t)  00:08:22.3  + [225    sec]  [100   %]  [np
726]
Solving time (hh:mm:ss.t)  00:12:07.3  + [172.60 sec]  [76.712%]  [np
726]
Solving time (hh:mm:ss.t)  00:15:00.0
ATHENA> struct outfile=.history12.str
ATHENA> #
ATHENA> struct outfile=/tmp/deckbMAAhqaibb
ATHENA>
EXTRACT> init inf="/tmp/deckbMAAhqaibb"
EXTRACT> extract name="Gate Oxide Thickness" thickness material="SiO~2"
mat.occno=1  x.val=0.45
Gate Oxide Thickness=100.795 angstroms (0.0100795 um)  X.val=0.45
EXTRACT> #
EXTRACT> quit
```

```
ATHENA> implant boron dose=8.0e11 energy=10 tilt=0 rotation=0 amorph
lat.ratio1=1.0 \
>         lat.ratio2=1.0
ATHENA> struct outfile=.history13.str
ATHENA> #
ATHENA> deposit poly thick=0.2 divisions=10
ATHENA> struct outfile=.history14.str
ATHENA> #
ATHENA> etch poly left p1.x=0.35
ATHENA> struct outfile=.history15.str
ATHENA> #
ATHENA> method compress init.time=0.10 fermi
ATHENA> diffus time=3 temp=900 weto2 press=1.00 hcl.pc=3
Solving time (hh:mm:ss.t)  00:00:00.0  + [1e-05  sec]  [100   %]  [np
923]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.0004 sec]  [4950  %]  [np
923]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.0004 sec]  [100   %]  [np
923] *
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.0062 sec]  [1262.6%]  [np
923]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.0062 sec]  [100   %]  [np
923] *
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.0882 sec]  [1411.2%]  [np
923]
Solving time (hh:mm:ss.t)  00:00:00.1  + [0.0882 sec]  [100   %]  [np
923] *
Solving time (hh:mm:ss.t)  00:00:00.1  + [0.4707 sec]  [533.71%]  [np
923]
Solving time (hh:mm:ss.t)  00:00:00.6  + [1.3236 sec]  [281.18%]  [np
923] *
Solving time (hh:mm:ss.t)  00:00:01.9  + [2.4251 sec]  [183.21%]  [np
923] *
Solving time (hh:mm:ss.t)  00:00:04.4  + [2.4251 sec]  [100   %]  [np
923] *
Solving time (hh:mm:ss.t)  00:00:06.8  + [5.8415 sec]  [240.87%]  [np
923]
Solving time (hh:mm:ss.t)  00:00:12.6  + [5.8415 sec]  [100   %]  [np
923] *
Solving time (hh:mm:ss.t)  00:00:18.5  + [12.572 sec]  [215.23%]  [np
923]
Solving time (hh:mm:ss.t)  00:00:31.0  + [12.572 sec]  [100   %]  [np
923] *
Solving time (hh:mm:ss.t)  00:00:43.6  + [45     sec]  [357.91%]  [np
923]
Solving time (hh:mm:ss.t)  00:01:28.6  + [45     sec]  [100   %]  [np
923]
Solving time (hh:mm:ss.t)  00:02:13.6  + [45     sec]  [100   %]  [np
923]
Solving time (hh:mm:ss.t)  00:02:58.6  + [1.3366 sec]  [2.9702%]  [np
923]
Solving time (hh:mm:ss.t)  00:03:00.0
ATHENA> struct outfile=.history16.str
ATHENA> #
```

```
ATHENA> implant phosphor dose=3e15 energy=20 tilt=0 rotation=0 amorph
lat.ratio1=1.0 \
>         lat.ratio2=1.0
ATHENA> struct outfile=.history17.str
ATHENA> #
ATHENA> deposit oxide thick=0.12 divisions=8
ATHENA> struct outfile=.history18.str
ATHENA> #
ATHENA> etch oxide dry thick=0.12
ATHENA> struct outfile=.history19.str
ATHENA> #
ATHENA> implant arsenic dose=5.0e15 energy=50 tilt=0 rotation=0 amorph
lat.ratio1=1.0 \
>         lat.ratio2=1.0
ATHENA> struct outfile=.history20.str
ATHENA> #
ATHENA> method compress init.time=0.10 fermi
ATHENA> diffus time=1 temp=900 nitro press=1.00
Solving time (hh:mm:ss.t)  00:00:00.0  + [1e-05  sec]  [100   %]  [np
999]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.0009 sec]  [9900  %]  [np
999]
Solving time (hh:mm:ss.t)  00:00:00.0  + [0.1    sec]  [10101.%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:00.1  + [0.1495 sec]  [149.50%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:00.2  + [0.1495 sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:00.4  + [0.2027 sec]  [135.59%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:00.6  + [0.2027 sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:00.8  + [0.3381 sec]  [166.82%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:01.1  + [0.3381 sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:01.4  + [0.3670 sec]  [108.54%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:01.8  + [0.3670 sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:02.2  + [0.7753 sec]  [211.22%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:02.9  + [0.6455 sec]  [83.260%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:03.6  + [0.6455 sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:04.2  + [0.6245 sec]  [96.740%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:04.9  + [0.6245 sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:05.5  + [0.7877 sec]  [126.13%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:06.3  + [0.7877 sec]  [100   %]  [np
999] *
```

```
Solving time (hh:mm:ss.t)  00:00:07.1  + [1.8447 sec]  [234.17%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:08.9  + [1.5832 sec]  [85.821%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:10.5  + [1.5832 sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:12.1  + [2.1678 sec]  [136.92%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:14.2  + [2.1678 sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:16.4  + [1.6712 sec]  [77.093%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:18.1  + [1.6712 sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:19.7  + [4.6114 sec]  [275.92%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:24.4  + [4.6114 sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:29.0  + [3.75   sec]  [81.319%]  [np
999]
Solving time (hh:mm:ss.t)  00:00:32.7  + [3.75   sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:36.5  + [3.75   sec]  [100   %]  [np
999]
Solving time (hh:mm:ss.t)  00:00:40.2  + [3.75   sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:44.0  + [7.5    sec]  [200   %]  [np
999]
Solving time (hh:mm:ss.t)  00:00:51.5  + [7.5    sec]  [100   %]  [np
999] *
Solving time (hh:mm:ss.t)  00:00:59.0  + [0.9806 sec]  [13.075%]  [np
999]
Solving time (hh:mm:ss.t)  00:01:00.0
ATHENA> struct outfile=.history21.str
ATHENA> #
ATHENA> etch oxide left p1.x=0.2
ATHENA> struct outfile=.history22.str
ATHENA> #
ATHENA> deposit alumin thick=0.03 divisions=2
ATHENA> struct outfile=.history23.str
ATHENA> #
ATHENA> etch aluminum right p1.x=0.18
ATHENA> struct outfile=.history24.str
ATHENA> #
ATHENA> struct outfile=/tmp/deckbNAAiqaibb
ATHENA>
EXTRACT> init inf="/tmp/deckbNAAiqaibb"
EXTRACT> extract name="sdxj" xj material="Silicon" mat.occno=1
x.val=0.1 junc.occno=1
sdxj=0.124392 um from top of first Silicon layer  X.val=0.1
EXTRACT> # extract the long chan Vt...
EXTRACT> extract name="n1dvt" 1dvt ntype vb=0.0 qss=1e10 x.val=0.49
n1dvt=0.286724 V  X.val=0.49
EXTRACT> # extract a curve of conductance versus bias....
```

```
EXTRACT> extract start material="Polysilicon" mat.occno=1 bias=0.0
bias.step=0.2 bias.stop=2 x.val=0.45
EXTRACT> extract done name="sheet cond v bias" curve(bias,ldn.conduct
material="Silicon" mat.occno=1  region.occno=1) outfile="extract.dat"
EXTRACT> # extract the N++ regions sheet resistance...
EXTRACT> extract name="n++ sheet rho" sheet.res material="Silicon"
mat.occno=1 x.val=0.05 region.occno=1
n++ sheet rho=20.1831 ohm/square  X.val=0.05
EXTRACT> # extract the sheet rho under the spacer, of the LDD region...
EXTRACT> extract name="ldd sheet rho" sheet.res material="Silicon"
mat.occno=1 x.val=0.3 region.occno=1
ldd sheet rho=44.115 ohm/square  X.val=0.3
EXTRACT> #
EXTRACT> extract name="channel surface conc." surf.conc impurity="Net
Doping"  material="Silicon" mat.occno=1 x.val=0.45
channel surface conc.=1.6151e+16 atoms/cm3  X.val=0.45
EXTRACT> #
EXTRACT> extract name="Vt" ldvt ntype qss=1e10 x.val=0.45
Vt=0.30302 V  X.val=0.45
EXTRACT> #
EXTRACT> quit

ATHENA> struct mirror right
ATHENA> struct outfile=.history25.str
ATHENA> #
ATHENA> electrode name=gate x=0.5 y=0.1

Note:   The electrode was not found on the surface of the structure.
       It was found inside the structure. The material at this
      location is polysilicon. Electrode is set for this region.
      Location is x = 0.500000, y = -0.114866.


ATHENA> struct outfile=.history01.str
ATHENA> #
ATHENA> electrode name=source x=0.1

Note:   Material at chosen location is aluminum. Electrode is set
      for this region. Location is x = 0.100000


ATHENA> struct outfile=.history02.str
ATHENA> #
ATHENA> electrode name=drain  x=0.84

Note:   Material at chosen location is aluminum. Electrode is set
      for this region. Location is x = 0.840000


ATHENA> struct outfile=.history03.str
ATHENA> #
ATHENA> electrode name=substrate backside
ATHENA> struct outfile=.history04.str
ATHENA> structure outfile=finaldevice.str
ATHENA>
```

```
ATHENA>
ATHENA>
ATHENA>
ATHENA> ################################refine the
mesh################################
ATHENA> struct outfile=/tmp/deckbHAAcqaibb
ATHENA> quit

real     2:20.2
user     1:58.3
sys         0.6
118.0u 0.0s 2:19 84% 0+0k 0+0io 0pf+0w
0.0u 0.0s 0:00 0% 0+0k 0+0io 0pf+0w

*** END ***


                                D E V E D I T

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                    devedit 2.6.0.R (Thu Dec 12 12:40:19 PST 2002)
                  libSvcFile 1.8.3 (Sat Dec  7 17:56:58 PST 2002)
                   libsflm 4.14.3 (Sat Dec  7 18:02:49 PST 2002)
                    libSDB 1.4.3 (Tue Dec 10 19:51:05 PST 2002)
                libDW_Version 2.0.0.R (Thu Nov 28 05:44:29 PST 2002)

                    MeshBuild Library based on MeshBuild v1.9.0
   Copyright (c) 1991 Integrated Systems Laboratory, ETH Zurich,
Switzerland

                Executing on host: icfab1  Mon Oct 25 10:36:59 2004


DevEdit> init infile=/tmp/deckbHAAcqaibb !mesh
Mesh in /tmp/deckbHAAcqaibb contained:
      Number of points = 1981
      Number of triangles = 3764
DevEdit> # Set Meshing Parameters
DevEdit> #
DevEdit> base.mesh height=0.1 width=0.1
DevEdit> #
DevEdit> bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
line.straightening=1 align.points when=automatic
DevEdit> #
DevEdit> imp.refine imp="NetDoping" sensitivity=1
DevEdit> imp.refine min.spacing=0.02
DevEdit> #
DevEdit> constr.mesh max.angle=90 max.ratio=300 max.height=1 \
>     max.width=1 min.height=0.0001 min.width=0.0001
DevEdit> #
DevEdit> # Perform mesh operations
DevEdit> #
```
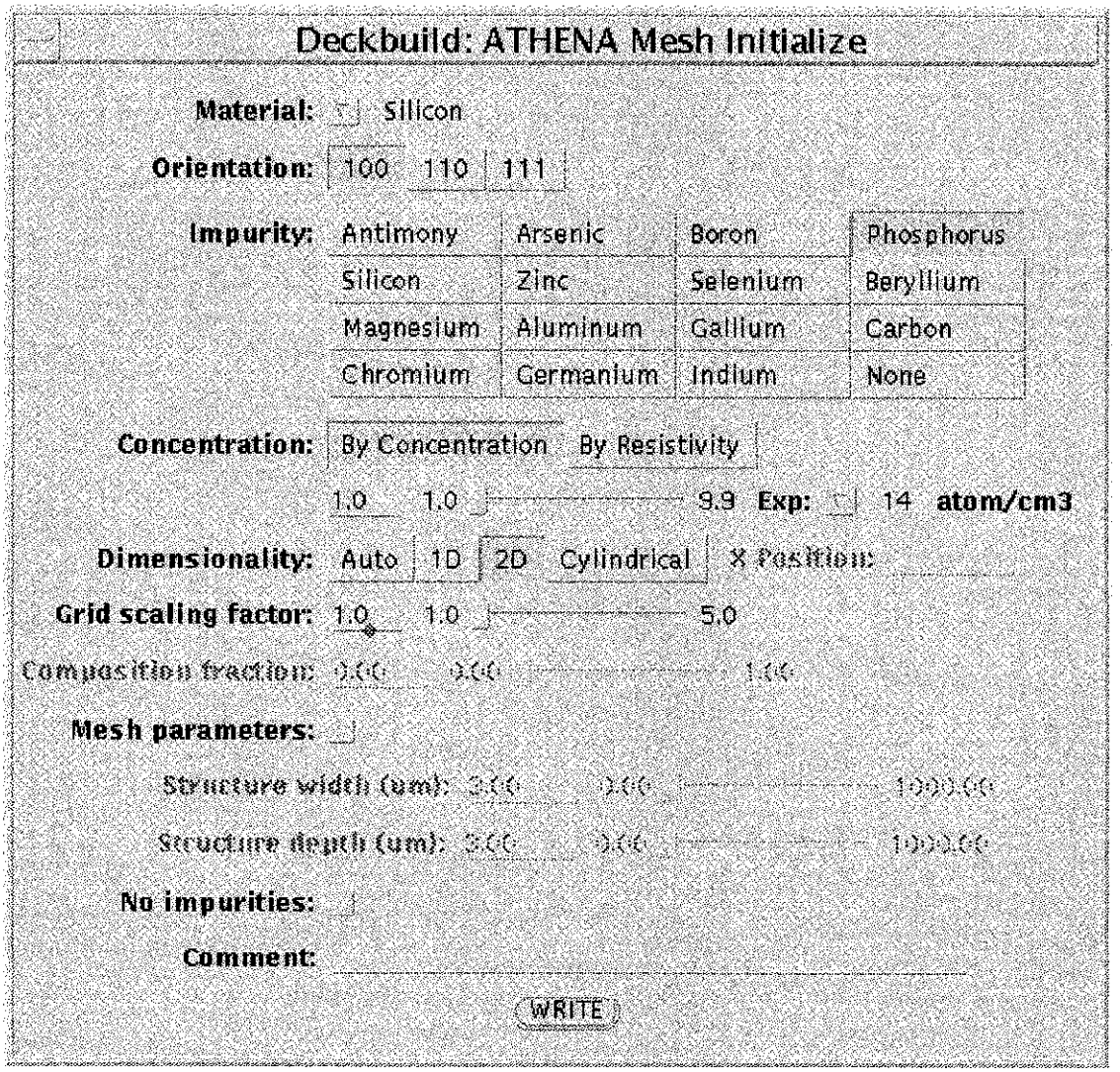

```
DevEdit> Mesh Mode=MeshBuild
Building initial tensor-product mesh...Done
Refining on geometry... Done
Refining on size... Done
Refining on Impurities...Done
Handling green points...Done
Dividing to triangles... Done
Testing Consistency of mesh... Done
Mesh statistics:
      Number of points = 873
      Number of triangles = 1625
      Obtuse triangles 0 (0%)
      Obtuse triangles in Semiconductor 0 (0%)
DevEdit> refine mode=y x1=0.34 y1=0.22 x2=0.65 y2=0.24
Refine Region
Creating list... done.
Refining... done.
Handling green points... done.
Dividing to triangles... done.
DevEdit> refine mode=y x1=0.35 y1=0.22 x2=0.67 y2=0.23
Refine Region
Creating list... done.
Refining... done.
Handling green points... done.
Dividing to triangles... done.
DevEdit> refine mode=both x1=0.65 y1=0.26 x2=0.83 y2=0.34
Refine Region
Creating list... done.
Refining... done.
Handling green points... done.
Dividing to triangles... done.
DevEdit> refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.57
Refine Region
Creating list... done.
Refining... done.
Handling green points... done.
Dividing to triangles... done.
DevEdit> refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.53
Refine Region
Creating list... done.
Refining... done.
Handling green points... done.
Dividing to triangles... done.
DevEdit> refine mode=y x1=0.80 y1=0.34 x2=1.0 y2=0.38
Refine Region
Creating list... done.
Refining... done.
Handling green points... done.
Dividing to triangles... done.
DevEdit> structure outf=refine.str
DevEdit>
DevEdit>
DevEdit> ## tonyplot refine.str
DevEdit>
DevEdit>
```

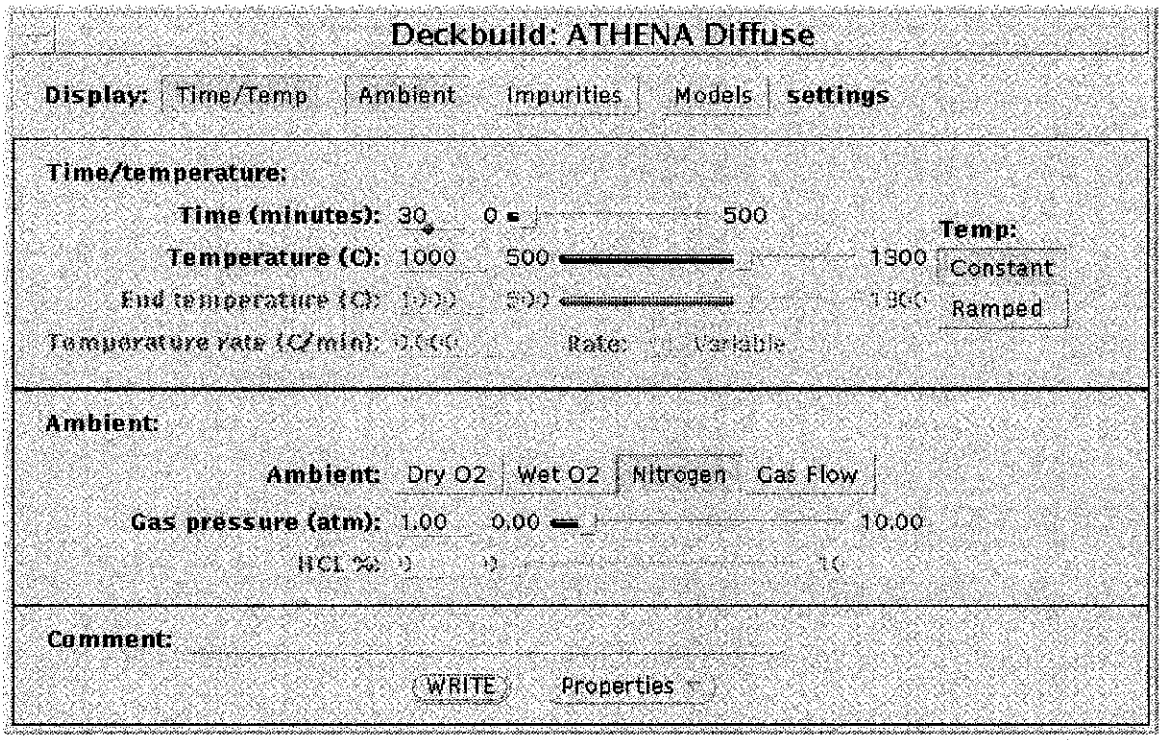
APPENDIX 7

USER INTERFACE TO ASSIST IN GENERATING ATHENA & ATLAS COMMANDS

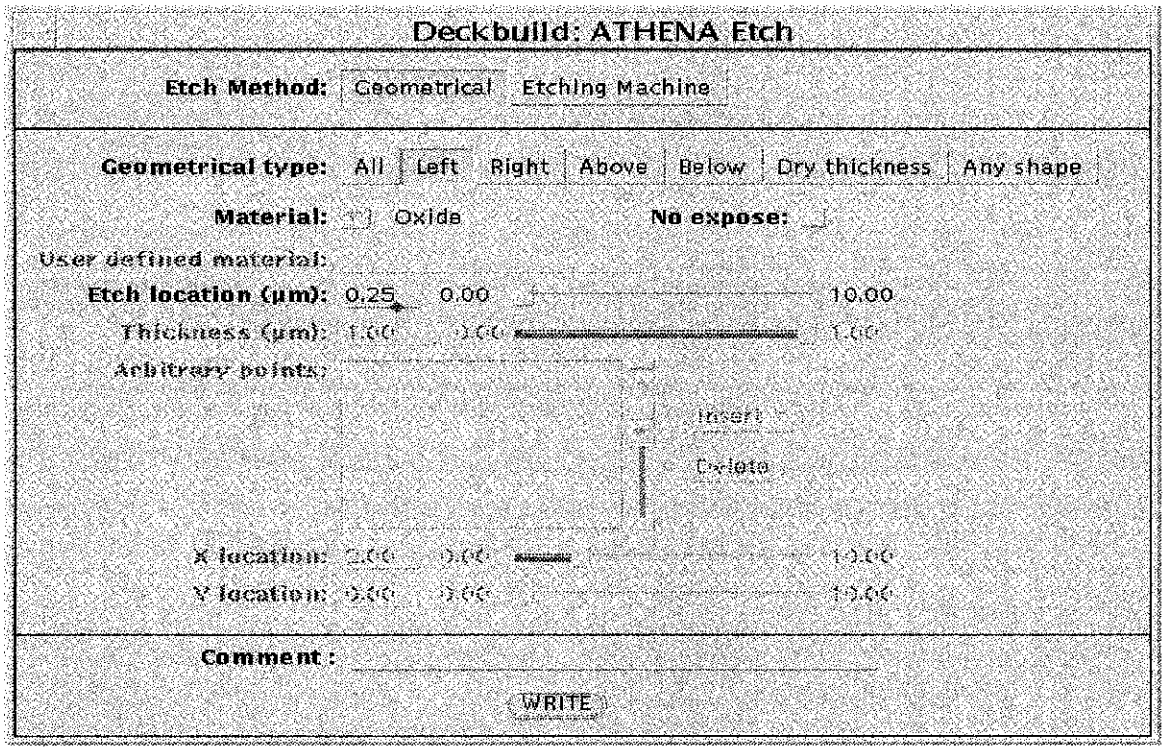
MESH INITIALIZE



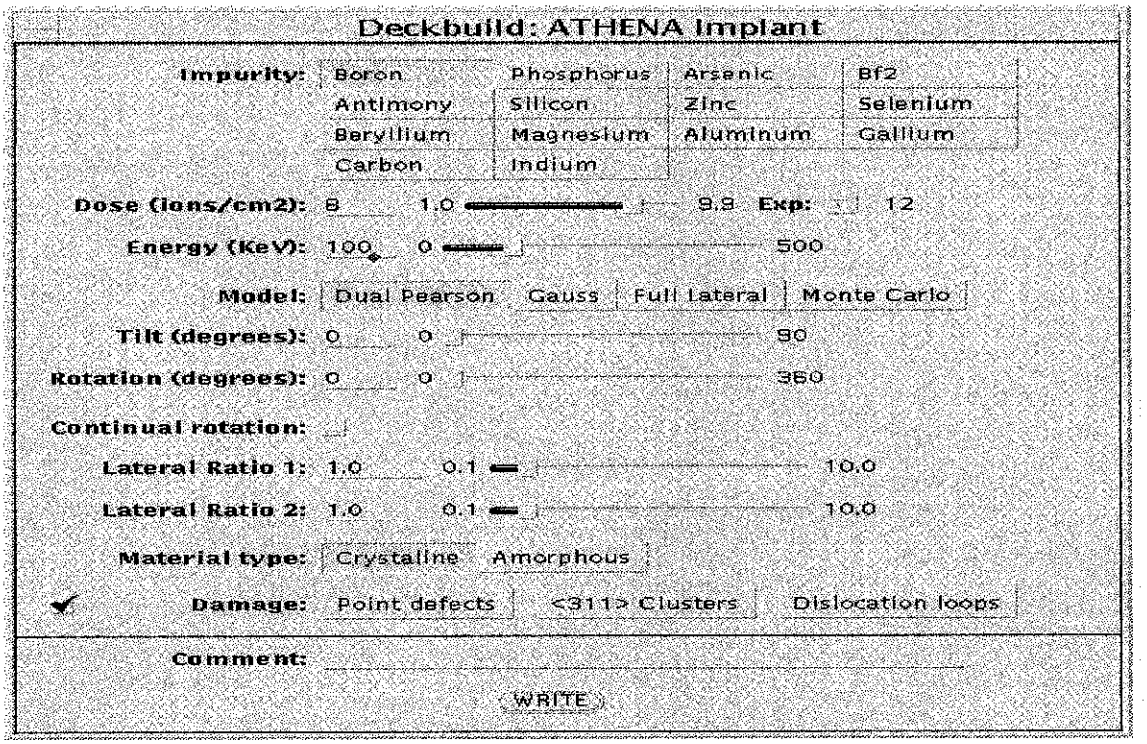
DIFFUSION INTERFACE



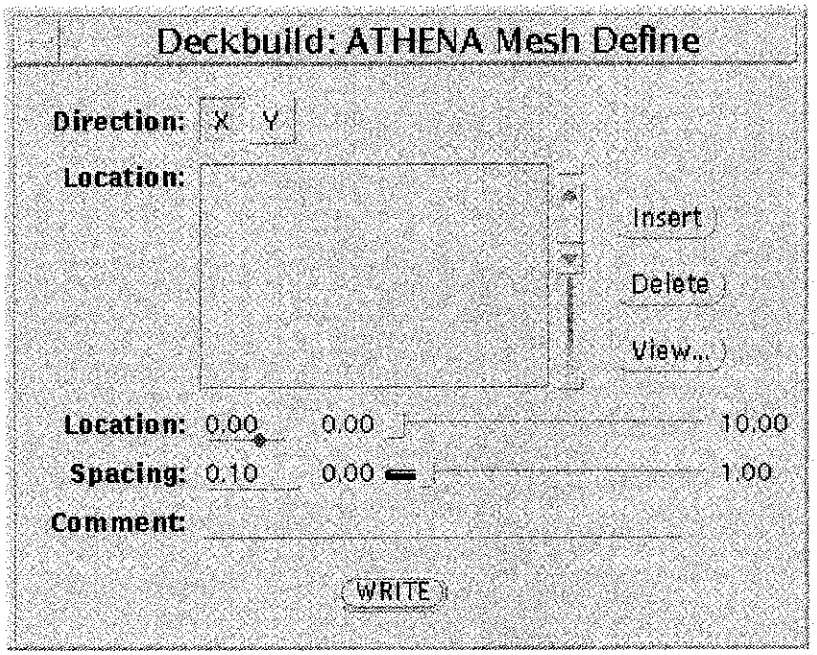
ETCH INTERFACE



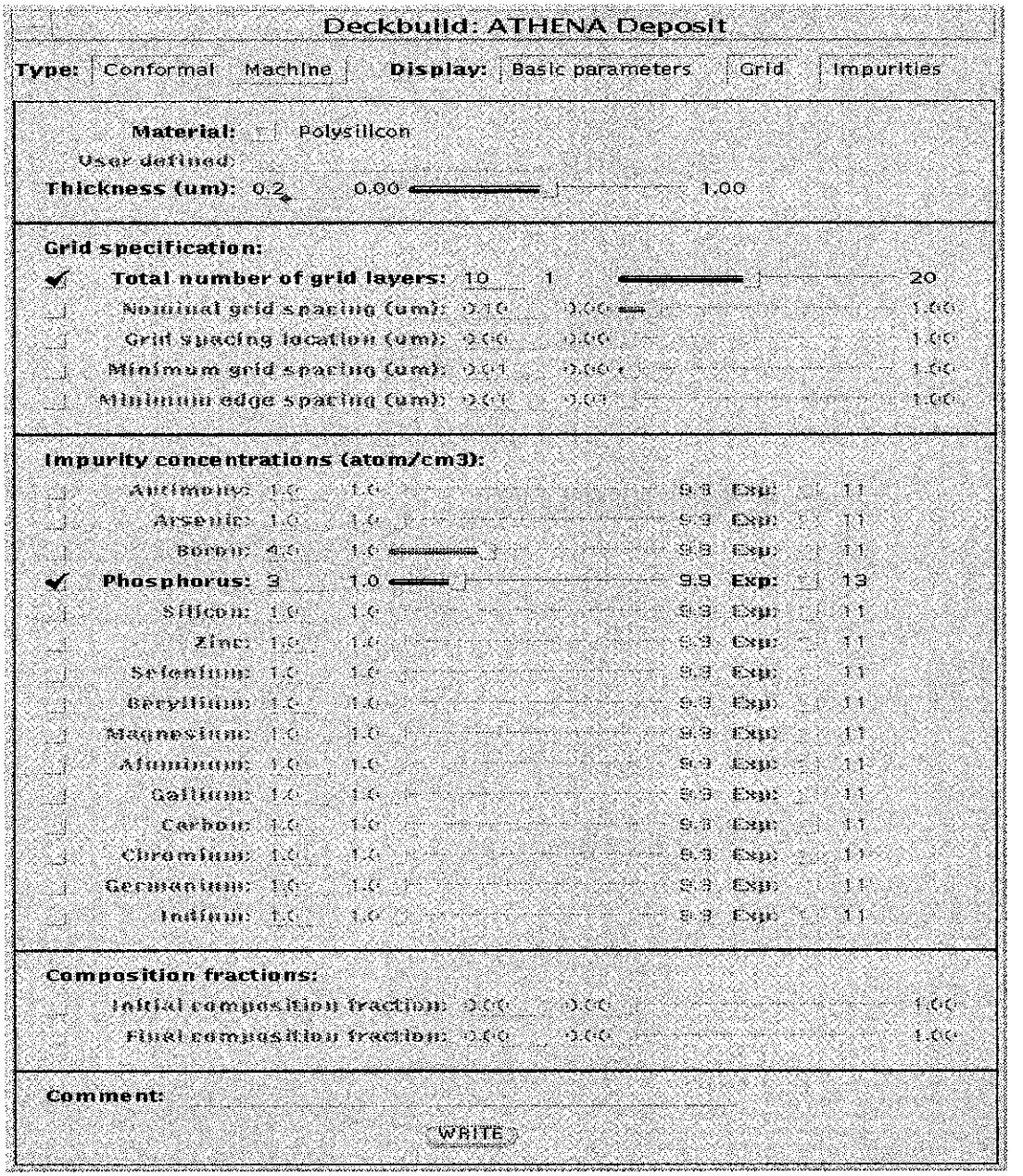
ION IMPLANTATION INTERFACE



MESH DEFINITION



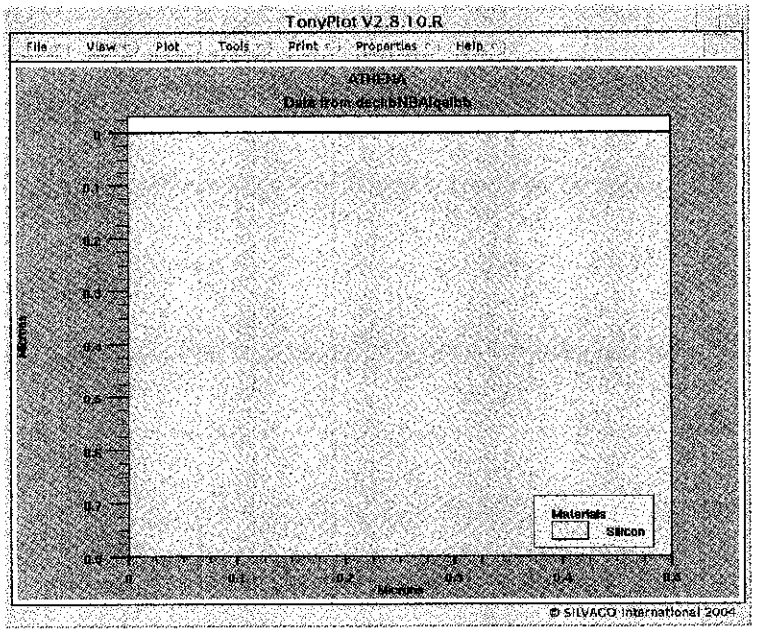
DEPOSITION INTERFACE



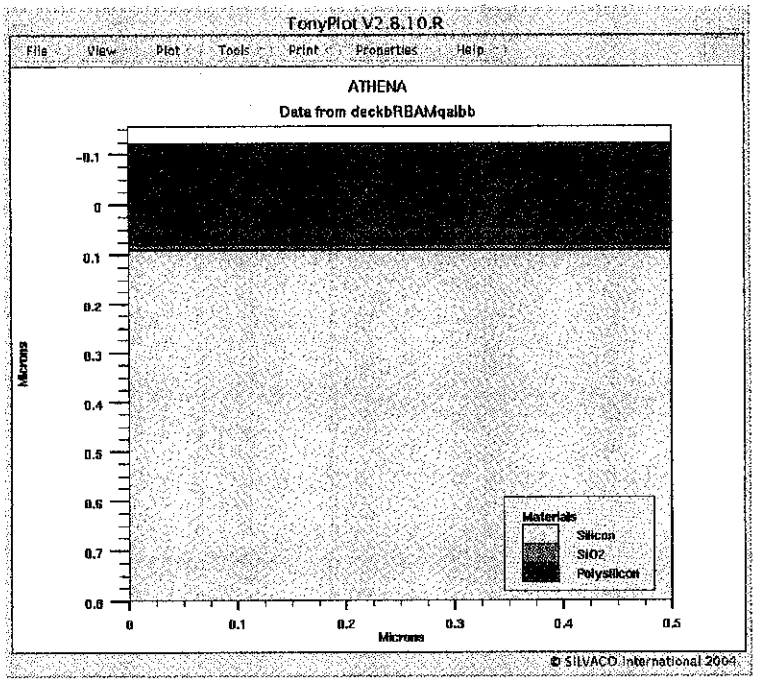
APPENDIX 8

TONYPLOT OUTPUT – DURING PROCESS

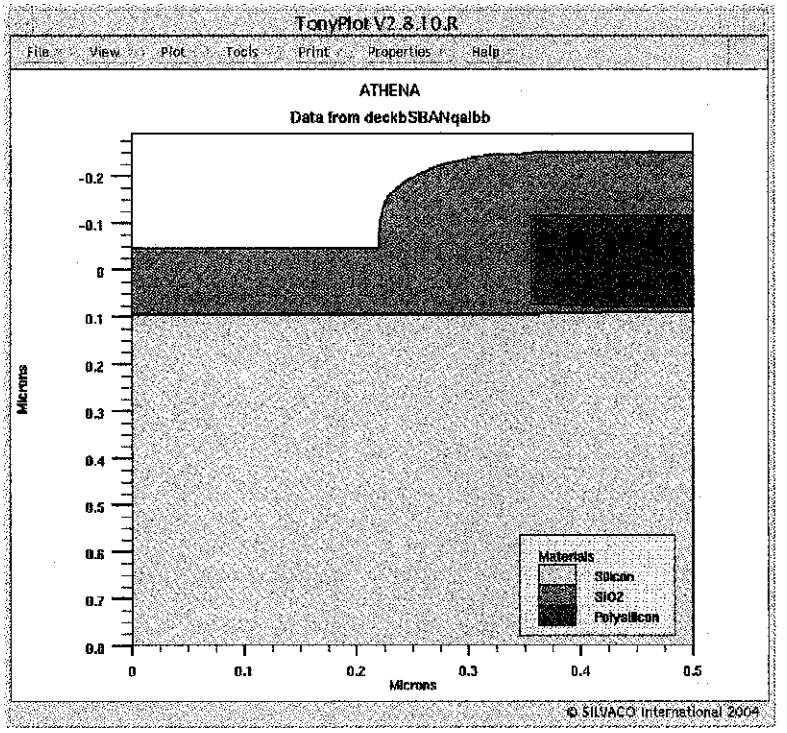
MESH INITIALIZATION



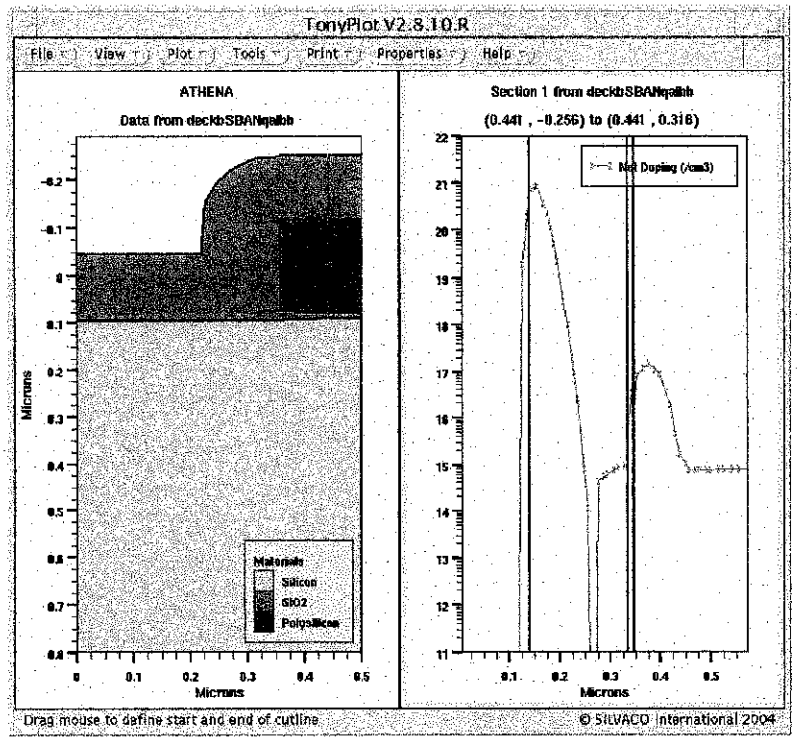
POLYSILICON DEPOSITION



SPACER OXIDE GROWTH



CUTLINE



NMOS DEVICE OPTIMIZATION AND FABRICATION USING ATHENA & ATLAS SIMULATION SOFTWARE

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Dr John Ojur Dennis, Electrical & Electronics Faculty, *Universiti Teknologi Petronas, Malaysia*

Abstract – 0.3 micron size NMOS device has been fabricated and optimized using SILVACO Athena & Atlas process and device simulator. An almost standard NMOS fabrication technology has been used for this purpose. The influence of different fabrication options like channel doping, gate oxide thickness, annealing condition, device scaling, and titled angle implantation has been investigated. Several electrical testing has been carried out on the optimized device like I_{ds}-V_{gs} curve extraction, threshold voltage extraction, off-stage current extraction, breakdown effect, sheet resistance extraction and transient response measurement. Results show that optimized device gives significant improvement in various areas over standard NMOS. The optimization was investigated based on existing 0.5 micron structure by IC MICROSYSTEM.

Index Terms – Threshold voltage, Gate Oxide Thickness, Scaling, Mixed Mode, Transient Response

1. INTRODUCTION

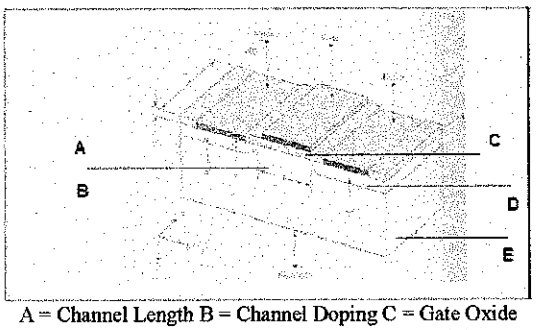
Over many years, experiments have proven that NMOS (N-channel Metal Oxide Semiconductor Field Effect Transistor) perform better than PMOS due to higher drive current, higher mobility, easier to implement scaling technology and low power consumption. However, there is still room for further optimization as the technology trend for miniaturization of NMOS and integrated devices continue to grow. Several objectives have been outlined which include optimizing NMOS by reducing threshold voltage, minimizing gate length, minimizing short channel effect, reducing off-stage leakage, increasing switching speed, minimizing power loss and increasing drain current extraction. The finalized device was tested with mixed-mode inverter circuit to test its functionality and switching speed.

The major concern for the optimization of semiconductor devices will be the cost required to perform experimental analysis using expensive industry standard lab equipments like reactive ion etcher, SEM/EDX, chemical solution, oxidation furnace, ion implanter and high magnification microscope. Thus, it is highly recommended to perform optimization and analysis using simulation. One of the best process and simulation tool is Silvaco Athena & Atlas simulation software. It provides user with various capability in process and electrical testing.

2. LITERATURE REVIEW

This project concentrates on simulating and optimizing NMOS based on existing theory and findings in journals, comparing and suggesting better steps out of existing optimizations. This section will cover all relevant theories behind the simulation aspect, fact and data to support all the findings.

In general, most of the optimization concentrates on the variation of gate oxide thickness, channel doping concentration, total internal resistance, channel length and substrate thickness. Figure 1 shows optimization points in a typical NMOS structure.



A = Channel Length B = Channel Doping C = Gate Oxide Thickness D = Total Resistance E = Substrate Thickness

Figure 1: Optimization Point in a Typical NMOS

Development of gate oxide thickness has been related to the oxidation process. Oxidation has been termed as the ability of a silicon surface to form silicon dioxide. This dielectric layer has various thickness that serve different function at different active region. Table 1 shows the silicon dioxide thickness for various applications. Notice that gate oxide is relatively thin compared to other oxide regions like field oxide and masking oxide. Gate oxide affects a lot of electrical properties like threshold voltage, off-stage leakage and tunneling effect.

Table 1: Silicon Dioxide Thickness and Its Application

Silicon Dioxide Thickness, A	Application
60 –100	Tunneling Gates
100 – 500 (typical)	Gate Oxides, Capacitor dielectrics
200 – 500	LOCOS Pad Oxides
2000 – 5000	Masking Oxides
3000 - 10000	Field Oxides

Gate oxide thickness has reverse relationship with threshold voltage reduction. The gate oxide thickness is a reverse proportion to the gate capacitance. With the gate oxide thickness increasing, the gate oxide capacitance goes down, which means that the gate has less control on the channel and threshold voltage will increase [1,5]. Thus, making thinner gate oxide will reduce the overall threshold significantly. However, this will lead to another problem of off-state leakage. As proven, lowering the threshold voltage will lead to increment of leakage current [2]. Selection of gate oxide thickness must balance between desired turn-on gate voltage and maximum allowable leakage current.

Another fabrication step of concern will be channel doping concentration. Channel doping affects Fermi potential directly. With channel doping concentration increasing, the Fermi potential increases. Fermi potential is the energy at which the probability of occupation by an electron is exactly one-half. Also with the channel doping increasing, more effort is needed to invert the channel. Therefore, with higher channel doping, higher threshold voltage is formed [1, 4].

Threshold voltage can be further improved from the process of channel doping through halo implant. The short channel behavior of both NMOS and PMOS transistors was further enhanced by the introduction of halo implants. The halo implant is a high-angle implant. Since the halo implant uses a high angle it must be done in four 90-degree rotations in the implant tool to ensure both sides of the channel are doped and that transistors oriented in both X and Y directions get doped.

Optimization also can be achieved via minimization of gate length as well. Switching speed of a typical NMOS has been controlled by the total capacitance available. Since time constant, τ ,is related to the total resistance, R, and capacitance, C, by the expression $\tau = RC$, increasing the device speed can be achieved by minimizing its resistive and capacitive components [3,7,8]. Here, the approach is to increase the switching speed by reducing capacitance. The capacitance has direct relationship with area which is **width multiplied by length**:

$$C_{area} = LW.C_1 \quad (1)$$

L is the device length, W is the device width, C_1 stands for device dielectric constant. As the actual dimension of finished devices might be slightly larger or slightly smaller than the expected length, a variation introduced δ on the length and width. The equation 2.4 is complicated by addition of δ to improve capacitance value accuracy and shown in equation 2.5.

$$C_{area} = (L + \delta) \times (W + \delta) \times C_1 \quad (2)$$

It is know that, **width of device** cannot be simply change since it affects the total resistance and device properties. We do not want to complicate device optimization. Thus, minimizing length by reducing gate length is the best solution.

Another optimization performed on NMOS is to minimize the total internal resistance and reduce the power loss. In order to achieve this, calculation for total internal resistance must be well understood. The total resistance in a MOSFET can be categorized into three major parts as shown in figure 2 [6]. Equation 3,4 and 5 give the expression for total internal resistance calculation for a typical NMOS structure.

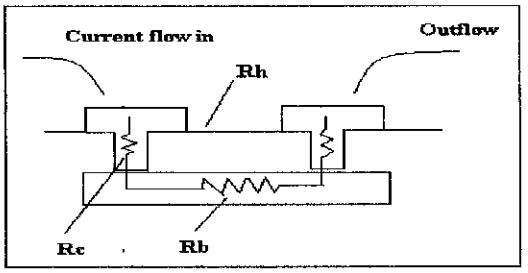


Figure 2: Total Resistance in a Device Structure

$$R = Rb + Rh + Rc \quad (3)$$

$$R = \frac{Lb}{Wb} Pb + 2\frac{Lh}{Wh} Ph + 2\frac{Rc}{Wc} \quad (4)$$

$$R = \frac{Lb+\delta Lb}{Wb+\delta Wb} Pb + 2\frac{Lh+\delta Lh}{Wh+\delta Wh} Ph + 2\frac{Rc}{Wc+\delta Wc} \quad (5)$$

Optimization mentioned earlier on the channel width, gate oxide thickness, channel doping, capacitance and so forth have a very harmonic relationship. The important principle in MOSFET scaling is that channel length and gate oxide thickness must decrease together. Scaling one without the other does not yield adequate performance improvement. Experiment shows that gate oxide thickness and channel length must be scaled together to achieve adequate performance. Normally, for a submicron device with gate length of less than 0.5 micron, the gate oxide thickness featuring silicon dioxide should be fabricated well below 10 nm. However, scaling of gate oxide thickness must take into consideration numerous factors like leakage current, breakdown voltage and punch through effect. Thus, thicker oxide might bring performance degradation in one factor but improve other parameters. Minimal gate oxide might encourage tunneling effect unless better gate material is used like silicon nitride. However, use of silicon nitride in fabrication is far more costly than conventionally growing oxide in silicon.

3. METHODOLOGY

Before starting to simulate a device, detailed understanding of the fabrication and semiconductor characteristics is required.

Next, information is gathered and analyzed in order to choose a device to develop on. This device must meet certain requirements like industry demand, future design requirement, currently still in the optimization stage and has large scale utilization in wafer technology.

After selecting a device to optimize on, identifying its optimization point is vital. Any steps taken to modify the existing structure or properties must bring significant effect on its electrical characteristics. Thus, considerable amount of study must be carried out. For instances, optimization of NMOS must bring significant impact when performing electrical testing like Id –Vgs Curves, Sub-Threshold Slope Extraction, breakdown voltage extraction, drain current, transient response, RF parameters and so forth.

Finally, a working prototype is developed using ATHENA process simulation. This prototype must contain a complete and syntax free source code. Further optimization can be performed by adjusting or altering data available in the source code. ATHENA Process Simulation Framework enables process and integration engineers to develop and optimize semiconductor manufacturing processes. ATHENA provides an easy to use, modular, and extensible platform for simulating ion implantation, diffusion, etching, deposition, lithography and oxidation of semiconductor materials.

ATLAS Device Simulation Framework enables simulation of electrical, optical, and thermal behavior of optimized device. ATLAS provides a physics-based, easy to use, modular, and extensible platform to analyze DC, AC, and time domain responses for all semiconductor based technologies in 2 and 3 dimensions.

Mixed Mode Circuit simulation will be the last part of the project work before minor optimization and advance theoretical studying are conducted. Mixed mode is a circuit simulator that can include elements simulated using device simulation, as well as compact circuit models. It combines different levels of abstraction to simulate small circuits. Mixed mode uses advanced numerical analyses that are efficient and robust for DC, transient, small signal AC and small signal network analysis. Mixed mode can include up to 100 nodes, 300 elements and up to ten numerical simulated ATLAS devices.

4. RESULTS AND DISCUSSION

4.1 ATHENA Output Structure

Figure 3 shows the final output of the fabricated and optimized NMOS device. Dev-Edit Mesh Editor has been used to improve the mesh structure. This is particularly important when the sub-micron device is put under electrical testing. Coarse structure will not allow detail analysis and will generate inappropriate data.

Table 2 shows the whole lists of optimization values compared with the existing figures. Justification over the changes of optimized parameters will be discussed in the following sections.

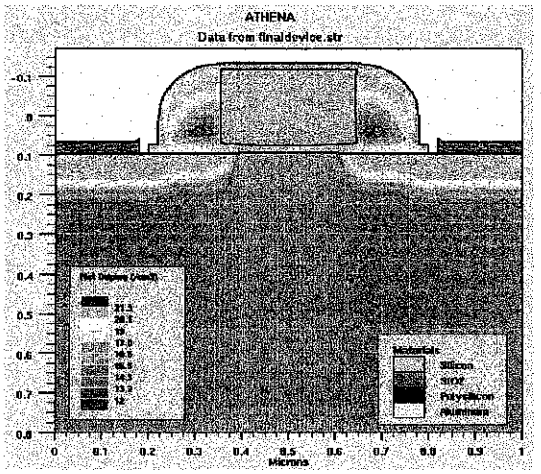


Figure 3: Optimized 0.3 Micron Structure

Table 2: Amendments to Existing Fabrication Steps

	Sample from Silvaco IC Microsystem	Optimized Structure
P-well Implant – Channel Doping	8 x 10^{12} cm^3 boron impurities	8 x 10^{10} cm^3 boron impurities
Gate length	0.5 micron length	0.3 micron length
Gate Oxide Thickness	130nm	100nm
Threshold Voltage Implant	9.5 x 10^{11} cm^3	8 x 10^{11} cm^3
SiGe Layer	Not Applied	Applied as additional progress

4.2 Threshold Voltage Reduction

There are several factors that control the threshold voltage. The first one is channel doping which affects the Fermi potential. With channel doping increasing, the Fermi potential increases. Also, with channel doping increasing, the depletion charge in the channel increases. Thus, more effort is needed to invert the channel. Therefore, by adjusting the channel doping to minimum concentration, the threshold voltage required to deplete the entire channel will be reduced.

Several experiments have been carried out to validate the relationship between channel doping and threshold voltage. Various concentration of channel doping is obtained through ion implantation. After this, threshold voltage is extracted from the Atlas simulation. At the end of the experiment, a finalized channel doping backed with theoretical explanation is chosen as the finalized device process parameters. Table 3 shows experimented channel doping versus acquired threshold voltage.

Channel Doping	Threshold Voltage (v)
8e13 cm^3	1.14603
8e12 cm^3	0.477319
8e11 cm^3	0.263273
5e11 cm^3	0.23712
8e10 cm^3	0.075V – 0.2V

Table 3: Channel Doping versus Threshold Voltage

From the analysis, it's obvious that the threshold voltage reduces to less than 0.2V once channel doping drops to **8e10 cm^3 and below**. This analysis is valid based on previous discussion that Fermi potential drops as channel doping reduces. However, anything lower than that might cause our NMOS to lose its extrinsic properties, thus failing to act as a switching device. With very minimum channel doping, MOSFET cannot create appropriate inversion layer when field effect is excited from gate. Furthermore, very low threshold voltage might cause off-stage leakage to rise exponentially. In other words, it is best not to have low channel doping but end up having very thick gate oxide just to overcome leakage problem.

The second factor is the gate oxide thickness. The gate oxide thickness is in reverse proportion to gate capacitance. With the gate oxide thickness increasing, the gate oxide capacitance goes down, which means the gate has less control on the channel and threshold voltage will increase. Thus, the reverse process is performed by reducing gate oxide thickness to minimize threshold voltage.

However, enormous leakage current has been recorded once oxide thickness is reduced to less than 100nm. An experiment has been conducted to measure overall off-stage leakage current versus gate oxide thickness. The oxidation time and HCI pressure has been kept constant since it's easier to manipulate overall furnace temperature and pressure than varying HCI acidic concentration or time. Figure 4 shows graphical relationship of gate oxide thickness versus off-stage leakage curremt. From the analysis, we can conclude that it is best to maintain gate oxide thickness at 100nm unless other better dielectric materials like silicon nitride is utilized. The exact thickness limit varies for each device and fabrication components.

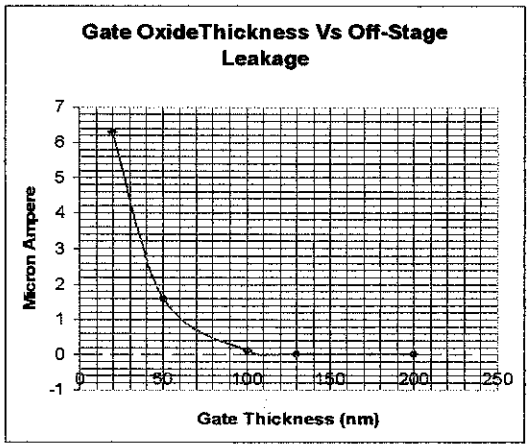


Figure 4: Gate Oxide Thickness versus Off-Stage Leakage

The third factor is the minimization of gate length. The theory behind is related to drain induced barrier lowering (DIBL). DIBL is related to the lowering of source/substrate barrier due to the influence of the drain polarization which increases when gate length decreases. This leads to a decrease of threshold voltage at large drain voltages.

4.3 Gate Scaling

When the dimension of an MOS transistor is reduced, three distinct features are seen in the device's characteristic. First, the drain current is found to increase with the drain voltage beyond pinch off [5]. This is in contrast with the I-V curves of a long channel transistor, where the drain current becomes constant after the pinch off condition is reached. The drain current tends to exhibit soft breakdown that is not seen in long channel. Furthermore, the drain current is not zero at zero gate voltage. Figure 5 shows drain current extraction for 0.3 micron optmized device.

The second distinct short-channel characteristic is seen in the sub-threshold regime. When the gate length minimizes to submicron, the basic shape of the long channel device remains unchanged. However, in the extreme case, where gate length is in nano scale, the output current might not be able to turn off, and the transistor might not be able to function as a switch. However, to date, INTEL has managed to produce efficient MOSFET switching device down to 90nm length [2].

The third feature is the shift of the threshold voltage with the channel length. The threshold voltage decreases with the channel length.

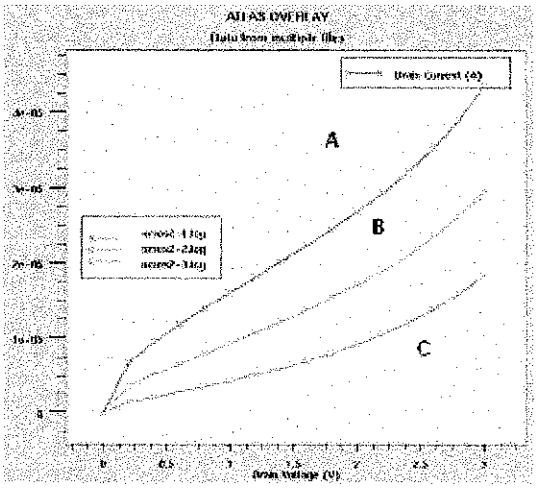


Figure 5: Drain Current Rise Beyond Pinch-off for Optimized Device (0.3 Micron)

4.4 Drain to Source Voltage Extraction (Vds)

The ideal drain voltage to be used is 0.5v because it delivers high current while still in the **ohmic zone (V=IR).** When the curve converges, power loss is very high due to more voltage needed to deliver minimal current. Figure 6 shows optimized drain voltage. If the graph is extrapolated further, the drain current should increase beyond pinch off but at lower rate. This is the characteristic of short-channel transistor. It also exhibit soft breakdown that is not seen in long-channel devices.

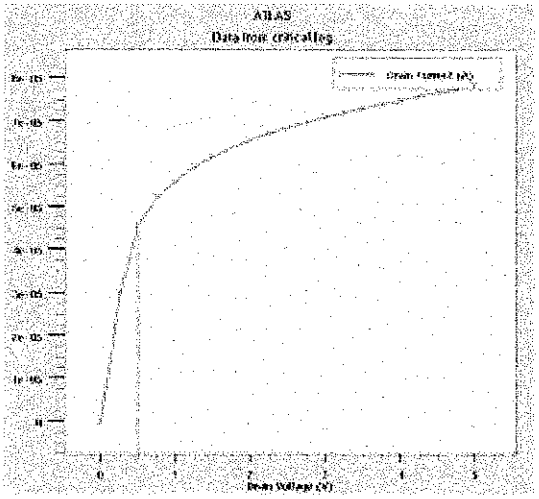


Figure 6: Recommended Drain Voltage Stood at 0.5V

4.5 Off-stage Leakage Current Reduction

As stated previously, less threshold voltage will lead to higher off-state leakage current. This theory is also valid to the optimized device where significant leakage current is collected when threshold voltage is minimized. However, the main concern over here is to ensure that the accumulated leakage current does not exceed the maximum acceptable leakage.

According to the theory, as long as [2]:

$$\frac{Ion}{Ioff \times leakage} > 10^{6} \qquad (6)$$

Then, the device leakage current is deemed acceptable. Here, it's noticed that the turn-off leakage current for the optimized 0.3micron (0.3V threshold voltage) device is **1.2589 x 10^{-12} A/um.** The drain current (I_{on}) extracted at Vds 0.5V (recommended Vds Voltage) stood at 4.5 x 10^{-5} ampere. Thus, $\frac{4.5 \times 10^{-5}\ (ID)}{1.2589 \times 10\text{-}12\ A/um} = 36x10^{6}$, which exceed 10^{6}.As mentioned previously, as long as $\frac{Ion}{Ioff, leakage} > 10^{6}$, the fabricated device is considered as passing minimal leakage tolerance level.

4.6 Analysis on Best Ion Implantation Profile

The channeling effect causes some ions to penetrate deeply into the single-crystal substrate. This can form a "tail" on the normal dopant distribution curve. It is an undesirable dopant profile, which could affect microelectronic device performance. Therefore several methods have been used to minimize this effect.

One way to minimize the channeling effect is ion implantation on a tilted wafer, typically with a tilt angle of 7 degrees. By tilting the wafer, the ions impact with the wafer at an angle and cannot reach the channel. The incident ions will have nuclear collisions right away, and effectively reduce channeling effect.

Another way to solve channeling effect is to diffuse a layer of thin silicon dioxide. Thermally grown silicon dioxide is an amorphous material. The passing implantation ions collide and scatter silicon and oxygen atoms in the screen layer before they enter the single-crystal silicon substrate.

Apart from tilted angle implantation, ions bombard energy has significant impact on the overall quality of impurities in the substrate. Energetic ions penetrate the target, gradually lose their energy through collision with the atoms in the substrate, and eventually rest inside the substrate. Figure 7 shows ion trajectory and projected range.

Generally, the higher the ion energy, the deeper it can penetrate into the substrate. However, even with the same implantation energy, ions do not stop exactly at the same depth in the substrate, because each ion has different collisions with different atoms.

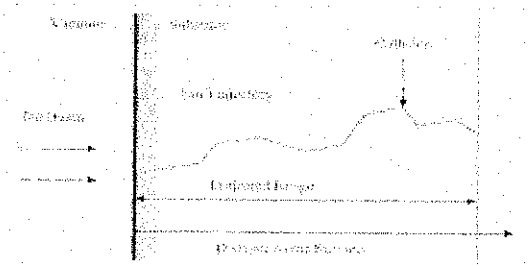


Figure 7: Ion trajectory and projected range

Higher-energy ion beam can penetrate deeper into substrate, and therefore have a longer projected ion range. Since smaller ions have smaller collision cross sections, smaller ions at the same energy can penetrate deeper into substrate and the mask materials.

Projected ion range is an important parameter for ion implantation, because it indicates the ion energy needed for certain dopant junction depth. It also gives information on the required implantation barrier thickness for ion implantation process. Since our substrate thickness is 0.8 micron and effective thickness required could be only 0.5 micron, we use **100 keV** energy to bombard boron into the substrate.

4.7 Junction Breakdown

When a sufficiently large reverse voltage is applied to a p-n junction, the junction breaks down and conducts a very large current. Although the breakdown process is not inherently destructive, the maximum current must be limited by an external circuit to avoid excessive junction heating. Optimized device has proven to achieve higher reliability and durability over excessive current. Figure 8 and 9 show damage after avalanche effect both in the optimized device and existing NMOS.

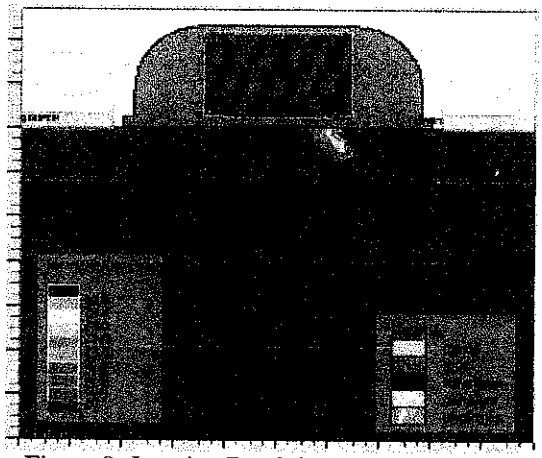


Figure 8: Junction Breakdown Extraction, 0.3 micron Optimized Device

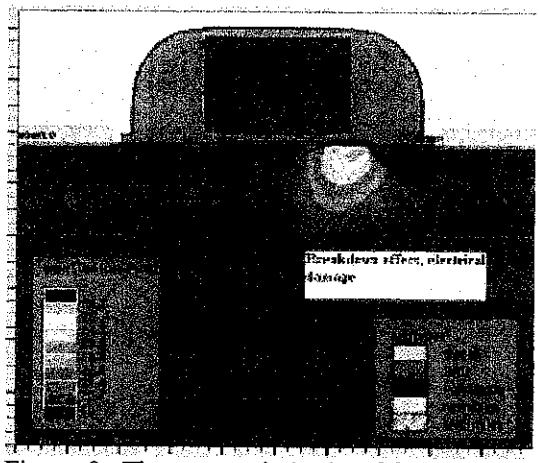


Figure 9: The non-optimized MOSFET shows weak defend against excess of current

4.8 Resistance Calculation

Gate Poly is only about 2 to 3 ohms per square. This low value of resistance works well for gates but useful range of resistance is much more than that. One way of making a region of higher resistance is to implant extra stuff in the poly, discouraging electrons flow or making the poly thinner. Thus, thickness of poly does make a significant role in controlling the overall resistivity. Total resistance calculated theoretically:

$$R = \frac{Lb + \delta Lb}{Wb + \delta Wb} Pb + 2\frac{Lh + \delta Lh}{Wh + \delta Wh} Ph + 2\frac{Rc}{Wc + \delta Wc} \quad (7)$$

$$R = \left(\frac{\left(1.2x10^{-6}\right) + \left(0.05x1.2x10^{-6}\right)}{\left(0.6x10^{-6}\right) + \left(0.05x0.6x10^{-6}\right)} x3.3x10^{3}\Omega - m \right) + 2\left(\frac{23\Omega - micr}{0.03micro} \right.$$

$$R = \left(\frac{1.26x10^{-6}}{0.63x10^{-6}}\right)x3.3x10^{3}\Omega - m + (1533.33\Omega)$$

$R = 6600\ \Omega + 1533.33\Omega$

$R = 8133.33$ ohm

Here we assume that contact resistance will be the depth of source and drain, body resistance covers entire channel length and head resistance to be ignored since we didn't implant additional chunk of poly on top of source/ drain region.

The sheet resistivity is taken from silicon properties of 3.3 x 10^3 ohm –meter. However, the exact value simulated using atlas electrical parameters might vary due to introduction of impurities.

4.9 Transient Response

An experiment has been conducted to test the capability of single device's reaction over a single pulse. The device under test (Optimized Device) has shown rise time and fall time within a pulse size of 1000ps. The fall time from peak 5v until reaching steady state off-voltage is 1.0 e-9 second or equivalent to 1Ghz switching speed when going from high to low voltage. The rise time is recorded at much significant higher speed at 2 e-10 second or 5Ghz. Figure 10 shows recorded transient analysis simulation performed on the optimized device, given a pulse width of 1000 picoseconds and negligible rise and fall time.

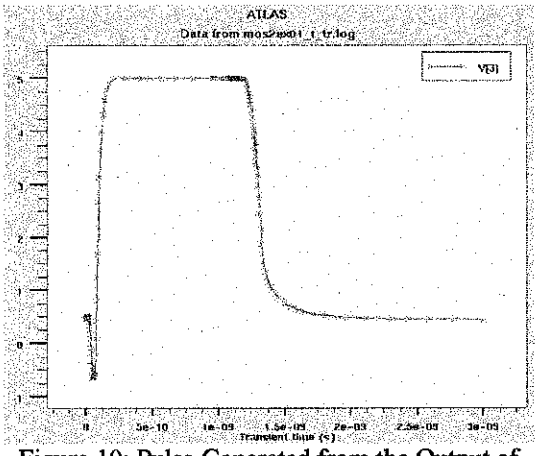


Figure 10: Pulse Generated from the Output of Drain Voltage and The Response Time

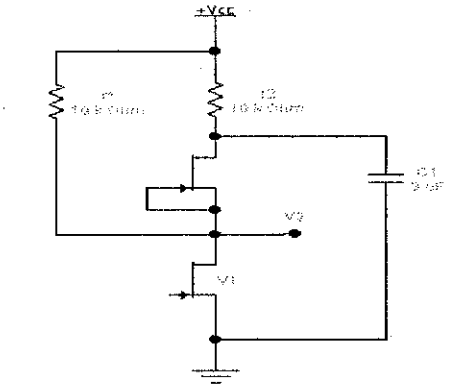


Figure 11: NMOS Inverter Circuit

4.10 Optimization Obtained

This project has successfully optimized several electrical characteristic of NMOS based on the improvement on the fabrication steps and material used. Table 4 gives a comparison of optimization achieved by comparing with existing structure given in sample NMOS recipe from Silvaco IC Microsystem

Table 4: Optimization Achieved

Electrical Parameters	**NMOS recipe from Silvaco IC Microsystem**	**Optimized Device**
Threshold Voltage	0.7V	0.2V
Drain Current Extraction	Pinch off at drain voltage 2V	Rise beyond pinch off, short channel characteristic.
Off-state Leakage	1.258 x 10^{-9} A/um	1.2589 x 10^{-12} A/um
Tilt-angle for Ion Implantation	No tilt angle perform, experienced channeling effect	Reduce channeling effect after tilt angle 7 degrees for ion implantation
Junction Breakdown	Weak against excessive current	Soft breakdown
Transient Response	Less than 1 Ghz Switching Speed	2Ghz Switching Speed, performed on simplified Inverter Circuit

5. CONCLUSIONS

Athena & Atlas is very useful simulation software for various optimizations of different types of semiconductor devices. It is a good starting point for researchers and industry practitioners to actually fabricate a virtual device before transferring the design pattern into costly lab experiment. By using this software, user can minimize the production cost since the effect of varying all the necessary parameters can be analyzed by simulation.

Several objectives have been achieved throughout this project. This includes simulating fabrication of an NMOS device which follows industry fabrication standards ranging from mesh initialization to aluminum contact deposition. Various optimization and testing at the process simulation have been performed such as applying different doping concentration at the channel, varying gate oxide and device size, utilizing different substrate material and varying process parameters. The VLSI fabrication theory has been acquired up to a **sufficient depth level** to perform optimization on the NMOS device which leads to better threshold voltage reduction, drain current extraction, power loss minimization, break down effect reduction, minimization of resistivity, smaller leakage current and faster switching speed. In order to perform optimization, in depth understanding of various capabilities of ATHENA & ATLAS is a must. Most of the optimization is performed by editing the source code used to generate device structure and electrical testing output.

Several changes have been made from the existing structure such as changing of P-well boron impurities from 8 x 10^{12} cm^3 to 8 x 10^{10} cm^3, reducing gate length from 0.5 micron to 0.3 micron, reducing gate oxide thickness from 130 nm to 100 nm, reducing threshold voltage implant from 9.5 x 10^{11} cm^3 to 8 x 10^{11} cm^3 and depositing SiGe layer to improve device mobility. Deposition and optimization of SiGe layer has been treated as future work since its involves further study on the properties of germanium.

As a result of manipulating fabrication recipe, the optimized device has recorded significant improvement over the predecessor. Optimizations include better threshold voltage extraction (0.2v), drain current rise beyond pinch off, better drain current extraction, better device structure after ion implantation due to tilted implantation, lower off-stage leakage current (**1.2589 x 10^{-12} A/um**) and minimization of junction breakdown effect.

Finally, the optimized device has been proven to function properly in an inverter circuit and recorded an encouraging switching speed of 2 GHz. This verifies the functionality of the optimized device.

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