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SIMULATION AND MITIGATION OF POWER QUALITY
DISTURBANCES ON A DISTRIBUTION SYSTEM USING
DVR

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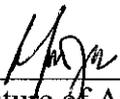
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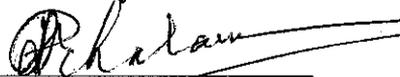
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Permanent address :1, Jalan Melur 5
:Taman Melur,
Jalan Pusing, 31000
Batu Gajah.

Name of Supervisor
Prof. Dr. P.A VENKATACHALAM

Date : 7 MARCH 2005

Date : 7 MARCH 2005

Prof. Dr. P.A. Venkatachalam
Professor
Electrical & Electronic Engineering
Academic Block No. 22
Universiti Teknologi PETRONAS
Bandar Seri Iskandar
31750 Tronoh, Perak Darul Ridzuan, MALAYSIA.

UNIVERSITI TEKNOLOGI PETRONAS

Approval by Supervisor (s)

The undersigned certify that they have read, and recommend to The Postgraduate Studies Programme for acceptance, a thesis entitled "Simulation and Mitigation of Power Quality Disturbances on a Distribution System using DVR" submitted by K.Chandrasekaran for the fulfilment of the requirements for the degree of Master's in Science in Electrical and Electronics Engineering.

Date : 7 MARCH 2005

Signature

:



Main Supervisor

:

Date

: 7/3/05

Prof. Dr. P.A. Venkatachalam
Professor

Co-Supervisor 1

:

Electrical & Electronic Engineering
Academic Block No. 22

Co-Supervisor 2

:

Universiti Teknologi PETRONAS
Bandar Seri Iskandar
31750 Tronoh, Perak Darul Ridzuan, MALAYSIA.

UNIVERSITI TEKNOLOGI PETRONAS
SIMULATION AND MITIGATION OF POWER QUALITY DISTURBANCES ON A
DISTRIBUTION SYSTEM USING DVR

By

K.CHANDRASEKARAN

A THESIS

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DEGREE OF MASTERS OF SCIENCE IN

ELECTRICAL AND ELECTRONICS ENGINEERING

BANDAR SERI ISKANDAR,

PERAK

MARCH 2005

DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UTP or other institutions.

Signature :  _____

Name : K.CHANDRASEKARAN

Date : 7 MARCH 2005

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K.Chandrasekaran (G2010044)

SIMULATION AND MITIGATION OF POWER QUALITY DISTURBANCES ON A DISTRIBUTION SYSTEM USING DVR

BY

K.Chandrasekaran

ABSTRACT

Voltage sag is the most important power quality problem faced by many industrial customers. Equipment such as process controllers, programmable logic controllers, adjustable speed drives, robotics, etc used in modern industrial plants are actually becoming more sensitive to voltage sags. Voltage sags are normally described by the magnitude variation and duration, and also characterized by unbalance, non-sinusoidal wave shape and phase angle shift.

One of the most common mitigation solution is installing uninterrupted power supply (UPS). To meet the demand for more efficient mitigation solution, the Dynamic Voltage Restorer (DVR) will be deployed. When a fault occurs, either at the high voltage source end or at the consumer end, the DVR injects active and reactive power for the restoration of the voltage sags in the network.

This thesis presents the power quality problems faced by the power distribution systems in general and then concentrates on analyzing an important and specific distribution system in particular. A dynamic voltage restorer (DVR) is connected on the 11KV of an utility feeder to Ipoh hospital, in reducing the voltage sags, that affect the operation of sensitive loads to the hospital.

Case studies were conducted at four industrial sites (Hitachi plant and Nihoncanpack at Bemban, Filrex at Bercham and Ipoh Hospital) by monitoring and taking physical sag measurements for a period of one month. The real time measurements were carried out to

identify the types power quality disturbances that exists in the various plants before providing the custom power device as a mitigation tool.

The Ipoh Hospital is taken for a special case study since the hospital has to maintain high quality power supply to the medical equipments such as CT Scan, Magnetic Resonance Imaging (MRI), Magnetic Scanner, X-ray unit, and other life saving equipment.

For simulation study, PSS/ADEPT and PSCAD/EMTDC software packages were used in modeling of the power distribution system. With the PSS/ADEPT simulation tool, the voltage severity is studied by introducing different types of faults. The PSCAD/EMTDC is a graphical user interface simulation tool to simulate sag waveforms for various types of faults. A DVR was modeled using the PSCAD/EMTDC software and simulated for voltage sag mitigation. The recorded waveform shows the DVR as a potential custom power solution provider. The DVR can improve the overall voltage regulation. The results obtained from the DVR show that the voltage sags are reduced by bringing the supply voltage level to 100%. The simulated results were verified for selected faults theoretically.

SIMULATION AND MITIGATION OF POWER QUALITY DISTURBANCES ON A DISTRIBUTION SYSTEM USING DVR

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ABSTRAK

“Enapan voltan” merupakan satu masalah kritikal yang sedang dihadapi oleh kebanyakan industri. Peralatan seperti (pengawal proses, pengawal bolehalih cara logik, pemula laju bolehubah dan robotik) yang digunakan di industri moden menjadi semakin sensitif kepada “enapan voltan” kerana peralatan kini telah menjadi semakin kompleks dan juga disambungkan ke proses-proses yang canggih. “Enapan voltan” selalu dijelaskan dengan menggunakan variasi magnitud dan tempoh. Di samping kuantiti ini, “sags” juga boleh dikategorikan dengan ketidakseimbangan, “bentuk gelombang tidak simul” dan “anjakan sudut fasa”.

Terdapat beberapa penyelesaian yang membawa kepada mitigasi kesan voltaj “sags”. Pemasangan bekalan kuasa tidak terganggu (Uninterrupted Power Supply, UPS) merupakan satu penyelesaian paling am. Akan tetapi, disebabkan oleh permintaan yang semakin meningkat untuk penyelesaian yang membawa kepada mitigasi yang lebih efisien, pemulih voltan dinamik (Dynamic Voltage Restorer, DVR) telah dicipta. Ini adalah sejenis “converter” berasaskan kuasa elektronik. Bila berlaku kesilapan, DVR akan mengeluarkan kuasa aktif dan reaktif untuk memulihkan voltaj “sags”.

Dalam tesis ini, dibincangkan cara-cara yang mungkin dapat mengurangkan voltaj “sags”. Empat kes kajian telah dijalankan (Hitachi plant dan Nihoncanpack diBemban, Filrex diBercham dan Hospital Ipoh) dengan memantau setiap kes selama sebulan untuk mengenalpasti jenis masalah kualiti kuasa yang bertindakbalas jika berlaku gangguan kualiti kuasa. Satu kes kajian menarik telah dijalankan pada rangkaian pengagihan (distribution network) Hospital Ipoh untuk meramalkan bagaimana voltaj “sags” akan

membawa masalah kepada peralatan perubatan seperti “CT Scan”, “Magnetic Resonance Imaging” , “Magnetic Scanner” dan X-ray. Perisian PSS/ADEPT dan PSCAD telah digunakan untuk memodalkan system pengagihan komponen dan juga simulasi voltaj “sags” disebabkan oleh pelbagai jenis kerosakan. Dengan PSS/ADEPT, satu titik dipilih dari rangkaian dan kesan voltaj “sags” ditentukan dengan mengenakan kerosakan pada titik yang dipilih.

Satu simulasi dibuat dengan PSCAD yang menunjukkan gelombang (waveform). DVR telah dimodal dan disimulasi dalam operasi, untuk memulihkan regulasi voltan. Keputusan simulasi ini telah dianalisa dan dibandingkan dengan teori.

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CHAPTER 1
INTRODUCTION

CHAPTER 1

INTRODUCTION

1.1 Background

Customers with highly sensitive computerized equipment such as variable speed drives or robots, automated production lines or machine tools, programmable logic controllers, power supply in computers and certain medical equipments desire high levels of power quality to ensure the proper and continued operation of their equipment and processes. The quality of power is judged by the ability to maintain voltage and current signals in power systems at constant amplitude, a nearly sinusoidal shape and a constant fundamental frequency at all times.

Power quality disturbances are normally caused by power system faults, incipient faults, capacitor switching events, large non-linear load switching events and transformer inrush current. The major power quality phenomena include voltage sag, harmonics, switching transients, lightning strike transients, voltage interruptions and voltage flicker. Interruptions occur when a protective device actually interrupts the circuit serving a particular customer. This will occur when there is a fault on that circuit. Voltage sags occur during faults in a wide part of the power system. Compared to interruptions, voltage sags occur much more frequently. The Dynamic Voltage Restorer (DVR) has been proposed as a solution to solve the voltage sag problem on a selected distribution system.

1.2 Voltage Sags

1.2.1 Definition

A voltage sag is a sudden reduction or decrease in rms voltage between 0.1pu and 0.9pu with a duration between 0.5 cycle and one minute at a point in an electrical power system due to a short circuit fault, motor starting, or the switching of a large load [1,2]. Figure 1.1

shows a measured voltage sag in one phase. Voltage disturbances lasting less than (0.04sec) are regarded as transient.

1.2.2 Voltage magnitude events

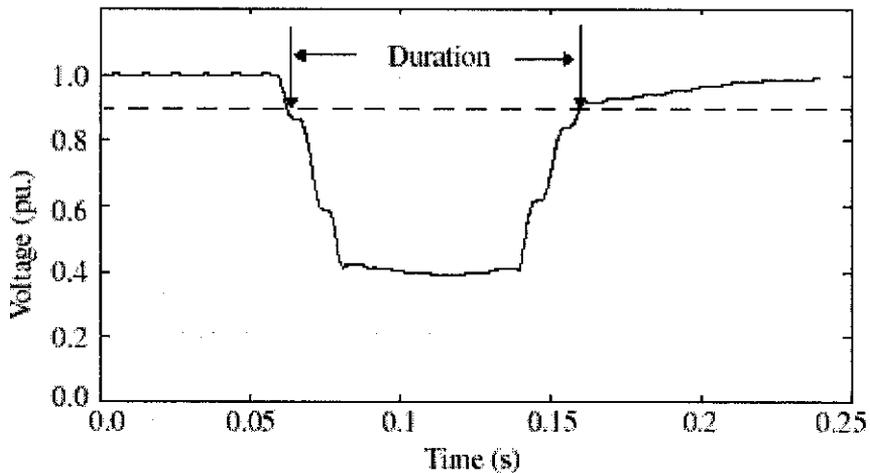


Figure 1.1: Voltage sag
(Courtesy of Lidonglic, Three-phase Unbalance of Voltage sags)

Interruption is a condition in which the voltage at the supply terminals is close to zero. Close to zero by the Institution of Electrical and Electronics Engineers (IEEE) means as “lower than 10%” of the nominal voltage [1, 2].

Instantaneous interruption is with duration between 0.04 sec and 0.5 sec [IEEE Std. 1159], [IEEE Std. 1250]. Momentary interruption is an interruption with duration between 0.5 and 3 seconds. Temporary interruption is an interruption with duration between 3 seconds and 60 seconds [2].

Sustained interruption is an interruption with duration longer than 1 minute. Under voltage is a voltage magnitude event with a magnitude less than the nominal rms voltage, and duration exceeding 1 minute [IEEE Std. 1159].

Swell is a voltage magnitude event with a magnitude above 110% of the nominal voltage, and duration between 0.04 seconds and 1 minute [IEEE Std. 1159].

A voltage sag is regarded as occurring on a 3-phase system if at least one phase is affected by the disturbance.

1.2.3 Origin of voltage sags

Voltage sags and short interruptions are mainly caused by phenomena leading to high currents, which in turn causes a voltage drop across the network impedances with a magnitude which decreases in proportion to the electrical distances of the observation point from the source of the disturbance. Voltage sags and short interruptions have various causes:

1. Faults on transmission Extra High Voltage (EHV) and distribution High Voltage (HV) and Low Voltage (LV) networks.
2. A healthy feeder affected by a fault on adjacent feeder connected to a common bus. The duration of sag is usually dictated by the operating time of the protective devices.
3. The isolation of faults by circuit breakers or fuses will produce interruptions (long or short) for users fed by the faulty section of the power system.
4. Short interruptions are often the result of the operation of automated systems on the network such as fast and/or slow automatic reclosers, or operation of off-load tap changers.
5. Long interruptions are the result of isolation of a permanent fault (requiring repair or replacement of component before re-energizing).
6. Overhead networks, which are exposed to bad weather, are subject to voltage sags than underground network.

7. An underground feeder connected to the same bus bar system as overhead or mixed networks will suffer voltage sags which are due to the faults affecting overhead lines.
8. Starting up large ac motors can cause voltage sags as shown in Figure 1.2.

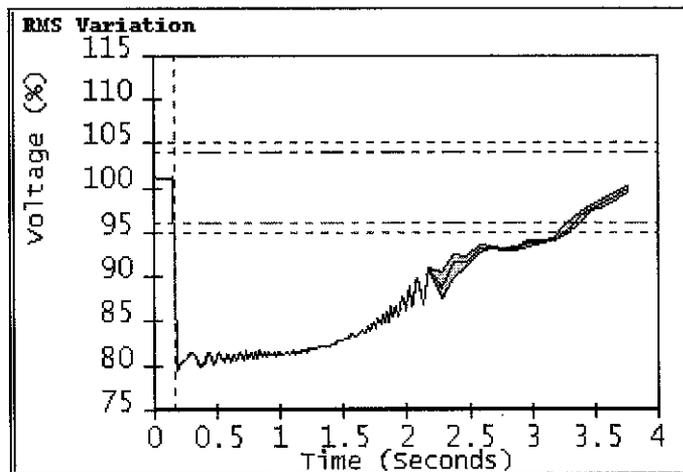


Figure 1.2: Voltage sag caused by motor starting
(Courtesy of MS 1533: 2002, Malaysian Standards)

The characteristics of the corresponding sag depend on the characteristics of the induction motor (size, starting method, load, etc) and the strength of the system at the point where the motor is connected.

1.3 Objectives of the thesis

The research undertaken in this project was to evaluate the effectiveness of a Dynamic Voltage Restorer (DVR) to mitigate the voltage sags on a selected power distribution system. The dynamics and accuracy of the DVR is highly dependent on the control strategy. Hence the design of the control system will play a very important role in the overall performance of the DVR. The propose DVR is connected at the 11KV of an utility feeder to the Ipoh hospital distribution system. Real time monitoring of power quality disturbances were carried out to identify desirability of providing the custom power device

as a mitigation tool. The effectiveness is evaluated under various fault conditions, the distribution system is likely to face. In this thesis, the following task has been completed and will be highlighted.

1. Four case studies have been done by monitoring the power quality disturbances that exist in the plant for a period of one month for each case.
2. Simulation on PSS/ADEPT software: used for accurate steady-state prediction of voltage magnitudes for load flow simulation and for balanced and unbalanced fault conditions. For fault calculations, a point is chosen on the network and the voltage sag severity is determined by introducing faults on the chosen point. The Ipoh Hospital distribution network has been modeled and simulated to obtain the magnitude of voltage sags for various faults at the respective nodes. There is no provision to model and simulate a DVR using this software.
3. Simulation on PSCAD/EMTDC software: to demonstrate the use of the detail DVR schematic design, the Ipoh Hospital distribution network has been developed using the PSCAD simulation program. Simulations are run and from the simulation results, studies are made about the performance of the DVR. The generated waveform shows voltage prediction with DVR in operation to improve the voltage regulation.

From the simulation results, the following areas have been looked into to assess the compensation capability of the DVR design:

1. Steady State Performance: To study the steady state conditions with DVR compensation, such as the percentage of magnitude compensation achieved.

2. Transient Analysis: For the purpose of transient analysis of the control system, the dynamic performance of the DVR in encountering sudden changes in the system will be studied.

1.4 Outline of the thesis

This thesis presents the power quality problems faced by power distribution systems in general and then concentrates analyzing an important and specific distribution system. Simulation studies are done using PSCAD and PSS/ADEPT software. PSS/ADEPT has been used for balanced and unbalanced fault analysis. A Dynamic Voltage Restorer (DVR) has been modeled in PSCAD to evaluate the effectiveness provided on the utility feeder to the Ipoh hospital in reducing the voltage sag. Both software are commercially available, have high accuracy and capabilities with their functions and limitations.

Chapter 2 provide brief overview of different power quality phenomena, power quality disturbances, terminology and power quality indices. It also covers power quality standards. The main interest in this thesis is voltage sags.

Chapter 3 discusses the evaluation of the PSS/ADEPT and PSCAD/EMTDC software packages technically. How the system components have been modeled in PSS/ADEPT for balanced and unbalanced fault analysis and load flow under normal conditions. The modeling procedure adopted in the PSS/ADEPT for modeling transformers of different vector groups and cables. The methodology adopted in EMTDC for selecting time step for integration, for solving algebraic and differential equations.

Chapter 4 discusses case studies done at four industrial sites by monitoring are presented. The distribution system that supplies power to Ipoh Hospital is taken for the case study. The reason for selecting this case is to analyze how the voltage sag magnitude affects many life saving equipment and devices.

Chapter 5 explains the mathematical analysis and the common custom power devices application such as Dynamic Voltage Restorer (DVR), solid state transfer switches and distribution static compensator.

Chapter 6 presents the different techniques in the design of the distribution system. How improvements against voltage sags and short interruptions can be achieved by using custom power devices such as Uninterrupted Power Supply (UPS), Solid State Transfer Switches (SSTS) and Distribution Static Compensator (D-Stat Com).

In chapter 7 the modeling and simulation of the Ipoh Hospital distribution network using the PSS/ADEPT and PSCAD/EMTDC software packages and the results are discussed.

Chapter 8 provides a summary of the thesis and the conclusion from the performed work as well as some ideas for future research work.

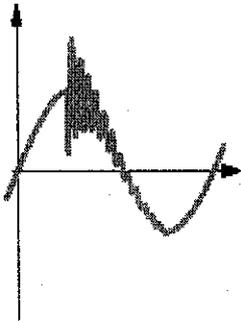
CHAPTER 2
POWER QUALITY

CHAPTER 2

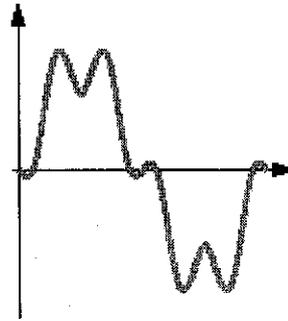
POWER QUALITY

2.1 Types of voltage disturbances

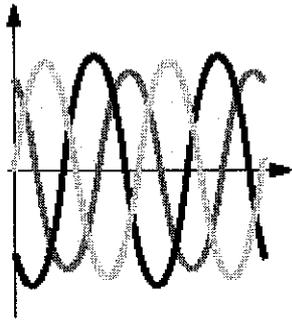
Different types of voltage disturbances are shown in Figure 2.1.



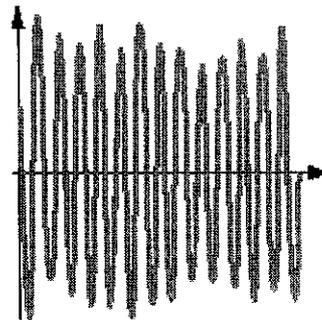
(a) Over voltage



(b) Harmonics



(c) Unbalance



(d) Voltage fluctuations

Figure 2.1: Types of voltage disturbances
(Courtesy of Philippe Ferracci, Power Quality Notes: no. 199, ECT 199(e) October 2001)

2.1.1 Frequency

The nominal frequency of the supply voltage is 50Hz. Under normal operating conditions, the permissible variation in frequency range is $\pm 1\%$. The causes of frequency variation:

poor speed regulation of local generation, faults on the bulk power system, large block of load being disconnected and disconnecting a large source of generation.

2.1.2 Over voltage

Figure 2.1(a) is an over voltage waveform. Over voltage is a voltage magnitude event with a magnitude greater than 110 percent at the power frequency nominal voltage for a duration longer than 1 minute [IEEE Std.1159].

Over voltage are of four types:

1. Temporary over voltage can appear due to an insulation failure between phase and earth or between phase and phase in insulated neutral or impedance earthed neutral system. The voltages of the healthy phases to earth may reach the line voltage levels. This phenomenon is called arcing ground fault. Overvoltage on LV installations may come from HV installations via the earth of the High voltage / Low voltage (HV/LV) substation.
2. Ferro resonance over voltage is a rare non-linear oscillatory phenomenon that occurs under a single line-to-ground fault condition which is produced in a circuit containing a capacitor and an inductor.
3. Switching over voltages is produced by the switching on and off of unloaded transformer, capacitor banks, no-load lines or cables [3].
4. Lightning over voltage is a natural phenomenon occurring during storms [4]. Normally aerial earthwire is used to shield outdoor substation as well as power lines on lattice structures.

The impacts of overvoltage vary according to the period of application, repetivity and magnitude. Generally, causing dielectric breakdown to equipment, degradation of equipment through ageing. Lightning can cause thermal stress (fire). Hence, it is important

to periodically check the effectiveness of system grounding. Substation neutral grounding resistance value not exceeding 3 ohms and lattice structures not exceeding 10 ohms.

2.1.3 Harmonics and interharmonics

Harmonics in power circuits are frequencies that are integer multiples of a fundamental frequency generated by non-linear electrical and electronic equipment [3,4]. The fundamental frequency combines with the harmonic sine waves to form repetitive sinusoidal distorted wave shapes as shown in Figure 2.1(b). Harmonics produced by various non-linear loads are shown in Figure 2.2, where total harmonic distortion (THD) for data processing load is 115%.

Harmonic voltages occur across network impedances resulting in distorted voltage which can disturb the operation of other users connected to the same source. The classification of harmonics with the fundamental frequency at 50 Hz is given in the Table 2.1. In three-phase sequences, the positive sequence voltages will produce positive direction torque for induction motors. The negative sequence currents make voltages that produce negative torque, which has a tendency to make motors run backwards [5]. When harmonics in a system containing high negative components, particularly the 5th harmonic, induction motor may experience “torque fight”. This puts the motor at risk of burning up.

Triplen harmonics are all the odd harmonic components that are multiples of the third (i.e. 3rd, 9th, 15th, 21st etc). Triplens become an important issue for grounded-wye systems with current flowing in the neutral. Two typical problems are overloading the neutral and telephone interference. When the three-phase currents are balanced, triplen harmonic currents behave exactly as zero sequence currents. In three-phase 4 wire supply system, these harmonics are in phase with each other and add numerically in the neutral conductor. Thus a larger size neutral conductor is used.

Table 2.1: Classification of harmonics

Harmonic	F	2nd	3rd	4th	5th	6th	7th	8th	9th	10th
Frequency	50	100	150	200	250	300	350	400	450	500
Sequence	+	-	0	+	-	0	+	-	0	+

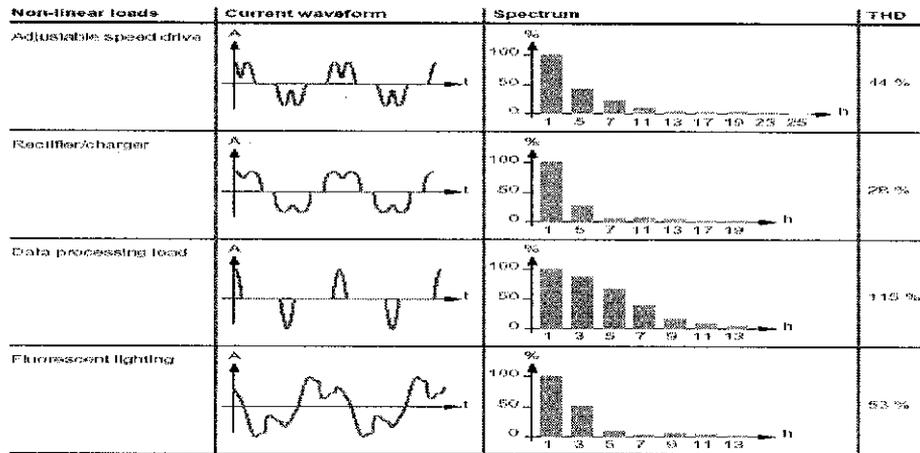


Figure 2.2: Characteristics of certain harmonics generators
 (Courtesy of Philippe Ferracci, Power Quality Notes: no. 199,
 ECT 199(e) October 2001)

Interharmonics are sinusoid components with frequencies which are not integer multiples of the fundamental component (they are located between harmonics). They are due to periodic or random variations in the power drawn by various devices such as arc furnaces, welding machines and frequency inverters (drives, cyclo-converters). The remote control frequencies used by the power distributor are also inter-harmonics. The spectrum may be continuous and vary randomly or intermittently. The magnitude of harmonic distortion can be reduced and suppressed by installing a suitably designed harmonic filter at the appropriate location in the installation. Other methods include the installation of line blocking inductors and selecting appropriate capacitor KVAR bank for power factor

improvements. The impact of harmonic: misoperation of sensitive equipment, capacitor failures in capacitor banks or fuses blowing due to transient current.

2.1.4 Voltage flicker

Voltage flicker can be due to rapid changes in rms voltage. Voltage flickers are caused by loads which are pulsating in nature, for example, arc furnaces and welding set. Fluctuations in the system voltage can cause low frequency light flicker depending on the magnitude and frequency of the variations. The impact of the flicker is annoyance to human observers. Fluorescent lamps are less sensitive to voltage flicker because of the effect of the phosphor coating and their operation with the ballast circuits. Compact fluorescent lamps (CFLs) operate at high frequencies using solid state ballast. High frequency light flicker from fluorescent lamps have been associated with headaches and eyestrain. Other impacts are: reduce life of electronic, reduce life of incandescent and fluorescent lamps, malfunctioning of phase-locked loops (PLL), maloperation of electronic controllers.

2.1.5 Transients

Transient (voltage or current) disturbance is due to change in the steady-state condition of voltage or current, or both with duration of less than a few cycles [IEEE. Std. 1250]. Power system switching operations such as switching on capacitor banks as shown in Figure 2.3, or switching unloaded transformer, switching during isolation or fault condition and lightning discharge can give transients as shown in Figure 2.4. Capacitor switching can cause resonant oscillations leading to an overvoltage some three to four times the normal rating, cause tripping or even damaging protective devices and equipment. Electronically based controls for industrial motors are particularly susceptible to these transients.

Surge arresters are installed to protect equipment from transient over-voltages by limiting the maximum voltage that can appear between two points in the circuit. Surge arresters should be installed as closely as possible to the equipment to be protected. The cable runs should be short and straight as possible to minimize surge impedance. The surge arresters must have good connection to earth.

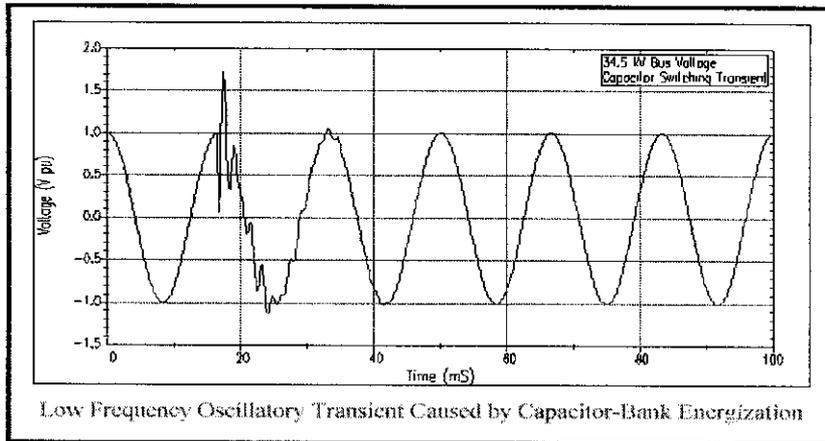


Figure 2.3: Low frequency transient caused by capacitor bank energization
(Courtesy of MS 1533: 2002, Malaysian Standard)

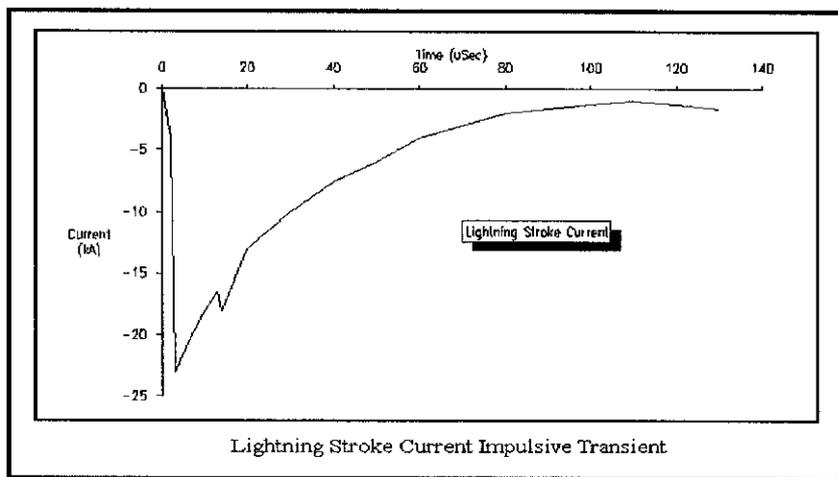


Figure 2.4: Lightning stroke current impulsive transient
(Courtesy of MS 1533: 2002, Malaysian Standard)

2.1.6 Voltage unbalance

The voltage unbalance occurs in a three-phase system in which the three voltage magnitudes are not equal or the phase-angle differences between them are not equal. The voltage unbalance is quantified as the ratio of the negative and positive-sequence voltage.

The maximum permissible value of negative phase-sequence voltage is 2% for one minute. Figure 2.1(c) is a voltage unbalance waveform.

2.1.7 Voltage magnitude variations

The steady-state voltage level fluctuation limits under normal conditions are: The percentage variations for 415V and 240V at +5% and -10%, up to 33KV at $\pm 6\%$, for 132KV and 275KV at +5% and -10%. [6]. The steady-state percentage variation limit under contingency condition is $\pm 10\%$ from voltage at 240V and up to 275KV.

Figure 2.1(d) is a voltage fluctuation waveform.

2.1.8 Notching

Notching is a periodic transient occurring within each cycle as a result of the phase-to-phase short circuits caused by the commutation process in AC to DC converters. Being periodic, this disturbance is characterized by the harmonic spectrum of the voltage waveform. The sharp edges created by the switching instants also contain high frequency oscillations that affect the insulation co-ordination of the plant and can give rise to radiated interference. This effect can be reduced by snubber circuits connected across the switching devices. The impact of notching: can upset electronic equipment and damage inductive components by their high level of voltage rise. However most high frequency content of notches beyond the control of utility is filtered by the power transformer at the service entrance.

2.2 Power Quality Indices

The commonly used power quality index is System Average RMS Variation Frequency Index (SARFI_X) [7, 8, and 9]. It provides a count rate of voltage sags, swells, and/or interruptions for a system. The size of the system is scalable: it can be defined as a single monitoring location, a single customer service, a feeder, a substation, a group of substations, or for the entire power delivery system.

$$SARFI_x = \frac{\sum N_i}{N_T}$$

where

x = threshold voltage (rms)

N_i = number of customers experiencing short-duration voltage deviations with magnitude above x % for $x > 100$ or below x % for $x < 100$ due to measurement event i .

N_T = number of customers served from the section of the system to be assessed.

$SARFI_x$ corresponds to a count or rate of voltage sags, swell and /or interruptions below a voltage threshold. For example, $SARFI_{90}$ considers voltage sags and interruptions that are below 0.90 per unit, or 90% of a system base voltage. $SARFI_{70}$ considers voltage sags and interruptions that are below 0.70 per unit or 70% of a system base voltage. $SARFI_{110}$ considers voltage swells that are above 1.1 per unit, or 110% of a system base voltage. The $SARFI_x$ indices are used to assess short-duration rms variation events only; with duration less than 60 seconds is included in its computation. Consider the following rms voltage variation event summary table, which was measured at a single site. The readings were recorded at Filrex Factory in Bercham, and are shown in Table 2.2.

The count of voltage sags and interruptions that would be included in the $SARFI_{90}$ is 4, as there were 4 voltage sags and interruptions measured at this location that had a minimum voltage below 0.9 per unit (90 percent) with a duration below 60 seconds. An example of determining $SARFI_x$ is shown in Table 2.3.

Table 2.2: Voltage event

Date / Time	Min. Voltage	Event duration
May – 15-2002 / 16:24:47	0%	17.94 sec
May – 15-2002 / 16:25:48	13%	60 ms
May – 20-2002 / 03:40:28	16%	100 ms
May – 29-2002 / 11:59:27	87%	1.3 sec
Till Jun-15-2002	None	None

Table 2.3: SARFI_x Rates Computed from Table 2.2

Index	Count	Rate per 30 Days
SARFI ₉₀	4	3.75
SARFI ₇₀	3	2.81
SARFI ₁₀	1	0.93

This is computed by dividing the 4 events by 32 days between the period 15 May 2002 and 15 Jun 2002 and then multiplying by 30 to normalize to events per 30 days. This is expressed as a rate of $4/32 \times 30 = 3.75$ events per 30 days.

2.3 International standards on Power Quality

IEEE STD 519-1992: Recommended practice and requirements for harmonic control in electric power system.

IEEE STD 1346-1998: Recommended practice for evaluating electric power system compatibility with electronics process equipment.

IEEE STD 1159-1995: Recommended practice for monitoring power quality.

IEEE STD 1250-1995: Guide on service for equipments sensitive to momentary voltage disturbances.

Malaysian Standard (MS) 1533-2002: Recommended practice in monitoring electric power quality.

Malaysian Standard (MS) IEC 61000-3-2: 2000: Electromagnetic Compatibility (EMC)

The standards regulate the requirements at the customer's point of connection to the electrical system.

SEMI F47: Voltage sag tolerance for semiconductor equipment

2.4 Conclusion

In this chapter various types of power quality disturbances have been discussed. Excessive harmonics in a network can cause overheating of neutral conductors, distribution transformers and malfunctioning of electronic equipment. Quality Indices are developed to reflect system service quality with respect to all rms voltage variations.

The active standard bodies in power quality are the Institute of Electrical and Electronic Engineers (IEEE), International Electro Technical Commission (IEC) and Malaysian Standard (MS).

CHAPTER 3
PSCAD/EMTDC AND PSS/ADEPT

CHAPTER 3

3.1 PSCAD

PSCAD is a simulator of electric circuits of low voltage power electronics systems, high voltage DC transmission (HVDC) and flexible AC transmission systems, as well as distribution systems and complex controllers. PSCAD can represent electric circuits in detail not available with conventional network simulation software. Transformer saturation can be represented accurately on PSCAD [10]. The following are some of studies that can be conducted with PSCAD:

- Insulation coordination of AC and DC equipment.
- Designing power electronic system and controls.
- Power quality analysis and improvements
- Variable speed drives, their design and control.
- Subsynchronous oscillations, their damping and resonance.
- Distribution system design with custom power controllers and distributed generation.

3.1.1 Modeling cable

Cables in electric power system are non-linear in nature due to frequency dependency in conductors (skin effect) and the ground or earth return path. The two methods for modeling cable lines for simulation in the time domain are:

1. Use of pi line sections. Pi line sections are most useful for very short line or cable where the propagation travel time is less than a time step.
2. Use of distributed lines. The distributed line models operate on the principle of traveling waves. A voltage disturbance will travel along a conductor at its propagation velocity (near the speed of light) until it is reflected at the end of the line. In a sense, a transmission line or cable is a delay function. Whatever is fed

into one end will appear at the other end after some delay. The calculation time step of the simulation should be less than the propagation time.

There are two pi line section components found in PSCAD. They are the Nominal Pi Section component and the Coupled Pi Section component. The Coupled Pi Section component is preferred over the Nominal Pi Section. The conductor voltages on the Coupled Pi Section component are always measured to true ground or earth. In transient studies with pi sections, it is important to consider whether a line should be represented by one or several sections. This dependent upon:

1. The calculation time step Δt .
2. The length of line.
3. The frequency of response required from the simulation model.

The time step marks the discrete intervals along the simulation time at which the simulator computes the voltage and current values. Greater accuracy of simulation can be achieved by having small a time step as possible. However, this increases the amount of computation, resulting in longer simulation time and greater amount of data. If frequency is being studied up to 2000Hz, then 50 μ sec calculation time step (Δt) is adequate.

If the length of the transmission or distribution line or cable is less than 15Km in length when $\Delta t = 50\mu$ sec, then one pi section is adequate to represent the line or cable. If the line is longer than 15Km, then two or more pi sections should be cascaded in series. The line is represented with positive sequence parameters in per unit (usually 100MVA base). The cable/line is represented by the parameters:

$$R + jX (B)$$

where:

R = series resistance (pu)

X = series reactance (pu)

B = shunt admittance (pu)

In this project, the COUPLED PI SECTION component has been used. The reason is the distribution cable length from the 132KV substation to the Ipoh hospital switching station is 10Km in length.

3.1.2 Transformer Model

The core of the transformer is prone to saturation leading to the phenomena of inrush current, remanence, and ferroresonance. The effect of winding capacitance are generally minimal and need not be modeled provide the frequencies of interest are less than about 2000Hz. Winding capacitance is important when fast front studies are to be performed and the magnetic effects can usually be neglected. The transformer model requires that there is leakage reactance, and so the concept of a fully ideal transformer without leakage reactance is not possible on PSCAD. The effect of winding resistance is negligible. For this project, the transformers at the source end are rated at 30MVA 132/11KV and at the load end are rated at 1.5MVA 11/0.415KV. The leakage reactance is 0.01pu (100MVA base). The star point of the 30MVA transformer is grounded at the primary whilst the 1.5MVA transformer is grounded at the secondary. This is done to give a balanced winding terminal voltage. The time to release flux clipping is also an important parameter to consider. When a case is starting up initially, then for calculation TIME less than the value entered here, the flux is inhibited or clipped and can't pass into saturation. This has the effect of centering the flux. This feature allows the network to initialize with the transformers being in saturation. For this project, the time to release flux clipping for both 30MVA and 1.5MVA transformer are 0.10sec and 0.15sec respectively.

3.2 PSS/ADEPT

PSS/ADEPT offers a full spectrum of design and analysis capabilities [11]. Using PSS/ADEPT, we can:

- Create and modify power network models graphically.
- Perform engineering analyses using multiple sources and unlimited nodes.
- Display the results of engineering analysis on the network diagram.

- Define and update single and multiple system component data via property sheets.

PSS/ADEPT was used in this project to study the load flow under balance and unbalance condition, the short circuit current and voltage magnitude at various nodes under fault condition. The PSS/ADEPT uses an iterative Y-Bus relaxation method to achieve solutions.

3.2.1 Transformer modeling

Two types of transformer models have been used in this project. The transformers are:

- Wye-delta (+30°)
- Delta-wye (+30°)

Figure 3.1 shows the PSS/ADEPT transformer types.

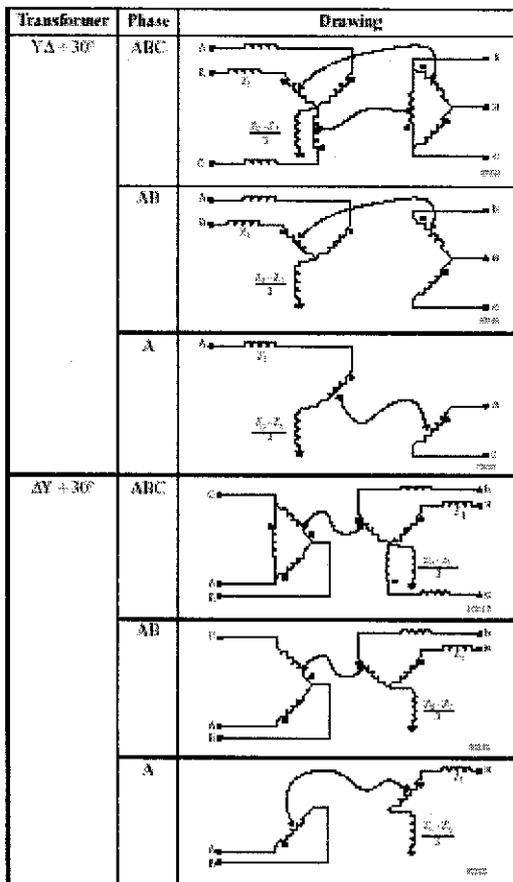


Figure 3.1: PSS/ADEPT transformer types

Each of these transformers have phasing ABC. Phasing is specified from the primary side of the transformer (e.g. for wye-delta transformer, the wye side is the primary). When specifying phasing, the designations A, B and C mean the first winding, second winding, third winding. Thus, for a wye-delta (+30⁰) transformer with A phasing is specified, the winding on the wye side of the transformer from phase A to ground exists and the winding on the delta side from C to A is installed. In PSS/ADEPT, the transformer taps are always on the TO side of the transformer, however we can always select the transformer type and FROM/TO nodes to get the connection desired. In PSS/ADEPT, the transformer size (in KVA) is specified on a single-phase basis. The single-phase basis is used because PSS/ADEPT allows modeling of single-phase branches. As an example, in the project, the three-phase substation transformer rating of 30 MVA 132/11KV, the rating per phase in PSS/ADEPT is 10,000KVA. This rating value with the winding voltage is used only to calculate the base impedance for the transformer. Each transformer has a positive and zero sequence impedance. The zero sequence impedance is used to represent grounding impedances in wye-connected windings. In this project, the transformers at the source end and at the receiving end are solidly grounded. The PSS/ADEPT will block the zero sequence current, shunting zero sequence current to ground.

3.2.2 Cable

The parameters required are: length in metres, construction type, positive-sequence resistance, positive-sequence reactance, zero-sequence resistance and zero-sequence reactance specified in ohm/unit length, positive-sequence charging admittance and zero-sequence charging admittance specified in $\mu\text{S}/\text{unit length}$, rating in ampere.

3.2.3 Source

A network to be solved in PSS/ADEPT must have at least one three-phase balanced source. The source will be represented by its terminal voltage, positive sequence and zero sequence impedance. When only the short circuit fault MVA of the source is known, it

must be converted to positive and zero sequence impedances. In this project, the source properties for the 132KV at Base 100MVA are calculated as follows:

$$\text{Positive-sequence impedance } (Z_{+ve}) = 2.4515 + j14.789 \Omega$$

$$\text{Zero-sequence impedance } (Z_0) = 1.7995 + j10.262 \Omega$$

$$\text{Impedance } Z_{\text{base}} = \frac{132^2}{100} = 174.24$$

$$Z_{+ve} \text{ pu} = \frac{2.4515 + j14.789}{174.24} = 0.0141 + j0.0848$$

$$Z_0 \text{ pu} = \frac{1.7995 + j10.262}{174.24} = 0.1032 + j0.05889$$

3.2.4 Calculating short circuits

A short circuit calculation determines the effect of a fault on the network. In PSS/ADEPT, there are two types of short circuit calculations: Fault calculation and Fault All. In this project, the desired faults (e.g. phase-to-ground fault, line-to-line fault and double line-to-ground fault) is selected at JAWAT2 in the network. When PSS/ADEPT runs the fault simulation, all node voltages, branch currents and fault currents are calculated. In the Fault All (includes all nodes in the network) calculation, a series of faults is sequentially and individually applied. Only the current magnitude in each of the fault is returned. Short circuit calculations are done using the network state prior to the fault occurrence. With the faults removed, a load flow is done to let the transformer taps set and to get the prefault voltage at each node. Static loads are then converted to constant impedance, based on the power and voltage at the node where they are connected. The actual short circuit calculation is then done. No transformer tap switching is done during the actual short circuit simulation.

3.3 Conclusion

This chapter describes the PSS/ADEPT and PSCAD/EMTDC software that was used in the simulation study. The PSS/ADEPT was used to study the load flow in the network prior to simulating a fault at the desired node. The magnitude of short circuit current and voltages at the various nodes were recorded. There is no provision to model and simulate a DVR in PSS/ADEPT. However, in PSCAD it was able to simulate a DVR circuit that was used to improve the voltage regulation during a fault in the selected network. In PSCAD the voltage magnitude with time duration for each phase can be represented graphically during a fault in the selected network.

CHAPTER 4
VOLTAGE SAGS – CASE STUDIES

CHAPTER 4

VOLTAGE SAGS - CASE STUDIES

4.1 Case studies

The following are the sample case studies which were conducted at Hitachi yoke plant, Filrex plant, Nihoncanpack and Ipoh hospital. The study involves data collection and practical measurements. Monitoring involves the capturing and processing of voltage and current signals of the power system. The purposes are: to monitor existing values of disturbances for checking against admissible limits, observing existing background levels and tracking the trends with time for any hourly, daily, patterns and verifying simulation studies.

4.1.1 Case study 1

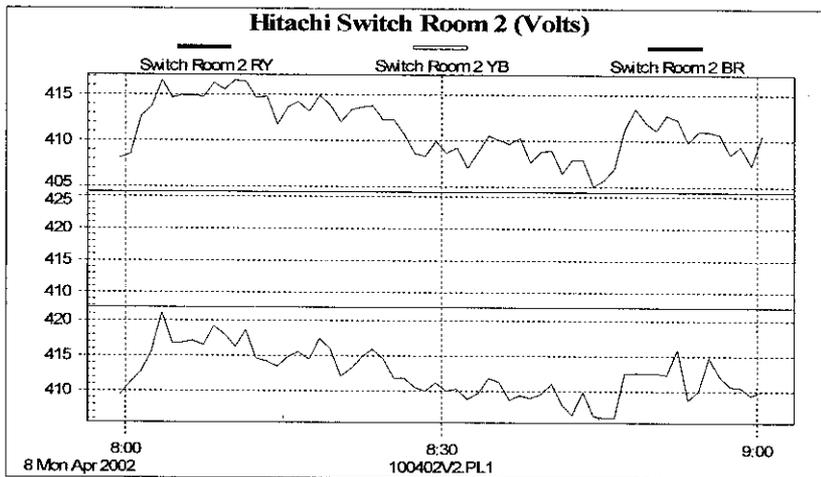
Hitachi yoke plant is situated at Bemban industrial estate, Batu Gajah. The factory is supplied by two parallel connected 2x1000KVA transformers rated at 22/.415KV each. Total demand of the factory is 1000KW.

a. Problems encountered

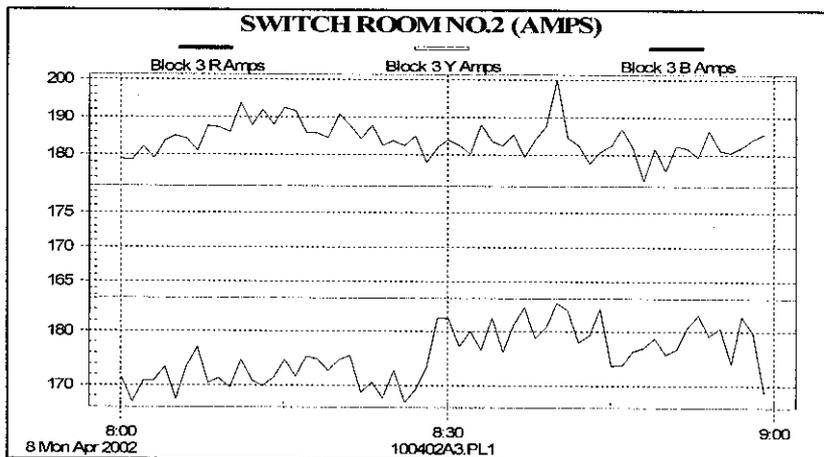
Major problem is voltage fluctuation causing sensitive machines like servomotors connected to production line frequently tripping. These servomotors are operated at 100 volt ac. A data logger was installed at the switch room on the low voltage side to monitor the voltage and current. From the monitored waveforms characteristics as shown in Figure 4.1, it is found that there are variations in the voltage and current measured at the consumer's main switch board N0.2. This occurs when there is a variation in the load at each shift interval.

b. Solution suggested

To minimize the problem, two prompt actions were carried out. Thermo vision checks to identify hotspots on the terminals and joints. To reduce the voltage variations, the customer was advised to install capacitor banks on the low voltage side to improve the power factor as well as to install on line Uninterrupted Power Supply (UPS) for each servomotors and the problem was contained.



(a) Voltage



(b) Current

Figure 4.1: Voltage and current variations
(Waveform measured on a Data Logger, courtesy of Hitachi plant Bemban)

4.1.2 Case study 2

Filrex (Rubberex) plant is located at Bercham industrial estate in Ipoh. This factory manufactures surgical and industrial rubber gloves. The factory receives electrical supply from an overhead line TRX1L 22KV connected via a 132/22KV substation. The 22KV supply is step-down through two (2x1.5MVA) transformer rated at 22 / .415KV, and the maximum demand is 2.0MW.

a. Problems encountered

The major complain from the consumer was frequent interruption. The most severe problem is the two out of the four ac servomotors connected on the Carrousel arm trip alternatively during voltage disturbance.

b. Solution suggested

A RPM Power recorder was installed at the 22KV main switchboard. The power tolerance curve obtained is as shown in Figure 4.2, where each dot represents an event that might disrupt equipment operations. An event is the change in the monitored voltage. The frequent 'power trips' were caused by system faults on the 22KV resulted in momentary interruption one after another because of autoreclosing operations.

The action plan under taken by the utility to reduce system faults include, thermo vision check on the lines and joints, rentice clearing, improve footing resistance, line patrolling, schedule and preventive maintenance, recalibration of the line protective scheme and installation of lightning arresters on the three phases at each pole support. This improved the performance of the line. At the consumer end, minor voltage adjustment was done. Firstly, the transformer voltage tap was adjusted from tap lower tap to upper tap, to give a ten volts boost on the low voltage output.

Secondly, for the position-control servomechanism of the servomotor, the input dc voltage to the amplifier that provides the source of control potential applied to the second stator winding of the servomotor was raised from lower level to next higher level.

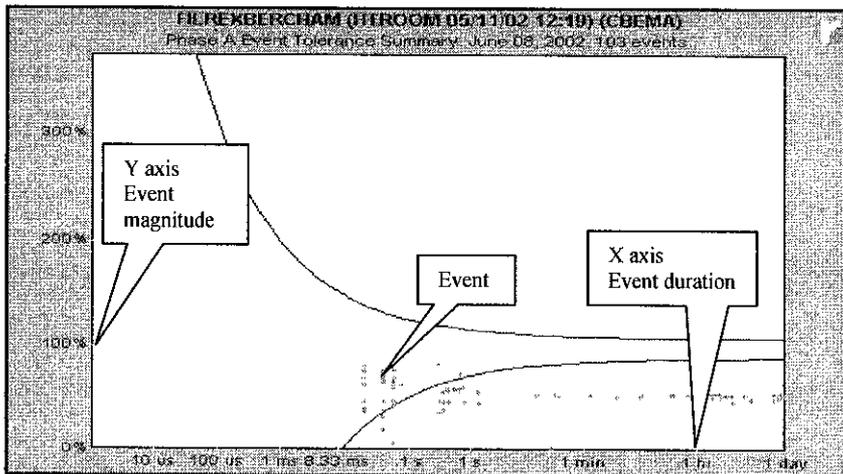


Figure 4.2: Power tolerance envelope of phase A
(Courtesy of Tenaga Nasional Berhad)

4.1.3 Case study 3

Nihoncanpack factory is located at the Bemban industrial estate in Batu Gajah. This factory manufactures cans for nestle products. The factory is supplied by a single 1000KVA 22/.415KV transformer.

a. Problems encountered

Process equipment fails due to voltage disturbances and harmonics. Power recorder was installed on the low voltage side to monitor voltage disturbances.

b. Solution suggested

From the monitored waveforms, 90 voltage sags and 25 wave shape faults were present. Efforts were under taken by the utility to reduce system faults include thermo vision check to identify hotspots and preventive maintenance.

4.1.4 Case study 4: Main target of the study

The Ipoh hospital is a 1000 bedded Government hospital situated in the centre of Ipoh city. The hospital has its own 11KV switching station feeding four indoor substations and two

500KW 415volts standby gen-set. Each substation has its own step-down transformer rating 11/415KV. The incoming source is from the main intake substation Kg. Jawa 132/11KV via 11KV underground cable rated at 185mm².

a. Problems encountered

The problem is voltage disturbances. The magnetic resonance imaging set (MRI), CT Scan and Magnetic Scanner trips frequently. These instruments receive electrical supply from substation N0.1 via 2x750KVA 11/415KV transformer. The monitoring equipment was connected at substation N0.1 low voltage outgoing side.

b. Solution suggested

From the monitored waveform, there were no transient, however there were 47 wave shape faults and 61 voltage sags occurred during the monitored period. Figure 4.3 shows the power tolerance envelope of phase C. Figure 4.4 is voltage sag on phase C with sag of 52.1%. Figure 4.5 is voltage sag on phase B with sag of 77.7%. To minimize system faults, on power cables, condition monitoring through use of very low frequency (VLF) Scanning Technique was done. Data related to Ipoh hospital is shown in Appendix H.

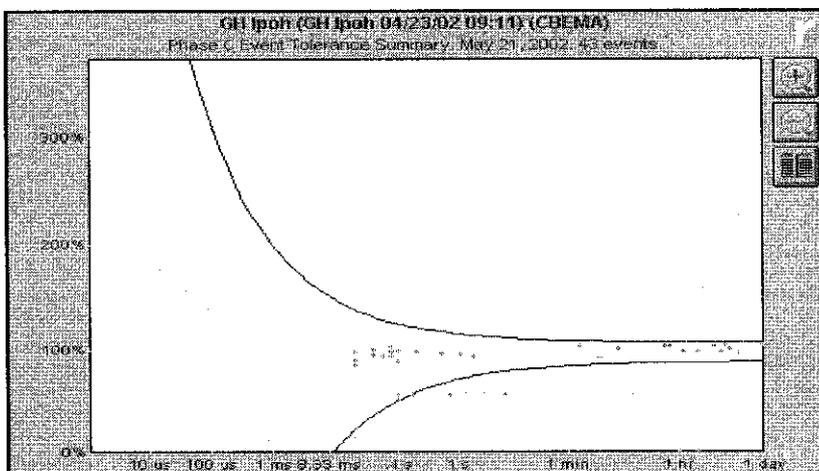


Figure 4.3: Power tolerance envelope of phase C (Voltage events) below magnitude 100% (Courtesy by Tenaga Nasional Berhad)

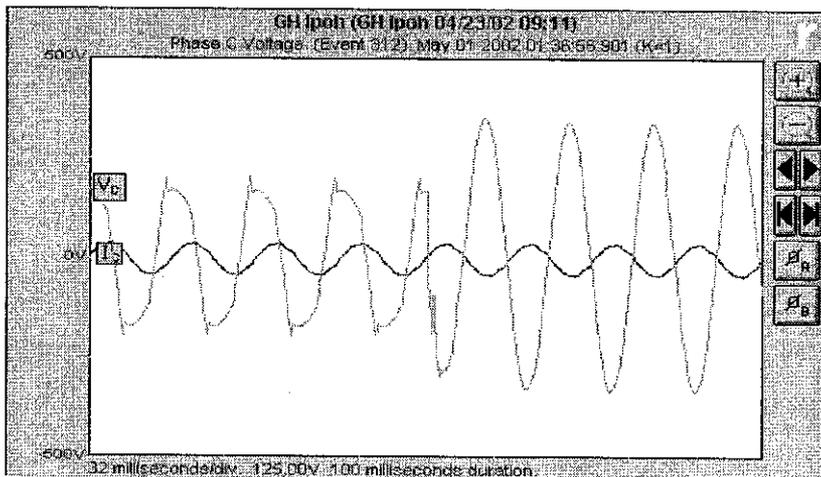


Figure 4.4: Voltage sag on phase C with notches
(Courtesy by Tenaga Nasional Berhad)

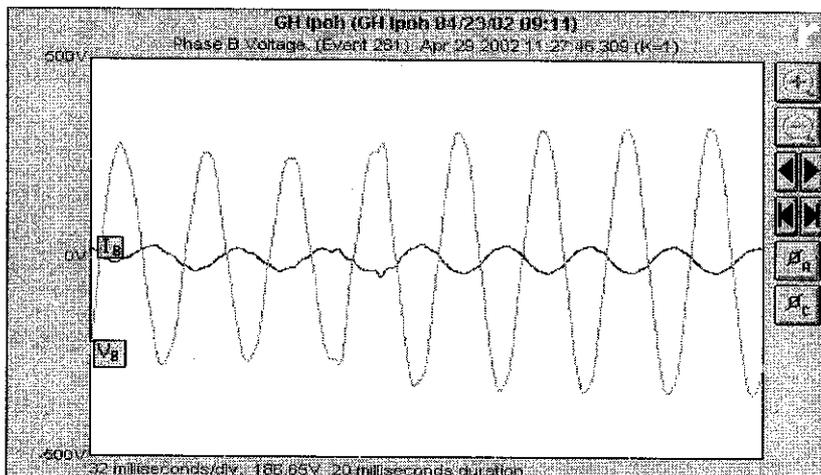


Figure 4.5: Voltage sag on phase B
(Courtesy by Tenaga Nasional Berhad)

4.2 Conclusion

We describe the case studies done at Hitachi, Nihoncanpack, Filrex and Ipoh Hospital. Data was collected and practical measurements carried by installing Reliable Power Meter (RPM) recorder. The importance of this recording is to identify the type, frequency, magnitude and duration of voltage events occurrence at the plant.

CHAPTER 5
POWER
MITIGATION DEVICE

CHAPTER 5

POWER MITIGATION DEVICE

5.1 Dynamic Voltage Restorer (DVR)

The Dynamic Voltage Restorer (DVR) is a device added in series between the power source (upstream side) and the load (downstream side). It functions to inject a voltage of arbitrary amplitude, phase and harmonic content into the distribution line so that the upstream disturbances will be compensated without affecting the load voltage. The performance of the DVR is affected by issues such as the pulse-width-modulation (PWM) method chosen, the overall control scheme and the filter.

5.1.1 Connection arrangement

The major parts of a DVR system are shown in Figure 5.1. In Figure 5.1, a key element is the voltage source inverter [2, 12].

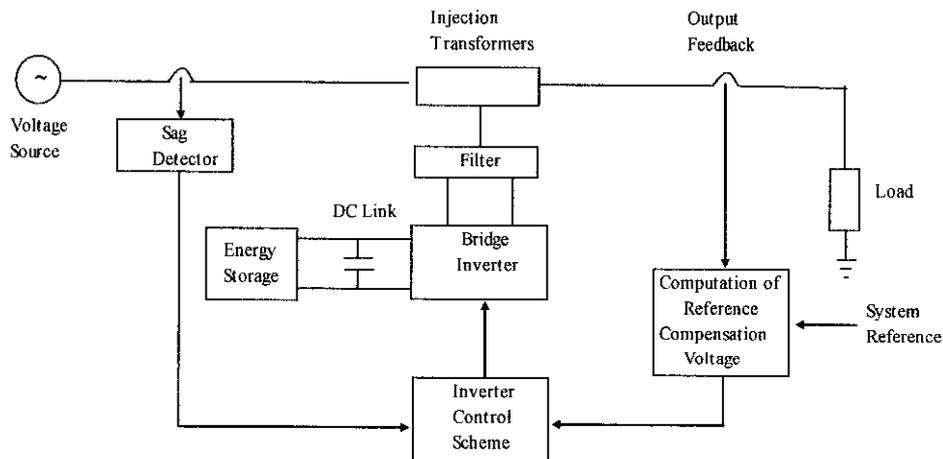


Figure 5.1: Block diagram of the DVR system

The voltage source inverter is responsible for producing the ac compensation voltage that is injected in series into the distribution line via the injection transformers. The dc power that feeds the inverter is obtained from the storage module. The inverter control scheme

implements the PWM scheme and generates the gate pulses for the inverter switches. The sag detector module detects the occurrence of a voltage sag and enables the inverter control scheme for generating the compensation voltage. The operation of the DVR can be summarized in the following steps:

1. Voltage sag detection: sagging detected, a signal is sent to the inverter control block to activate the control operation.
2. Reference Compensation Computation: reference compensation signal is computed by comparing the downstream load voltage, and the reference system voltage based on the feedback control scheme implemented. The reference signal thus computed is also sent to the inverter control block.
3. Inverter Switch Control: depending on the PWM control scheme used, the inverter control block sends switching pulses to the inverter switches to generate the required ac compensation voltage.
4. Filtering: inverter output passes through an LC low-pass filter to reduce the unwanted switching frequency components in the output voltage.
5. Injection into the line: the compensation voltage, having been filtered, is injected into the system via the injection transformers. The voltage thus injected adds on to the upstream voltage to produce the resultant compensated output voltage at the downstream of the line.
6. End of sag detection: once the sag is cleared, the sag detector sends a signal to the control block to stop the DVR from further compensating the system.

The control system of a DVR plays a very important role in the overall performance of the DVR, as the dynamic response and accuracy of compensation are very much dependent on the control strategy used.

5.2 Inverter Control Scheme of DVR

The performance of the DVR is dependent upon the type of PWM scheme used to switch on and off the power switches several times. The PWM operation of the inverter produces an output voltage consisting of a series of pulses whose width vary continuously. This pulsed voltage is then filtered to result in a sinusoidal output voltage. The PWM inverters offer important advantages to the control operation of the DVR. One advantage is that the PWM inverter is capable of having both frequency and magnitude control. The DVR is required to handle voltage sag conditions with system voltages that may vary dynamically both in magnitude and phase. As such, flexibility of control is very important to meet the dynamically changing conditions in terms of speed and accuracy. This is achieved through the use of fast response PWM scheme. It is essential that not too much unwanted harmonic is injected by the DVR itself into the distribution line as it compensates for the sag.

The PWM inverters can be subdivided into two categories, the voltage-mode and the current-mode control schemes, depending on the type of output signal feedback and the error signal control [2].

5.2.1 Voltage-mode control PWM inverter

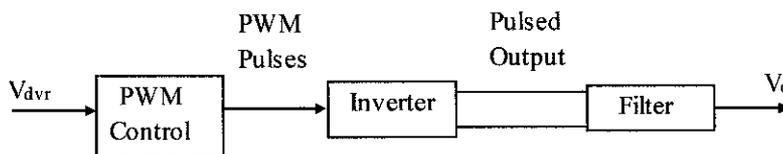


Figure 5.2: Voltage-mode control

Figure 5.2 shows the block diagram for the voltage-mode control of an inverter for the voltage-mode PWM control. The inverter used is a single-phase bridge inverter of the type shown in Appendix B. In general, in voltage-mode control, the inverter output voltage (V_o in Figure 5.2) is controlled based on a voltage reference signal (V_{dvr} in Figure 5.2). The

PWM control generates the PWM pulses based on this reference signal, and the pulses are used to control the switches of the inverter. Sine Pulse-Width-Modulation (SPWM) and selective harmonic elimination are examples of voltage-mode control schemes.

Selective harmonic elimination control scheme is based on confining unwanted harmonics to known frequency bands where they can be filtered out. In this thesis the SPWM control scheme is applied in the DVR application. The SPWM control has a modulating signal that is sinusoidal. This signal is compared with a triangular waveform generated by a generator to produce the PWM switching pulses. This pulsed output is made up of the fundamental component of frequency f , which is equal to the modulating frequency and other components at harmonic frequencies of f_1 . This pulsed output will be filtered through a low pass filter and the unwanted harmonic components of frequencies above f_1 will be filtered. The filtered output will be a smooth sinusoidal output waveform of the desired frequency f . Since a modulating signal derived from voltage error is used to control the output voltage of the inverter, the SPWM method is a voltage-mode control method.

5.2.2 Current-mode control PWM Inverter

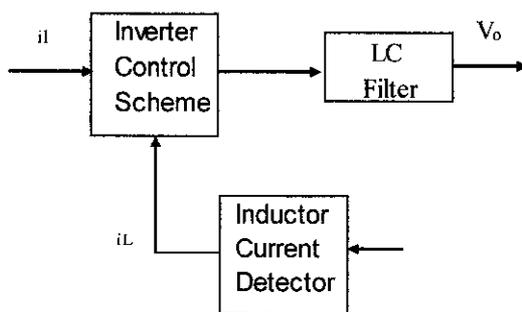


Figure 5.3: Current-mode control

Figure 5.3 shows the block diagram for the current-mode control of an inverter for the current-mode PWM control. In the current-mode control the inverter output current is being controlled based on the error between the actual output current and a reference

current signal. The inverter output current, in this case the filter inductor current i_L , is detected and compared with the reference signal i_i to generate the PWM switching pulses.

By directly controlling the inductor current, the effect of the inverter LC filter on the DVR transient performance can be minimized and the inverter's ability to closely track the reference control voltage can be improved. Hysteresis Current Control (HCC) and Constant Switching Frequency Predictive Control are examples of current-mode control schemes. To implement HCC an upper and a lower band limit are added to the reference signal i_i . The filter inductor current i_L at the output of the inverter is used to compare with this reference band. Whenever i_i hits any of the limits switching in the inverter occurs to make it stay within the band. With its faster dynamic response and insensitivity to load parameter variations, HCC offers improved DVR transient performance. The method is basically about forcing current to follow a reference signal.

5.2.3 Switching Frequency

In this work the selection of power electronic switches for the DVR inverter, the Gate Turn-off (GTO) Thyristor with free wheeling diode has been chosen as it allows fast response of the voltage source inverter and for high power operation. The GTO allows high switching frequencies of up to 25KHz and power range up to 5.0MW. The higher frequency inverter switching operation offers advantageous such as elimination of fast transients and high order harmonics. For a DVR of power rating ($< 1.0\text{MVA}$), a switching frequency of less than 2KHz can be used. However, the important criteria will be the order of harmonic to be filtered.

5.3 Storage Capacitor

If a small fault occurs on the protected system, then the DVR can correct it using only real power generated internally. For larger faults, the DVR is required to develop real power. To enable the development of real power an energy storage device must be used, normally the DVR design uses a battery bank or a capacitor bank. The rating of the capacitor bank or

battery bank is dependent upon system factors such as the rating of the load that protects and duration and depth of anticipated sags. When correcting large sag (using real power) the power electronics are fed from capacitor bank via a DC-DC voltage conversion circuit. The primary side of the DVR must be sized to carry the full line current. The DVR rating (per phase) is the maximum injection voltage times the primary current. A typical design value is 50%, 1 second; i.e., the controller is able to deliver 50% of nominal voltage for 1 second. In terms of energy-storage requirements this corresponds to full load for 500ms [2].

5.4 Injection Transformer

The injection transformer is a two winding transformer [2,12]. The primary is connected to the inverter and the secondary is series connected to the high voltage source. The criterion of selecting the injection transformer depends on the transformation ratio. Turns ratio greater than 1, the transformer operates in step-up mode, thus minimizing the energy storage from the capacitor. Another factor is the saturation level. The transformer should be operated below the saturation level to avoid output voltage distortion.

The leakage resistance and reactance should be small to reduce losses. Since the transformer is series connected at the load side, it is susceptible to large fault currents flowing through the winding during faults that develop at the load end. Bypass solid-state switches can be connected across each primary winding and can automatically close whenever an overcurrent is sensed in the distribution feeder serving the load.

5.5 Filter Design

The purpose of filter is to filter out the harmonic, thus ensuring the output voltage is sinusoidal. Two important factors are; corner frequency and the characteristic impedance of the LC filter. Under SPWM control the bridge inverter will generate a series of PWM square pulses. The pulsed inverter output then goes through the LC filter before being injected into the system. At the LC filter output is a switch controlled by the 'act signal' of

the sag detector. It is closed when no sag is detected to short-circuit the primary side of the injection transformer so as to inject zero compensation voltage into the system. This can be done by connection of back-to-back thyristors across the injection transformer.

5.6 Design Goals

The design goal is, duration for which voltage sags need to be corrected is between 20ms to 0.03ms. The required voltage compensation for sags varies between 10% and 50% of nominal voltage. During voltage sags, the load voltage must be maintained within the “Normal Operating Voltage” as defined by IEEE Std. 1159. A continuous monitoring of the load line voltage is incorporated to facilitate rapid detection of voltage abnormalities and remedial action.

5.7 Conclusion

The structure of the DVR system can be considered in terms of different modular parts. Of interest in this project will be the parts making up the DVR control system, namely the sag detection, inverter control block and the computation of reference compensation voltage. The tracking model, in which the reference output voltage is sinusoidal can be applied. For the inverter control schemes the voltage-mode and the current-mode control PWM schemes have been discussed.

CHAPTER 6
MITIGATION OF DISTURBANCES

CHAPTER 6

MITIGATION OF DISTURBANCES

6.1 Minimizing faults

Limiting the number of faults is an effective way to reduce both the number of voltage sags and the frequency of interruptions. Faults on overhead lines are mainly caused by trees, animals, lightning, wind and insulation failure [2, 13]. Faults due to lightning can be reduced by lowering the ground resistance at the foot of the tower or poles. The stroke is then conducted to earth by the towers. Reduction in the number of faults can be achieved by replacing overhead lines by underground cables, which are less affected by adverse weather. The fault rate of an overhead line is much higher than that of an underground cable; however the repair time of cable is longer.

6.2 Modifying fault-clearing practices

Reduction of fault-clearing time affects not the number of events, but only the duration of voltage sags. Therefore, it leads to less severe voltage sags. The automatic reclosure and sectionaliser can be installed for overhead line protection to avoid long interruptions on non-permanent faults such as transient, thus improving reliability and quality of the supply.

Figure 6.1 shows a circuit breaker is used for protection of the whole feeder, while each lateral is protected by a slow expulsion fuse. The circuit breaker opens for any fault in the feeder, thus interrupting all the loads. A recloser is used in order to limit the consequent long interruption for the customers, thus turning it into a series of short interruptions (for all the loads on the faulted feeders) and voltage sags (for loads on adjacent feeders), until the fuse on the faulted lateral blows. This practice may lead to large number of short interruptions which may turn into a large number of production stops for sensitive industrial and commercial customers.

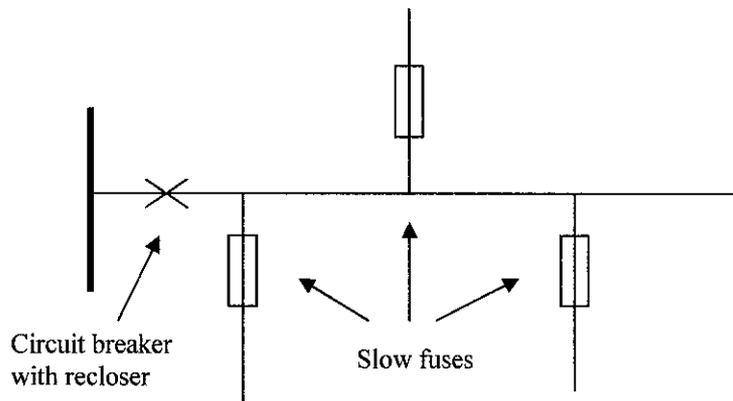


Figure 6.1: Radial system with one breaker for the whole feeder

If the fault-clearing time of the circuit breaker is unsatisfactory, current-limiting fuses or static circuit breakers of fast operation can be installed [13]. Figure 6.2 with multiple substations in cascade, time-grading of the over current relays are normally used in order to achieve selectivity. Moving from the load to the source, the tripping delay increases with 0.4 sec, a standard time-grading used so that the breaker nearest to the fault will open.

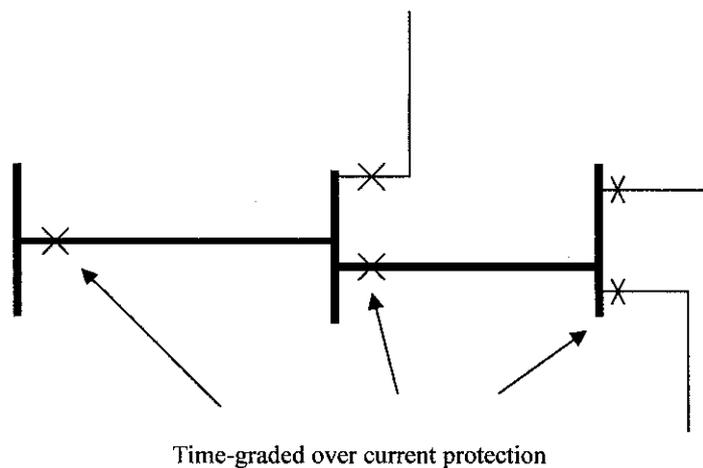


Figure 6.2: Radial distribution system with cascaded substations

6.3 System design

In the system of Figure 6.3 a number of feeders, protected by fuses, originate from the same distribution substation: a fault on a feeder will lead to fuse blowing, thus to an interruption for all the loads supplied by that feeder. No alternative path for supplying the loads is available, so repair or replacement of the faulted component is needed for restoration of the supply, thus leading to a long interruption.

The other loads connected to the same bus will experience voltage sag, whose magnitude is directly proportional to the impedance between the fault and the substation. The performance of radially-operated systems can be improved by reducing the number of feeders originating from the same bus, thus minimizing the number of faults leading to voltage sag for equipment fed from that bus. An alternative method is to supply the sensitive load through a dedicated feeder.

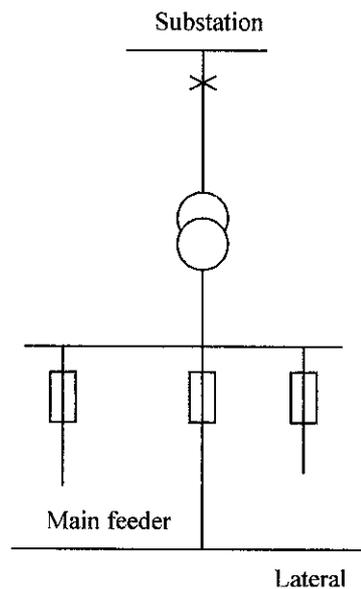


Figure 6.3: Radial distribution system

6.4 Network splitting

A system with high fault level Megavolt ampere (MVA) indicates the strength of an electrical network system. A high fault level implies low impedance between source and load and good system voltage profiles and low magnitudes of voltage sags when they occur [14]. It also has an influence on the operating time of protective devices under fault conditions. However high fault level requires switchgear with high rupturing capacities, which is expensive.

Connection of a local generator in the network system causes the fault level to rise above the existing switchgear rating. One method to reduce the faults in power system is by network splitting.

The network splitting scheme in Figure 6.4 uses the bus coupler between Bus1 and Bus2. By splitting the network the impedance between the 33KV and 11KV increases, reducing the fault current flowing from 33KV, for fault at F. However this scheme decreases the flexibility of the generator. When Bus2 needs maintenance, the generator (G) has to be disconnected from the network.

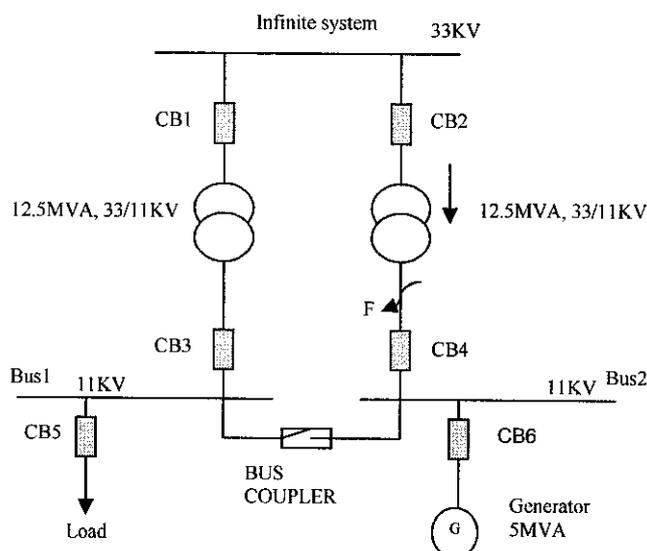


Figure 6.4: Network splitting

In Figure 6.5 circuit breaker CB7 is added but the flexibility and safety of the network as well as that of the generator (G) are improved. Under normal operation, the bus coupler is open separating the 11kv bus into two parts, Bus1 and Bus2. In general, voltage recovery is better when the network is split by a bus coupler.

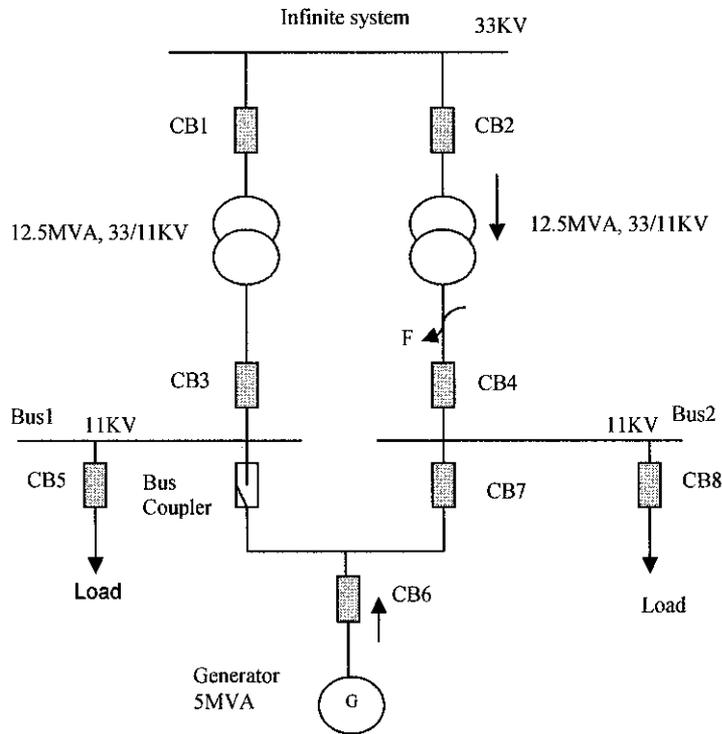


Figure 6.5: An alternative network splitting

6.5 Custom Power Devices

6.5.1 Uninterrupted Power Supply (UPS)

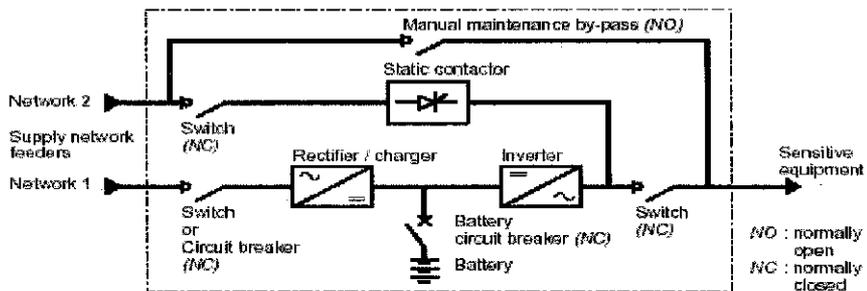


Figure 6.6: Schematic diagram of an on-line uninterruptible power supply (Courtesy of Philippe Ferracci, Power Quality Notes: no. 199, ECT 199(e) Oct 2001)

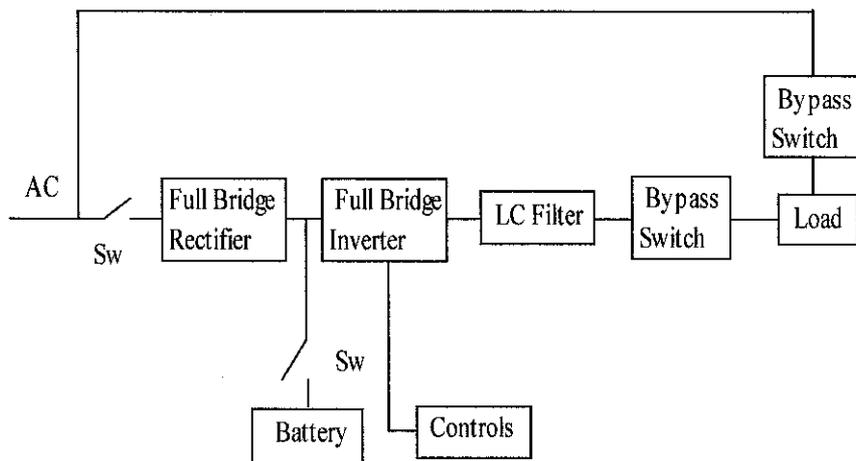


Figure 6.7: Block diagram for UPS

UPS (Uninterrupted Power Supply) as shown in Figure 6.6 is extremely popular for computers, personal computers, central servers, and process-control equipment. The block diagram for an UPS is shown in Figure 6.7. The model consists of a full bridge rectifier, battery, full bridge PWM inverter, LC filter, and two transfer switches and two bypass switches. The bypass switches are used for reverting to main ac line in the event of UPS failure or overloaded. The LC filter is for eliminating unwanted harmonic component.

The operation of the UPS can be divided into 2 modes such as normal operation mode and back-up operation mode.

Normal operation mode

A single-phase UPS is as shown in Figure 6.8. With reference to Figure 6.8, in the normal operating mode, both switch S1 and S2 are closed. The full bridge inverter receives energy from the main ac source through full bridge rectifier. The battery will be on float charge. The dc voltage during normal operation is slightly above the battery voltage so that the battery block remains in standby mode. The bypass switch BP1 is closed. The load is powered through the inverter which generates a sinusoidal voltage typically by using a

Pulse Width Modulation (PWM) switching pattern. If the inverter is overloaded, or if it fails, switch BP2 is turned on and BP1 is turned off.

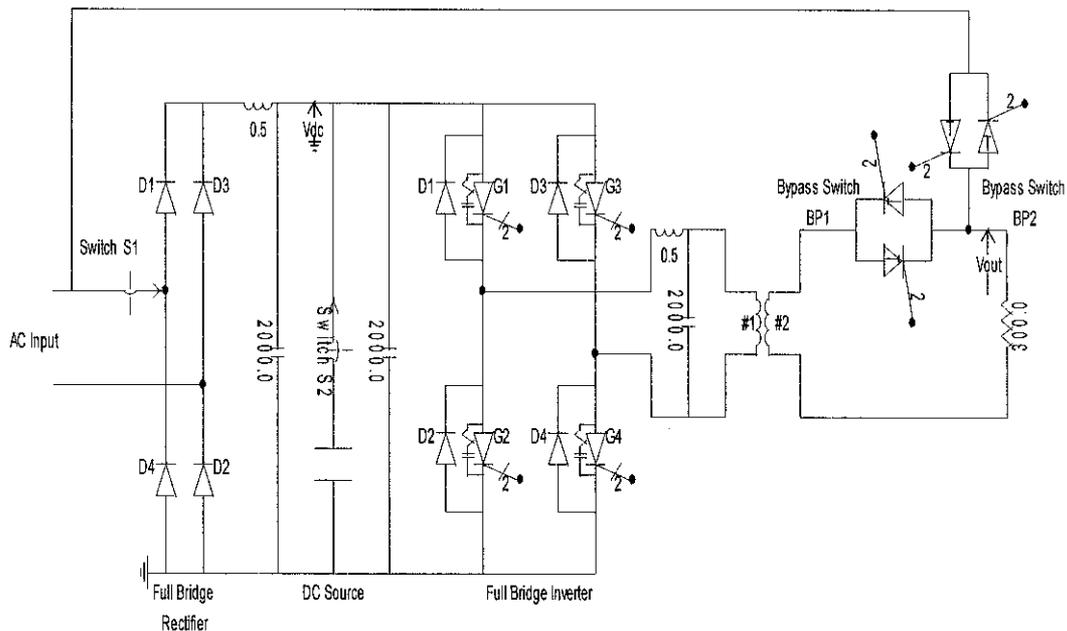


Figure 6.8: Single-phase model of UPS

Back-up power mode

During a voltage sag or interruption in the main ac source, static switch S1 is opened, shifting the input from the main ac source to the battery. Thus, the full bridge inverter receives energy directly from the battery. After the main ac source recovers, the static switch S1 will be closed again and the UPS will change its operating mode from back-up to normal operation mode. However, some UPS contain an additional AV regulator (AVR). The main function of the AVR is to regulate the voltage input and smooth out the electric circuit. For example, when there is sudden voltage spike or voltage sag, the AVR can detect this and suppress the voltage with a buck or boost action.

Bridge rectifier

With reference to Figure 6.9, during the positive half-cycle of the ac input voltage, diodes D1 and D2 conduct. During the negative cycle, diodes D3 and D4 conduct.

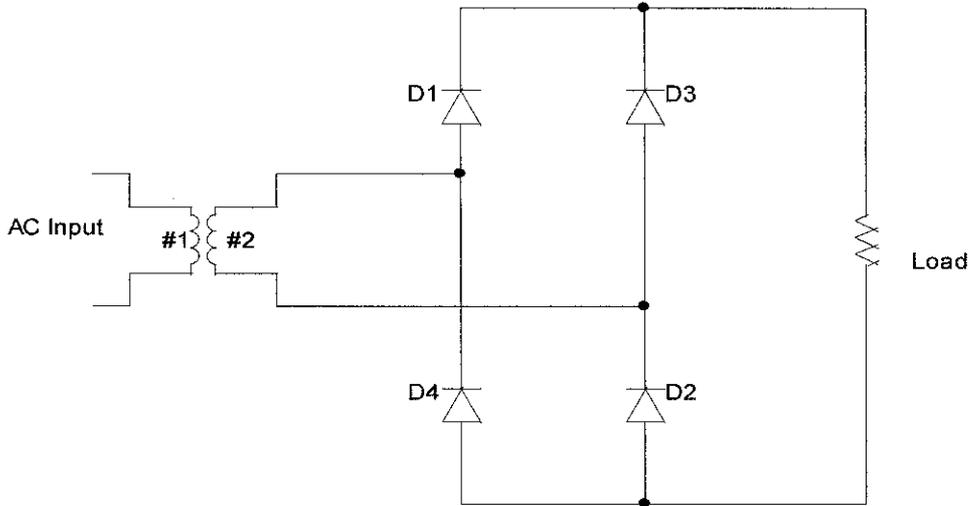


Figure 6.9: Single phase Full-wave bridge rectifier

The average output voltage is

$$V_{dc} = \frac{1}{\pi} \int_0^{\pi} V_m \sin \omega t \, dt = \frac{2V_m}{\pi} = 0.6366 V_m$$

The rms value of the output voltage is

$$V_{rms} = \left[\frac{1}{\pi} \int_0^{\pi} (V_m \sin \omega t)^2 \, dt \right]^{1/2} = \frac{V_m}{\sqrt{2}} = 0.707 V_m$$

Bridge inverter

Figure 6.10, the combination of a thyristor and a parallel-connected diode has the effect of a fully controlled bi-directional switch [15]. When Gate turn-off GTO (G1) and GTO (G4) is conducting and G3 and G2 is blocking, the load is connected to the positive supply terminal through G1 and vice versa. Thus each output terminal is effectively connected to

one side of the dc supply or the other, depending only upon the state of the thyristors. The GTO is commonly used in pulse-width modulated inverter drives operating at high switching frequency [16]. The output voltage of the inverter is required to be sinusoidal with controllable magnitude and frequency. Pulse Width Modulation (PWM) switching scheme is usually used. The sinusoidal reference control signal is compared with a triangular waveform generated by a generator to produce the PWM switching pulses as shown in Figure 6.11.

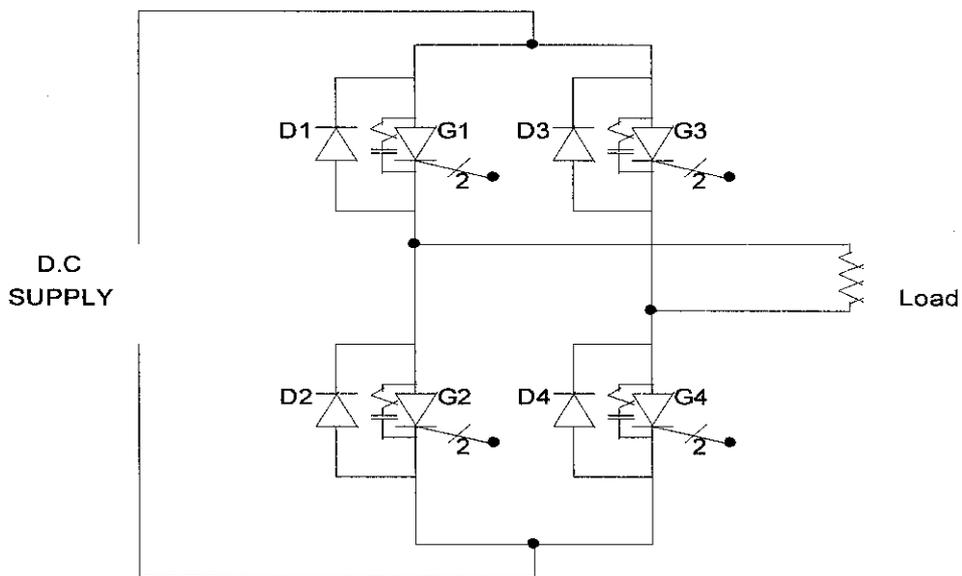


Figure 6.10: Bridge inverter with reactive feedback diodes

For a three-phase inverter, the line-to-line rms voltage is:

$$V_L = \left[\frac{2}{2\pi} \int_0^{2\pi/3} V_s^2 d(\omega t) \right]^{1/2} = \sqrt{\frac{2}{3}} V_s = 0.8165 V_s$$

The rms value of line-to-neutral voltage is:

$$V_P = \frac{V_L}{\sqrt{3}} = \frac{\sqrt{2} V_s}{3} = 0.4714 V_s$$

The triangular waveform will be at a high switching frequency more than the fundamental frequency of 50 Hz. Higher switching frequency will improve the efficiency of the inverter and reduce switching losses [17].

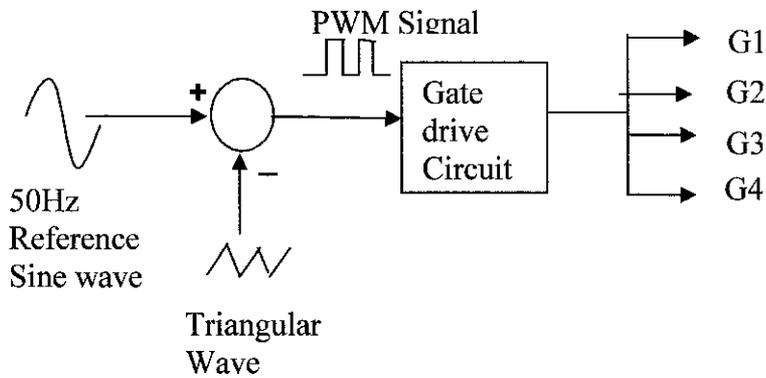


Figure 6.11: Inverter control block diagram

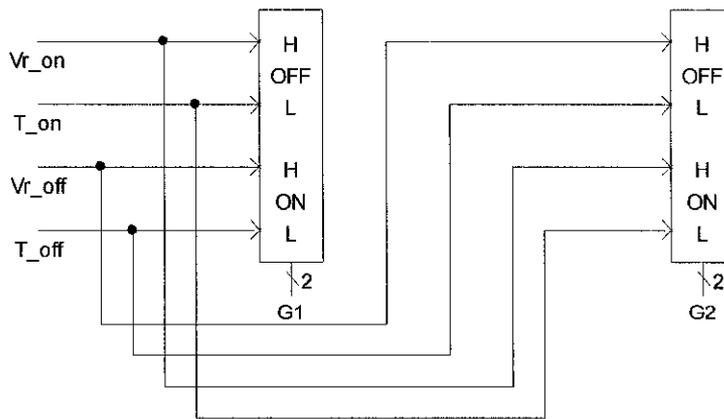


Figure 6.12: Gate drive circuit in PSCAD

The distortion factor and lower-order harmonics are reduced significantly. The signal is used to drive the inverter switches consisting of Gate Turn-off Thyristor. The pulse width

amplitude signal can be set between 0.0 and 1.0 with frequency of 50Hz. The gate drive circuit of a PSCAD component called an Interpolated Firing Pulses is used as shown in Figure 6.12. This component requires two sets of signals which are the reference signal (V_r on_ and V_r off) and triangular signal (T on and T off). One set of the signal is to turn on and the other is to turn off the GTO.

6.5.2 Solid-State Transfer Switch (SSTS)

The SSTS can be used very effectively to protect sensitive loads against voltage sag. The SSTS ensures continuous high-quality power supply to sensitive loads by transferring, within 4 ms at 50Hz, the load from a faulty bus to a healthy one. The basic configuration of this device consists of two solid-state switches of which, one is the main feeder and the other is the backup feeder. These switches have an arrangement of back-to-back connected thyristors, as shown in Figure 6.13.

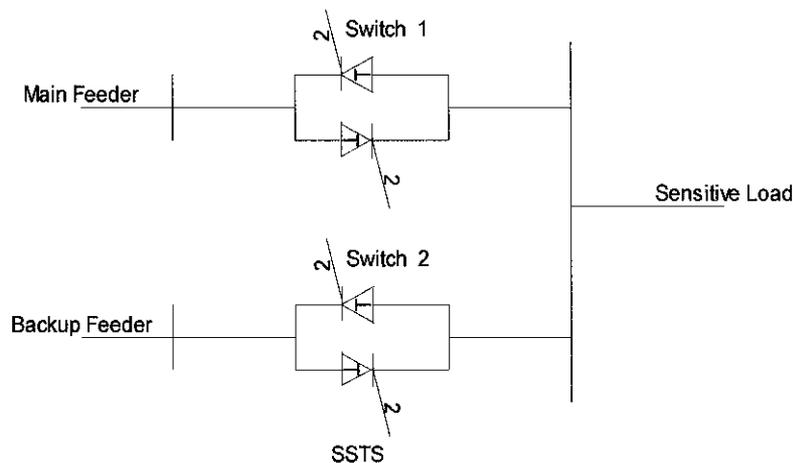


Figure 6.13: SSTS as a custom power device

Each time a fault is detected in the main feeder, the control system swaps the firing signals to the thyristors in both switches, i.e., Switch 1 in the main feeder is deactivated and Switch 2 in the backup feeder is activated. The control system measures the peak value of the voltage waveform at every half-cycle and checks whether or not it is within a

prespecified range. If it is outside limits, an abnormal condition is detected and the firing signals to the thyristors are changed to transfer the load to the healthy feeder.

6.5.3 Distribution Static Compensator (D-Stat Com)

The D-Stat COM consists of two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt with the ac system, and the control system [2]. A Stat Com does not contain any active power storage and thus only injects or draws reactive power. Limited voltage sag mitigation is possible with the injection of reactive power only [2], but active power is needed if both magnitude and phase angle of the pre-event voltage need to be kept constant. The shunt voltage controller is shown in Figure 6.14.

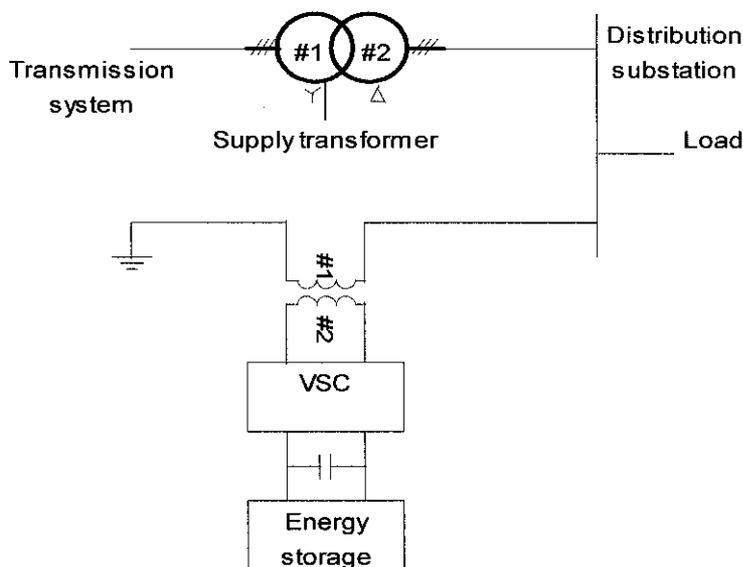


Figure 6.14: Shunt voltage controllers

The actual controller has the same configuration as the series controller (DVR). But instead of injecting the voltage difference between the load and the system, a current is injected which pushes up the voltage at the load terminals, in a similar way to the sag mitigation by a generator.

6.6 Conclusion

By taking proper measures in the design of the distribution system, improvements against voltage sags and short interruptions can be achieved. In this chapter, the impact of several possible actions has been discussed. Network splitting has high reliability, flexibility and is very effective for fault level reduction. Different types of custom power devices were discussed.

CHAPTER 7
MODELING, SIMULATION AND RESULTS

CHAPTER 7

MODELING, SIMULATIONS AND RESULTS

7.1 Software used

Two software packages were used for various stages of simulation, measurement and analysis of power quality disturbances in this project:

7.1.1 PSCAD/EMTDC- Version 4.0

Power System Computer Aided Design (PSCAD) is used in this project to simulate voltage sag waveforms [17]. Figure 7.1 shows the opening screen of PSCAD. PSCAD is a graphical user interface which substantially increases productivity in undertaking simulation of electromagnetic transients studies of electrical power systems. PSCAD/EMTDC is capable of simulating both electro-magnetic and electro-mechanical systems. EMTDC code is in FORTRAN. To perform the simulations, PSCAD represents and solves the differential equations of the entire power system in the time domain. The results are solved as instantaneous values in time and therefore the response of the power system can be duplicated at all frequencies, bounded only by the user-selected time step. This time stamp can be varied from nano-seconds up to many seconds. Simulation time-step of $50\mu\text{s}$ produces sufficiently accurate and stable results.

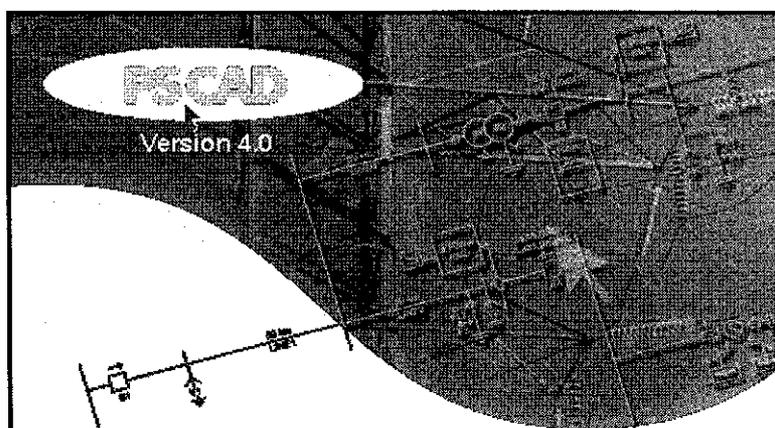


Figure 7.1: PSCAD opening screen

7.1.2 PSS/ADEPT

Power System Simulation/Advanced Distribution Engineering Productivity Tool (PSS/ADEPT) is used in this project to simulate voltage sag magnitude at various bus nodes and load flow study [11]. The PSS/ADEPT is an integrated interactive program for simulating, analyzing and optimizing performance of unbalanced distribution systems.

7.2 Modeling of the distribution system

Figure 7.2, Appendix A shows the single line diagram of the Ipoh hospital distribution system. The power distribution system of the Ipoh Hospital was selected for the study because important life saving sensitive equipments suffer mal-operation/interruption under various kinds of power disturbances. These equipments are connected at substation N0. 1.

7.2.1 Ipoh Hospital

The power distribution system consists of 11KV switching station feeding four 11KV substations. The N0.1 substation has 2 x 750KVA 11/0.415KV transformer, whilst the other three substations have 1 x 500KVA 11/0.415KV transformer each. The maximum demand of Ipoh Hospital is 1.22MW.

The 11KV switching station is connected to the supply utility main intake (Kg. Jawa) 132/11KV by a 11KV power cable paper insulated lead covered (PILC) size 185 mm² at approximately 10Km in length. The load pattern of the hospital distribution system mainly includes lighting and power, air-conditioner, computers, heaters and sensitive medical equipments. Some power quality related disturbances were reported in the hospital distribution system. The Magnetic Resonance Imaging (MRI), and CT Scan mal-operated and tripped occasionally. The abnormal tripping that leads to time consuming reset/restarting process for MRI and CT Scan, caused inconvenience to both the patient and the hospital authority. For site monitoring and recording of the disturbance, the Reliable Power Meter (RPM) recorder was installed at substation N0.1 11/0.415KV at the hospital distribution system.

7.2.2 Component Models

a. Source properties

The source of supply is from the 132KV Substation Kg.Jawa. Table 7.1, 7.2, and 7.3 shows the source properties, transformer and cable properties respectively.

Table 7.1: Source Properties

Positive sequence resistance (pu)	0.01410
Positive sequence reactance (pu)	0.08480
Zero sequence resistance (pu)	0.10320
Zero sequence reactance (pu)	0.05889

b. Transformer properties

Table 7.2: Transformer properties

Transformer Rating	Capacity (KVA)	Type	+ve seq. resistance (pu)	+ve seq. reactance (pu)	Zero seq. resistance (pu)	Zero seq. reactance (pu)
132/11 KV	30,000	Wye Delta +30 deg	0.0104	0.0994	3.0	0.0994
11/415 KV	750	Delta Wye +30 deg	0.0224	0.0469	0.1075	0.0469
11/415 KV	500	Delta Wye +30 deg	0.0246	0.0468	0.1482	0.0468
11/415 KV	1500	Delta Wye +30 deg	0.0224	0.0469	0.16085	0.0469

c. Underground power cable properties

Table 7.3: Underground cable properties

Rating (amps)	Size (mm ²) 11Kv	Type	+ve seq. resistance	+ve seq. reactance	Zero seq. resistance	Zero seq. reactance	+ve seq charging admittance
280	185 mm ²	PILC	0.195	0.0829	2.39	0.0406	218.04

7.3 Simulation results

7.3.1 PSS/ADEPT

The PSS/ADEPT software was used to model and simulate the load flow and sag magnitudes at various nodes under fault conditions. The results indicate the voltages at the respective buses as well as at the end-user equipments. Three types of faults were simulated namely: single line-to-ground fault (SLGF), double line-to-ground fault (DLGF) and line-to-line fault (LLF). The location for fault simulation is Bus JawaT2 as shown in Figure 7.2 in Appendix A. This node is at the source and frequently affected by faults. The results of simulation are shown in Tables 7.4 – 7.6 in Appendix C, power flow is in Appendix D, transformer status is in Appendix E and fault current is in Appendix F.

7.3.2 PSCAD

A Dynamic Voltage Restorer (DVR) used for voltage sag mitigation has been modeled using PSCAD/EMTDC and connected on the 11KV bus at JawaT2 of the Ipoh hospital distribution system because this node is affected by frequent faults. For this project simulations are run for three types of sag conditions, namely:

1. Single-phase fault
2. Double line-to-ground fault
3. Line-to-line fault

7.3.3 Ipoh Hospital Distribution Line Component Model

The Ipoh hospital distribution system in PSCAD is shown in Figure 7.3 in Appendix B, which includes the main power transformers rated at 30MVA 132/11KV 50Hz each and the distribution transformer rated at 1.5MVA connected at substation N0.1. Transformer parameters are shown in Table 7.7 – 7.8. Transformer T1 and T2 vector group is $Y_{Nd}11$ and tap is set at 10. Vector group of transformer at load end is Dy_n11 and tap is set at 3.

Table 7.7 : Parameters of 30MVA Transformers

Leakage reactance	0.05[pu]
Magnetizing current	0.40[%]
Air core reactance	0.20[pu]
Inrush decay time constant	0.15[sec]
Knee Voltage	1.25[pu]
Time to release flux clipping	0.10[sec]

Table 7.8 : Parameters of 1.5MVA Transformers

Leakage reactance	0.10[pu]
Magnetizing current	0.40[%]
Air core reactance	0.20[pu]
Inrush decay time constant	0.15[sec]
Knee Voltage	1.25[pu]
Time to release flux clipping	0.15[sec]

The source is at 132KV and base MVA is 100. The coupling circuit breaker is closed. The total length of underground cable from the source is 10Km rated at 11KV and is model using the Coupled Pi Section for simulation in the time domain. Pi line section is used because the cable length is 10Km and the propagation travel time is less than a time step. The injection transformers are connected to a 12-pulse Gate Turn-off (GTO) thyristors. The input to the three phase rectifier is via a step-down transformer. The input voltage is 2000V. The rectifier voltage output formula is:

$$\text{Rectifier output voltage, } V_{dc} = \frac{3 * \sqrt{3}}{\pi} V_m = \frac{3 * \sqrt{3}}{3.142} * \sqrt{2} * 2000 = 4677V$$

$$\text{Ripple} = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{1.6554V_m}{1.6542V_m}\right)^2 - 1} = \sqrt{1.0007^2 - 1} = 0.0374 = 3.74\%$$

The value of commutating reactance is calculated as follows:

$$V_x = 6fL_c I_{dc} \text{ where } L_c = L_1 = L_2 = L_3, V_x \text{ is voltage drop and } f \text{ is frequency.}$$

If the voltage drop is 1%, and the resistance is 50 ohms, then inductance L_c is:

$$L_c = \frac{46.77 * 50}{300 * 4677} = 0.002H$$

7.3.4 Storage Capacitor

When designing the DVR, we have to take into account the storage energy needed for compensation. The key factors are the amount of sag intended to compensate and the duration of the sag to compensate. The energy needed from storage capacitors will be:

$$\text{Energy needed, } E = \frac{1}{2} CV^2 \text{ J.}$$

The voltage decreases when the energy is extracted from the capacitor. The storage capacitor is charged by a variable dc voltage. Capacitors cannot be used to supply electric power to a constant-voltage dc bus, hence a (dc/dc) converter is needed between dc bus and the capacitor. The storage capacitor value is calculated as follows:

Energy needed, $E = \frac{1}{2} CV^2 = 1000 \times 0.5 \times 500 \times 10^{-3} = 250J$. The storage capacitor allowable voltage level drop is 0.8 nominal value. This value is chosen to be close to the maximum desired inverter output (0.8165). We wish to compensate 50% of voltage sag which is 2.34KVrms (out of 4.681KVrms nominal value). We can calculate the capacitor size need: $\frac{1}{2} CV^2 = \frac{1}{2} \times C \times (4.681^2 - 0.8^2 \times 4.681^2) = 0.5C \times 8KV = 250J$. Hence C is 63380 μ F. Thus the amount of energy in one capacitor is energy:

$E = \frac{1}{2} \times 63380\mu F \times 4.681^2 = 690kJ$. At 50% sag for 500ms, 75% of energy can be extracted from the capacitor i.e $0.75 \times 690kJ = 520kJ$. Hence power supplied to load for 500ms is 520kJ / 500ms equals 1041KW.

7.3.5 The Low-Pass LC Filter

The switching frequency is set at 1650Hz. This is to filter out the 33th order harmonic on harmonic content and also to comply to IEC standard 1000-3-2 and EN 61000-3. With f_s around 1650Hz, the inverter output will contain the fundamental component at the system

frequency of $f_{\text{sys}} = 50\text{Hz}$ and harmonics at multiples of around 1650Hz. To filter out the high frequency harmonic signals due to switching and to allow the desired $f_{\text{sys}} = 50\text{Hz}$ signal to pass through, the corner frequency (f_n) of the filter can be set to 250Hz, or the 5th order. This will give us $f_{\text{sys}} / f_n = 0.2$. For a second order system, this ratio will give us a gain of about 0dB. Hence:

$$\frac{1}{2\pi\sqrt{LC}} = 250$$

Another factor to consider is the characteristic impedance of the LC filter, i.e. $\sqrt{L/C}$ with respect to the load impedance $\sqrt{L/C} \ll |R_{\text{Load}} + j\omega L_{\text{Load}}| = 5.32 \Omega$

The following parameter values are determined for the LC filter:

Table 7.9: Parameter values for LC filter

Filter Components	Values
Corner Frequency (f_n)	250Hz
Characteristic Impedance	5.32
Inductance	0.106H
Capacitance	0.003F

7.3.6 DVR Design

The voltage of the faulted phase and the remaining other phases at the load on the low voltage side will depend on the system configuration, location of the fault, feeder impedance, distance of the fault and transformer connections between the fault system and load bus. For dimensioning of the DVR the following are essential: maximum power, maximum sag duration, minimum remaining voltage. The maximum duration from energy storage system is 500ms, thus a ride-through of 800ms should be sufficient.

The most fundamental characteristic of the Sinusoidal Pulse Width Modulation (SPWM) will be the amplitude modulation index $m_a = A_r / A_c$, where A_r is the modulated signal or

the reference and A_c is the triangular signal or the carrier and the ratio is 0 to 1.0. The m_a is set at 1.0 to cater for the worst case of 50% voltage sag. The series-connected injection transformer carries the full load current, the KVA rating S_{DVR} of the DVR is related to the maximum injection voltage and the KVA rating of the load S_{Load} as follows:

$$S_{DVR} = S_{Load} * \frac{V_{DVR,max}}{V_{Load}}$$

$$S_{DVR} = S_{Load} * \{ V_{DVR,max} \text{ in pu} \}$$

The phase voltage that can be inserted by the DVR is calculated as follows:

$$|V_{DVR}| = \frac{m_a V_d}{\sqrt{2}} * n \text{ KV}_{rms}, \text{ where}$$

$$= \left(\frac{V_{Sag}}{V_{tri}} * \frac{V_{dref}}{V_d} \right) * \frac{V_d}{\sqrt{2}} * n$$

n = injection transformer turns ratio.

Here with a V_d of 4.681KV \approx 5KV and a transformer turns ratio of 5KV / 0.8165 x 5KV, and considering 50% sag,

$$|V_{DVR}| = 0.5 * \frac{11KV}{\sqrt{3}} * \frac{1}{5KV} * \frac{6.531KV}{5KV} * \frac{5KV}{\sqrt{2}} * \frac{5KV}{5KV * 0.8165} = 3.753KV \approx 0.5pu. \text{ The}$$

rating of the device is thus approximately $0.5 * 1600 = 800KVA$. The DVR need not match the load rating as the DVR is only required to compensate for voltage sags, not outages.

7.3.7 The simulation system

Simulation were performed on the Ipoh hospital distribution system as shown in Figure 7.3, Appendix B. The value of impedances are calculated as follows:

$R_{cable} = 0.164 \Omega / Km$ and $X_{cable} = 80 \mu\Omega / m$ and impedance $Z = \sqrt{(1.64^2 + 2.4^2)} = 2.9 \Omega$ and source impedance (Z_S) and fault impedance (Z_f).

At 132KV end, the fault current for single phase fault is 5661A, double line-to-ground fault is 5452A and line-line fault is 5456A. The absolute source impedance:

$$Z_{SLGF} = \frac{132^2}{\sqrt{3} V_L I_L} = \frac{17424}{1.732 * 132 * 5661} = 13.46 \Omega$$

$$Z_{DLGF} = \frac{132^2}{\sqrt{3} V_L I_L} = \frac{17424}{1.732 * 132 * 5452} = 13.98 \Omega$$

$$Z_{LLF} = \frac{132^2}{\sqrt{3} V_L I_L} = \frac{17424}{1.732 * 132 * 5456} = 13.97 \Omega$$

Using the above data, the voltage sag will be as follows:

$$V_{SLGF} = \frac{Z_f}{Z_s + Z_f} = \frac{2.56}{13.46 + 2.56} = 16\%$$

$$V_{SDLGF} = \frac{Z_f}{Z_s + Z_f} = \frac{4.17}{13.98 + 4.17} = 23\%$$

$$V_{SLLF} = \frac{Z_f}{Z_s + Z_f} = \frac{3.94}{13.97 + 3.94} = 22\%$$

The purpose of this simulation is to study the capability of the DVR to regulate the load side voltage in the event of a fault. With reference to diagram in Appendix B, three simulations were carried out as follows; SLGF, DLGF and LLF. The fault is initiated at 0.6s. During the period of fault the voltage sagged by 0.16p.u, 0.23p.u, and 0.22p.u. as shown in Figure 7.4 – 7.17, respectively. In response to these voltage sags, the DVR injects a voltage V_{dvr} into the system, it will combine with the upstream system voltage to produce the compensated output voltage such that the load side voltage is maintained at its nominal value. With reference to Figure 7.5 and 7.7 , from the above measurement results:

Maximum level for V_A (Reference voltage)	= 8KV
Maximum level for v_a (Upstream system voltage)	= 6.5KV
Maximum level for v_{oa} (Output voltage)	= 8KV
% sag in Phase A (Downstream system voltage)	= v_a/V_A = $6.5/8 = 81.25\%$
% compensation achieved	= $v_{oa}/V_A = 100\%$

The drop in voltage is due to cable impedance. Hence the above calculations show that the DVR scheme presented is indeed capable of compensating for the sagged system. The compensation achieved in this case is 100% for a sag of 81.25%. This clearly shows that in terms of magnitude compensation the DVR/SPWM system is able to meet the requirements of the Computer Business Equipment Manufacture Association (CBEMA) standard. The simulation results revealed that the DVR responded well within 8ms.

Voltage tracking is achieved by the phase-locked loop (PLL) control loop. The phase-locked loop is loaded onto phases V_{arec} , V_{brec} and V_{crec} . The control frequency of the PLL is set at 33 (33th order). The injected voltage is the difference between the received end voltage per phase and the line voltage per phase. The difference is multiplied by $\sqrt{3}$ to form the line voltage of the series winding.

7.4 Verification of simulated results

All calculations are performed by using the per-unit (p.u) system.

Using data from Table 7.1 and 7.2:

Positive (Z_+), Negative (Z_-) and Zero (Z_0) sequence impedances are;

Source at 132KV, Base 100MVA:

$$Z_+ = (0.01410^2 + 0.08480^2)^{1/2} = 0.08596$$

$$Z_- = 0.08596 \text{ (assuming } Z_+ = Z_-)$$

$$Z_0 = (0.10320^2 + 0.05889^2)^{1/2} = 0.119$$

Transformer at 132/11KV, Base 100MVA:

$$Z_+ = (0.0104^2 + 0.0994^2)^{1/2} = 0.0999$$

$$Z_- = 0.0999 \text{ (assuming } Z_+ = Z_-)$$

$$Z_0 = (3.0^2 + 0.0994^2)^{1/2} = 3.0016$$

- a. Single Line-to-Ground Fault at Phase A Node Bus JawaT2

$$\text{Condition } V_A = 0, I_B = I_C = 0$$

Using the equivalent circuit:

$$I_{A1} = \frac{1\angle 0^\circ}{Z_1 + Z_2 + Z_0} = \frac{1\angle 0^\circ}{0.1859 + 0.1859 + 3.1206} = \frac{1\angle 0^\circ}{j3.4924} = -j0.286$$

$$I_A = \frac{3E}{Z_1 + Z_2 + Z_0} = \frac{3\angle 0^\circ}{j3.4924} = -j0.859$$

$$V_{A1} = E - I_{A1}Z_1 = 1 - (-j0.286 * j0.1859) = 0.9468 \text{ pu}$$

$$V_{A2} = -I_{A2}Z_2 = -(-j0.286 * j0.1859) = -0.0532 \text{ pu}$$

$$V_{A0} = -I_{A0}Z_0 = -(j0.286 * j3.1206) = -0.8925 \text{ pu}$$

$$V_A = 0.9468 - 0.0532 - 0.8925 = 0.0011 \sim 0 \text{ pu}$$

Similarly,

$$V_B = a^2V_{A1} + aV_{A2} + V_{A0}$$

$$0.9468(-0.5-j0.866) - 0.0532(-0.5+j0.866) - 0.8925$$

$$-1.3368-j0.8659 = 1.5 \text{ pu}$$

$$V_C = aV_{A1} + a^2V_{A2} + V_{A0} = 1.5 \text{ pu (Conjugates)}$$

$$|I_f| = \frac{3 * V_{ph}}{j(Z_1 + Z_2 + Z_0 + 3R_f)}$$

Fault current $I_f = 1030 \text{ A}$. (Simulation value is 1112.54A)

b. Double Line-to-Ground Fault at Phase AB at Bus JawaT2

Condition : $V_A = V_B = 0, I_A = 0$

$$I_{A1} = \frac{E}{Z_1 + \frac{Z_2 Z_0}{Z_2 + Z_0}} = \frac{1\angle 0^\circ}{j0.1859 + \frac{j0.1859 * j3.1206}{j3.3065}} = \frac{1}{j0.1859 + j0.175} = -j2.76$$

$$I_{A2} = -I_{A1} \frac{Z_0}{Z_2 + Z_0} = -(-j2.76) \left(\frac{j3.1206}{j0.1859 + j3.1206} \right) = j2.605$$

$$I_{A0} = -I_{A1} \frac{Z_2}{Z_2 + Z_0} = -(-j2.76) \left(\frac{j0.1859}{j0.1859 + j3.1206} \right) = j0.155$$

$$V_{A1} = 1 - I_{A1}Z_1 = 1 - (-j2.76 * j0.1859) = 0.484$$

$$V_{A2} = -I_{A2}Z_2 = -(j2.605 * j0.1859) = 0.484$$

$$V_{A0} = -I_{A0}Z_0 = -(j0.155 * j3.1206) = 0.484$$

$$V_C = V_{A1} + V_{A2} + V_{A0} = 1.45\text{pu}$$

$$V_B = a^2V_{A1} + aV_{A2} + V_{A0} = 0.487 * (-0.5-j0.866) + 0.484 (-0.5+j0.866) + 0.48 \\ = 0 \text{ pu}$$

$$V_A = aV_{A1} + a^2V_{A2} + V_{A0} = 0 \text{ pu (Conjugates)}$$

Fault current I_f is calculated as follows:

$$\text{Total impedance } Z_t = Z_1 + Z_2 + \frac{Z_0 * R_f}{Z_0 + R_f} = 0.41\text{pu.}$$

$$I_{a1} = \frac{1}{0.41} = 2.43$$

$$I_a = \sqrt{3} * 2.43 = 4.21\text{pu}$$

$$I_f = \frac{100\text{MVA}}{\sqrt{3} * 11000} * 4.21 = 22098\text{A (Simulation value is 19885.66A)}$$

c. Line-to-line fault

$$\text{Total impedance } Z_t = Z_1 + Z_2 + R_f = 0.44\text{pu.}$$

$$I_{a1} = -I_{a2} = \frac{1}{0.44} = 2.27$$

$$I_a = \sqrt{3} * 2.27 = 3.94\text{pu}$$

$$I_f = \frac{100\text{MVA}}{\sqrt{3} * 11000} * 3.94 = 20858\text{A (Simulation value is 18261.49A)}$$

There is a slight variation between the calculated values and the simulation results, as shown in (Appendix F). The difference is due to the approximation values used for source, transformer and cable properties respectively. The symmetrical component is explained in Appendix G [18].

7.5 Conclusion

The depth of sag depends upon the fault resistance at the point of fault and the source impedance. Sensitive equipments that do not have the ride through capability under this condition will mal-operate. Installing the uninterruptible power supply (UPS) is one of most common solution. The transformer winding connections between the point of fault and the equipment terminals attributes to the different voltage pattern at the various nodes.

The PSCAD/EMTDC simulation tool was used in the study of power quality and also model implementation and to carry out simulation studies. Custom power equipment, namely DVR was modeled to mitigate voltage sag and was connected at the 11KV BUS JAWAT2. When DVR is in operation the voltage sag is mitigated almost completely. The simulation carried out showed that the DVR provides good voltage regulation. The capacity of power consumption and voltage regulation depends on two factors: the rating of the dc voltage to the inverter and the characteristics of the series transformer.

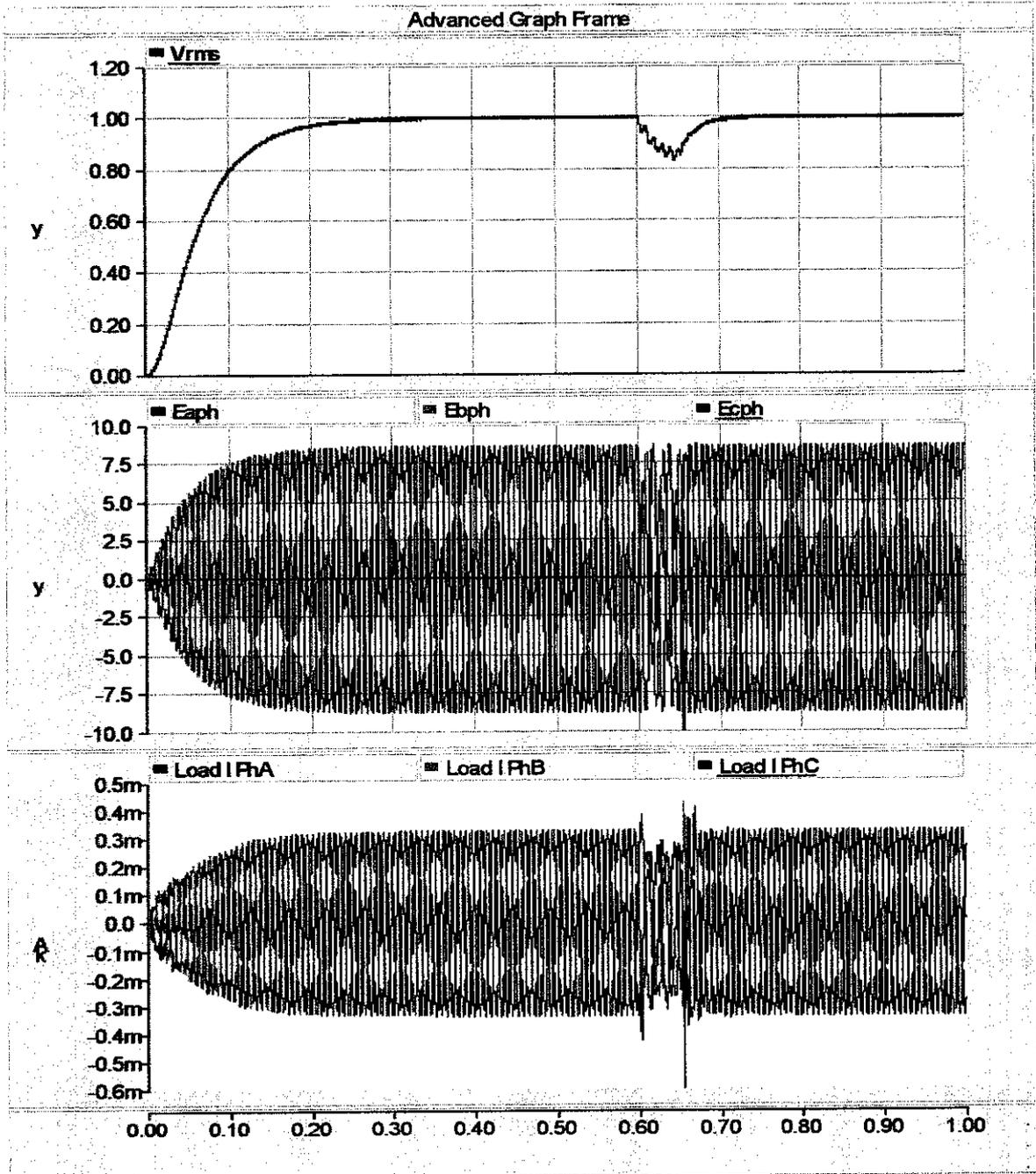


Figure 7.4: Single line-to-ground fault with 16% sag.

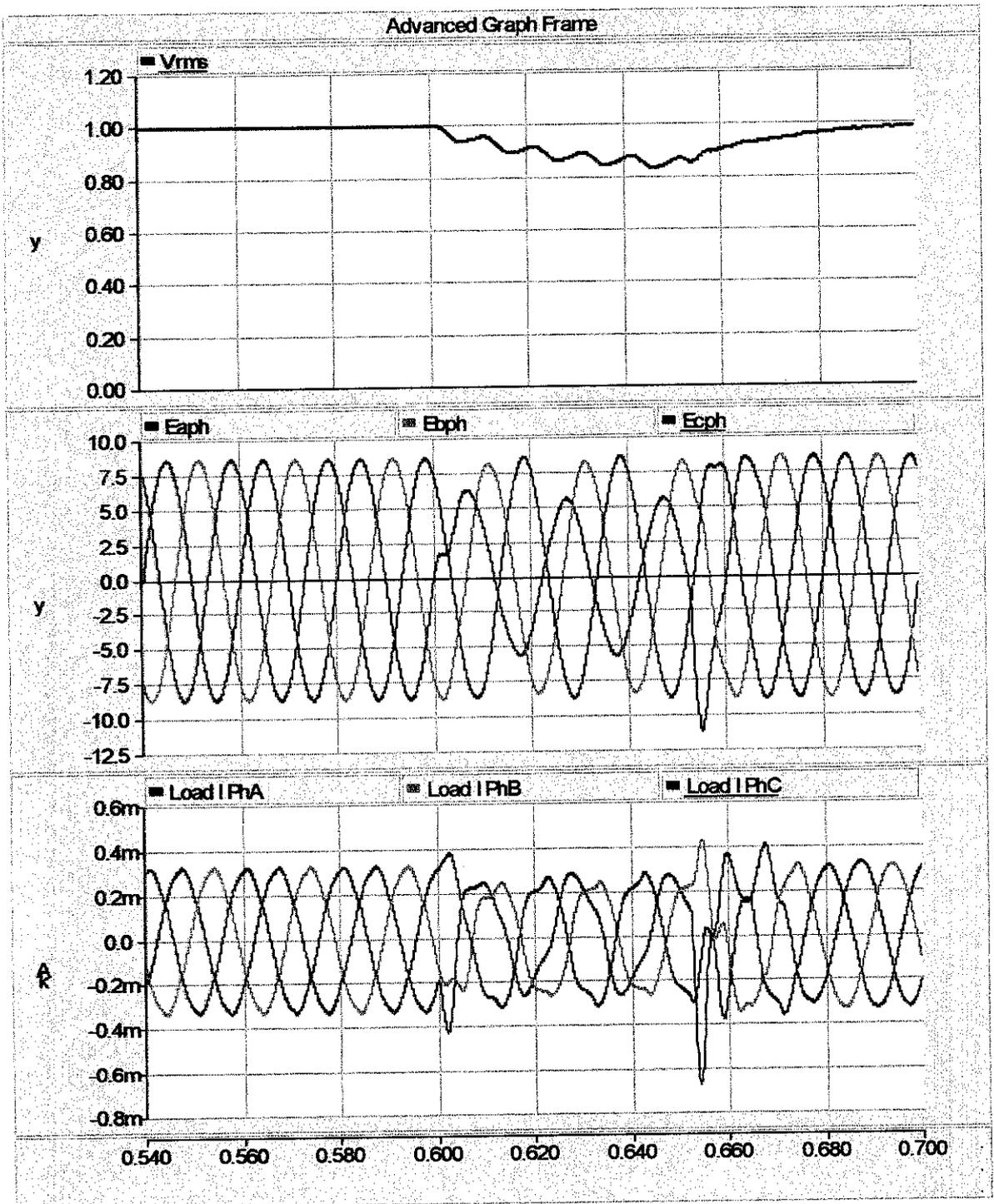


Figure 7.5: Single line-to-ground fault without DVR extended view

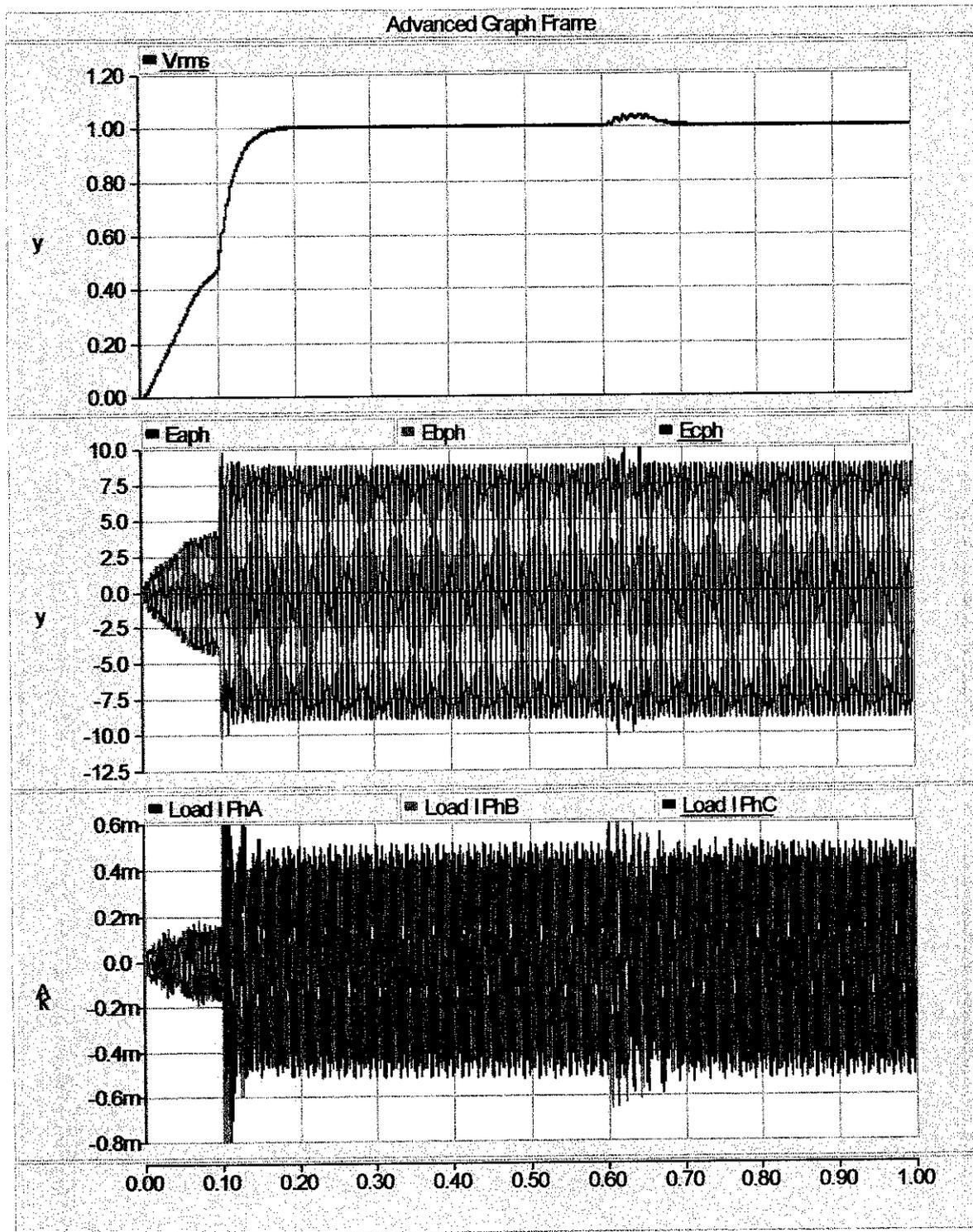


Figure 7.6: Single line-to-ground with DVR in operation

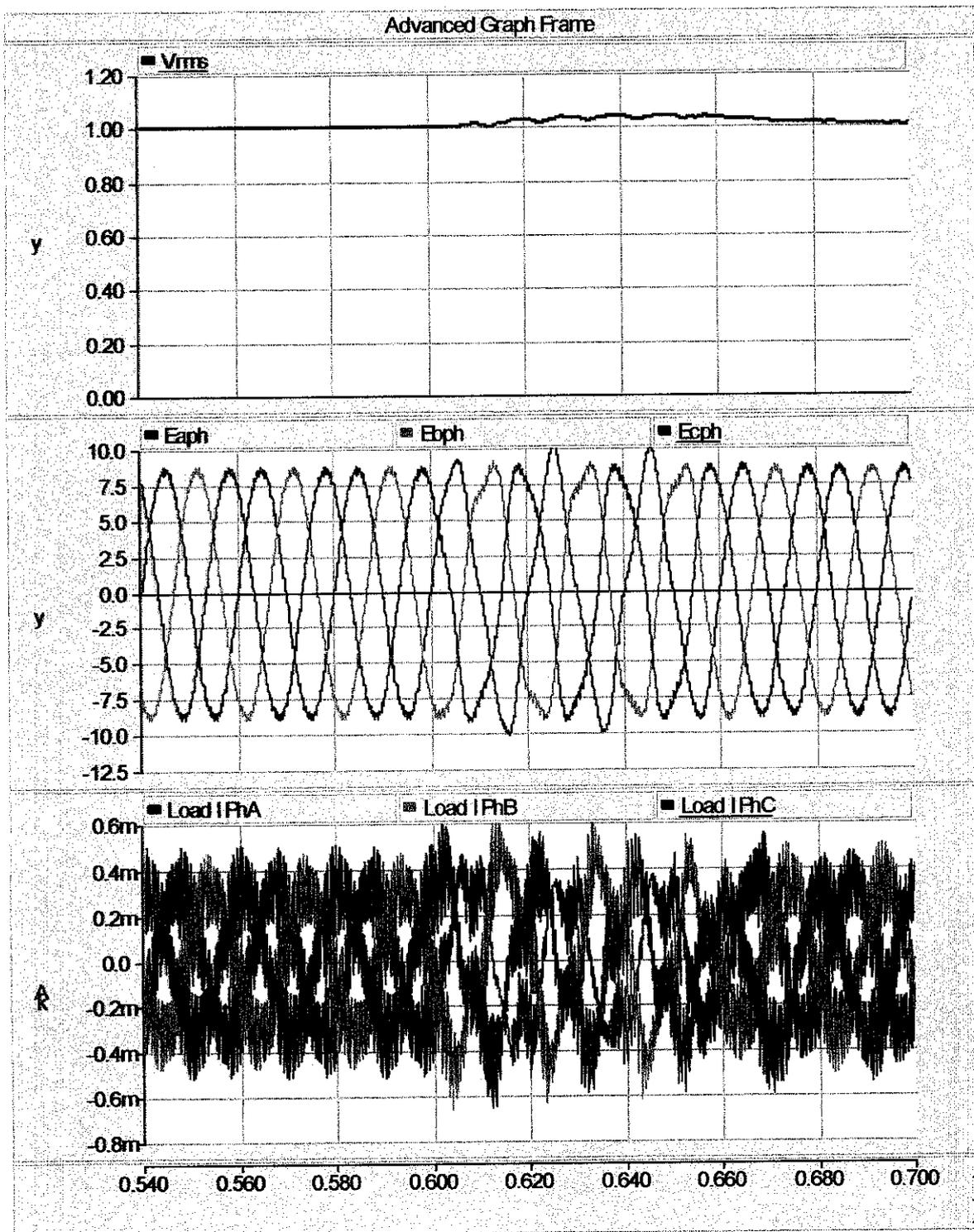


Figure 7.7: Single line-to-ground fault with DVR in operation extended view.

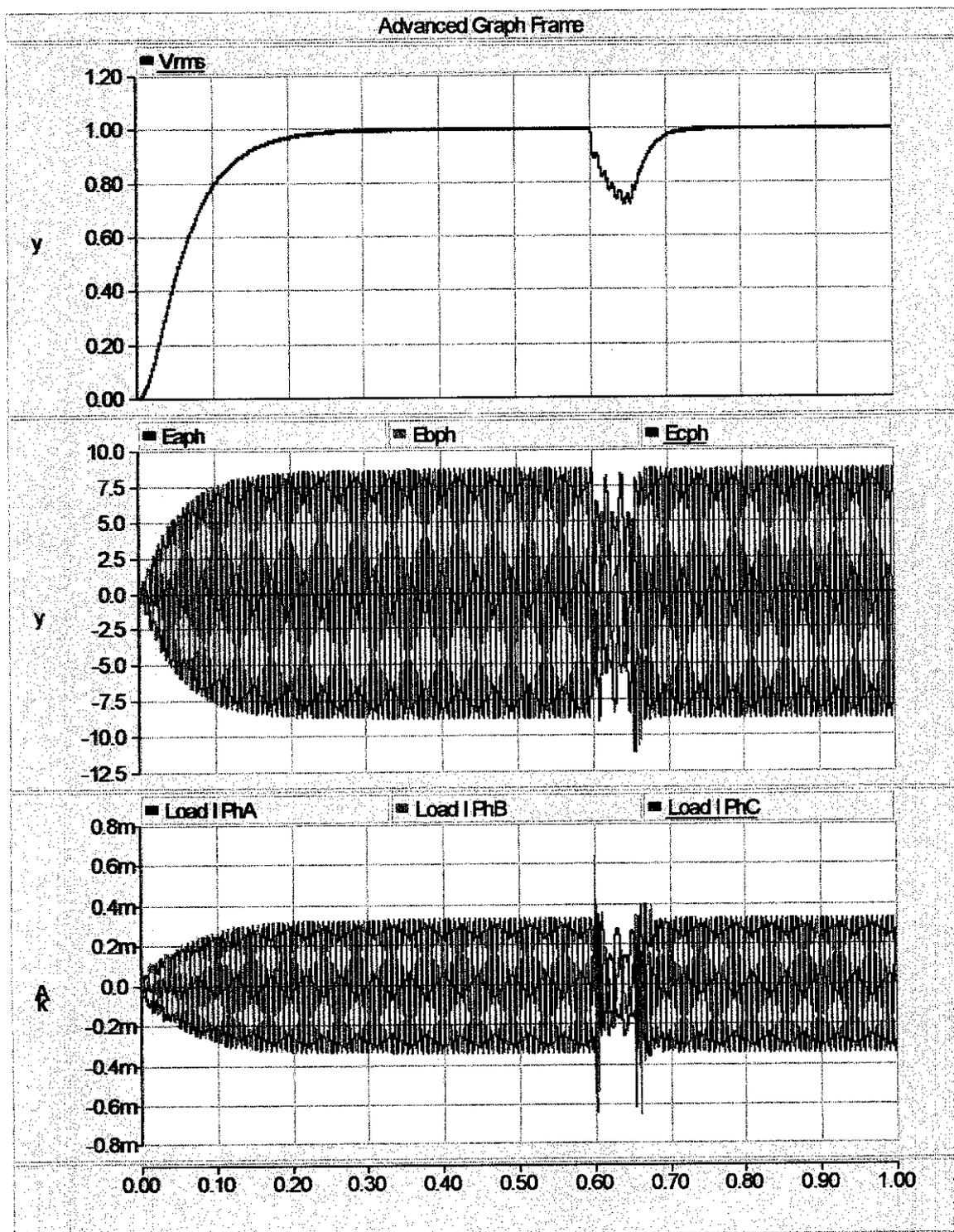


Figure 7.8: Double line-to-ground fault with 23% sag.

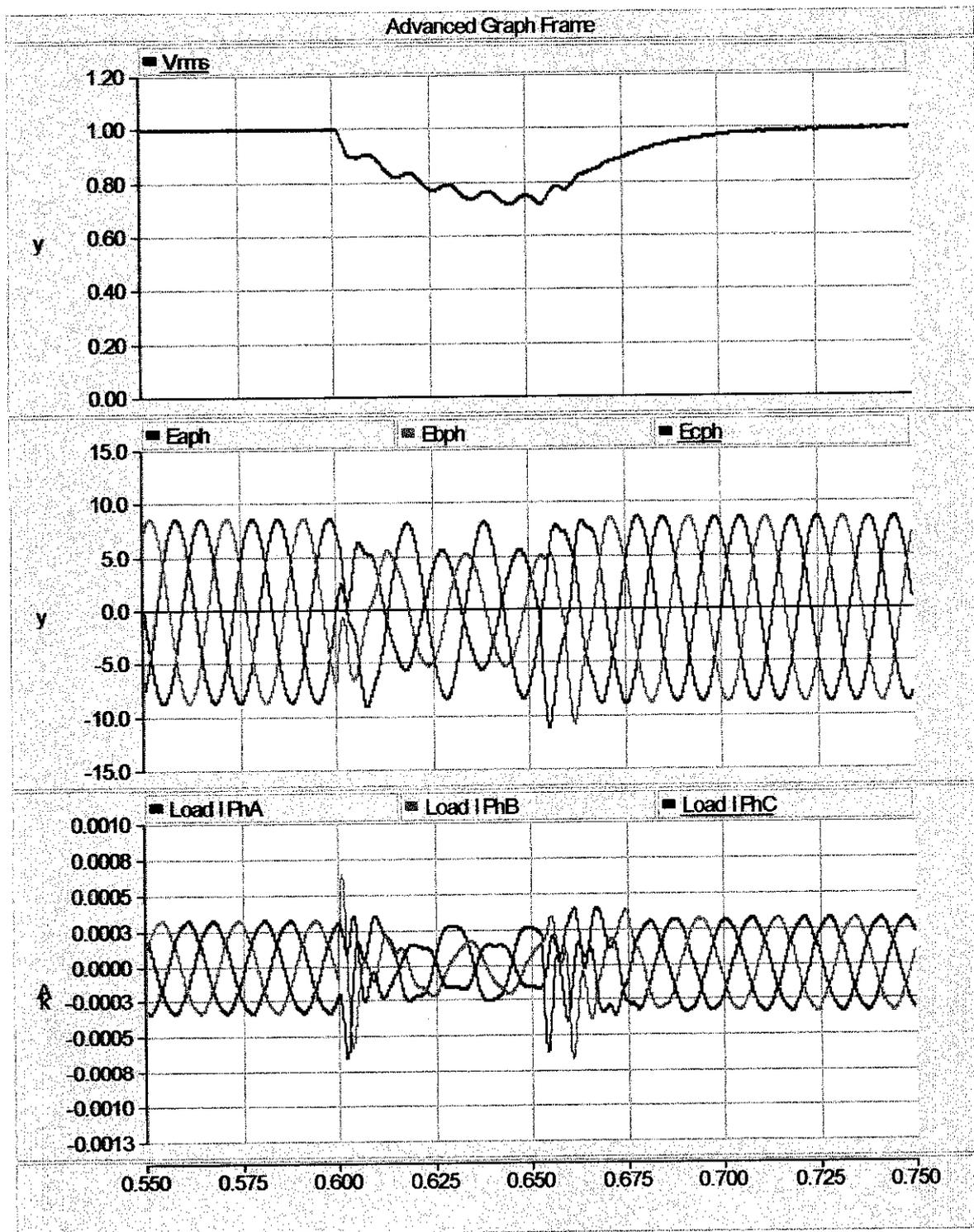


Figure 7.9: Double line-to-ground fault without DVR extended view.

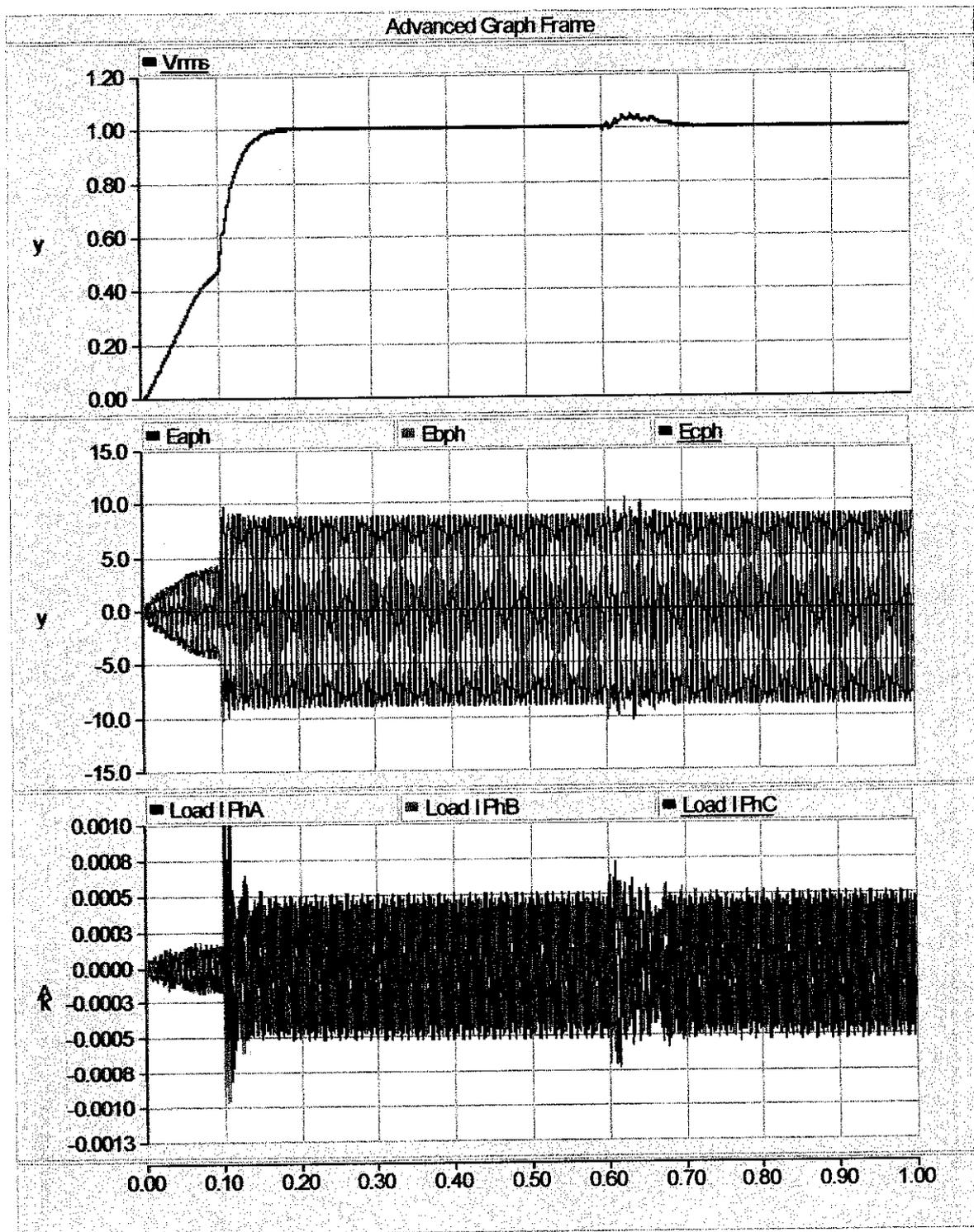


Figure 7.10: Double line-to-ground fault with DVR in operation.

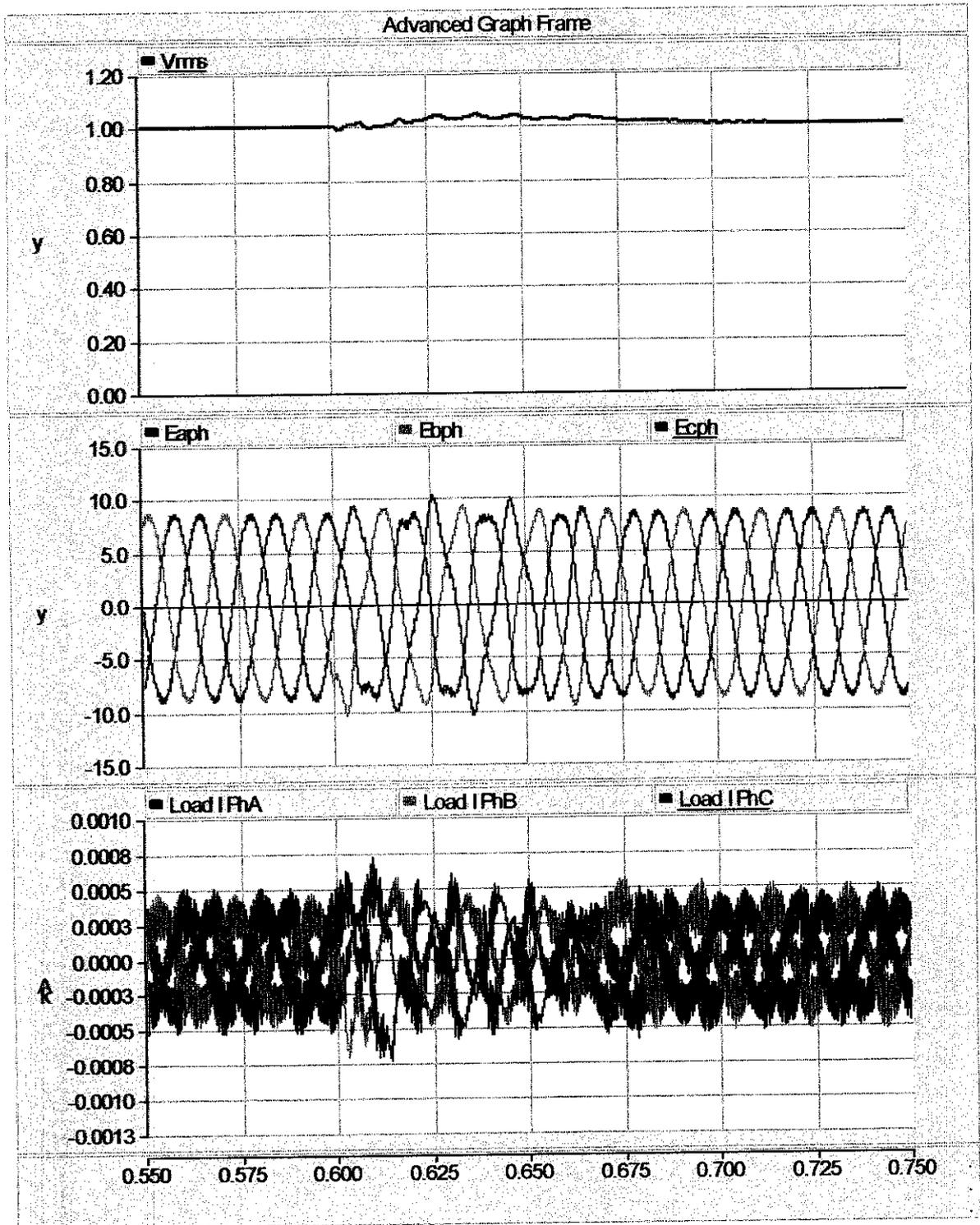


Figure 7.11: Double line-to-ground fault with DVR in operation extended view.

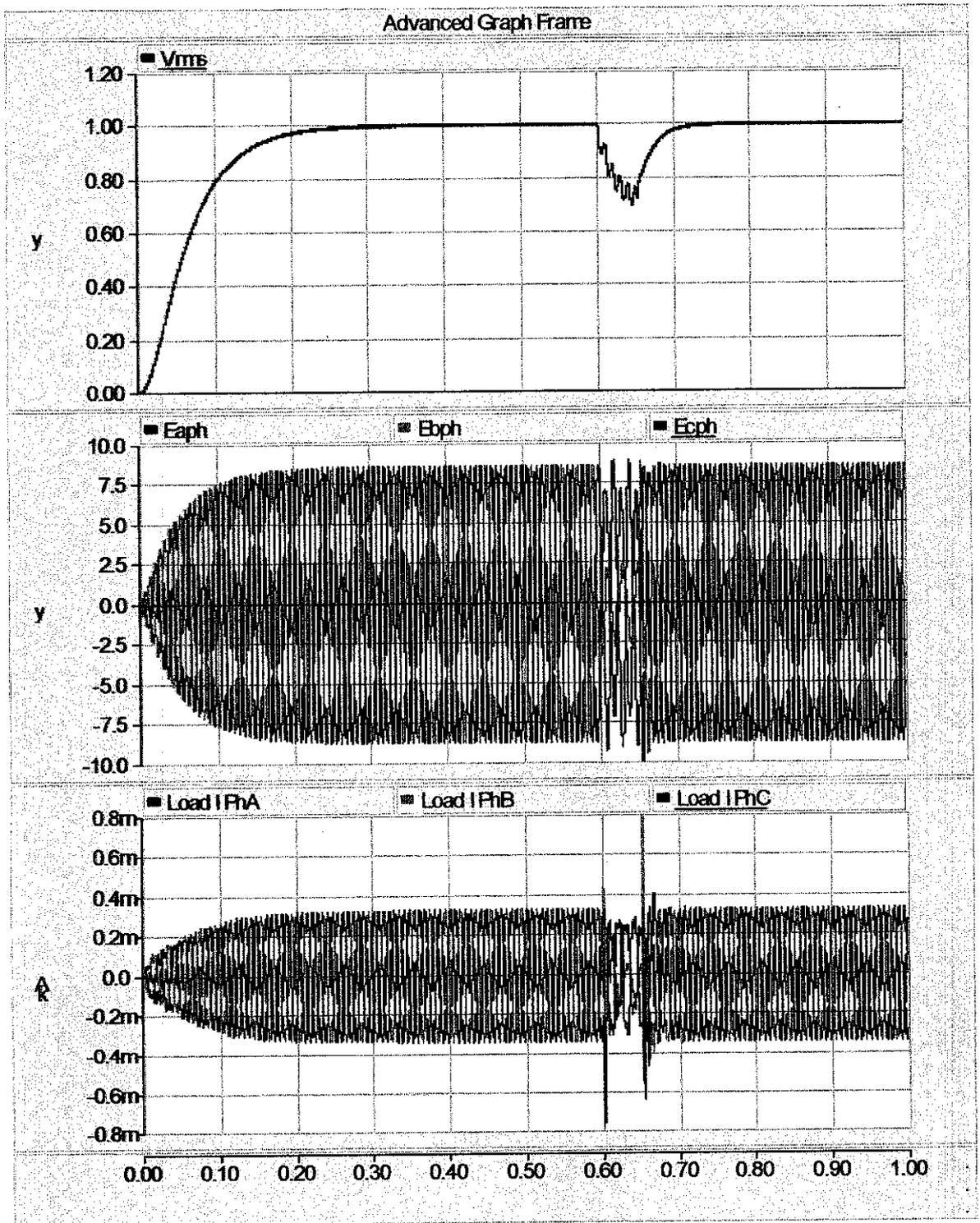


Figure 7.12: Line-to-line fault with 22% sag

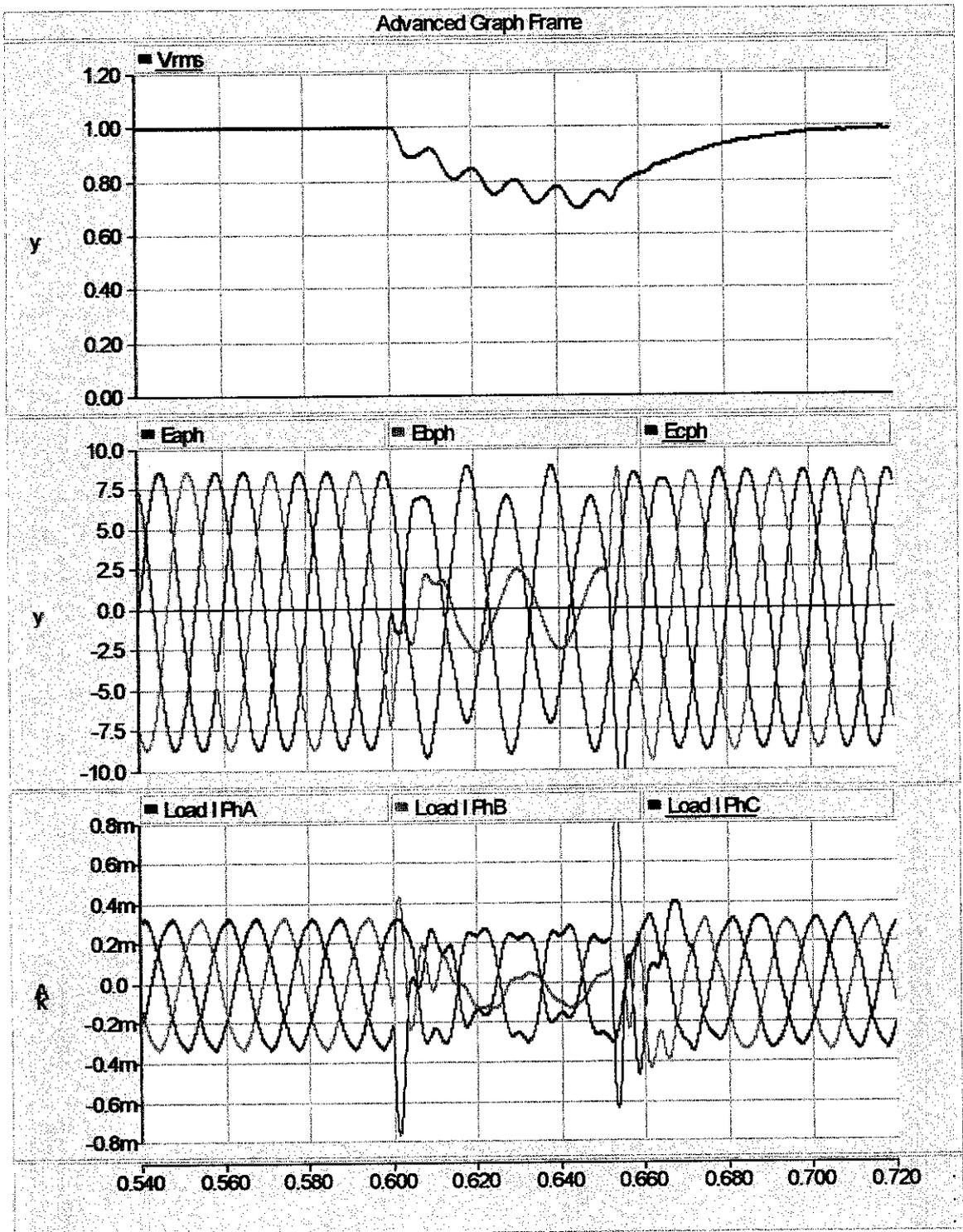


Figure 7.13: Line-to-line fault without DVR extended view.

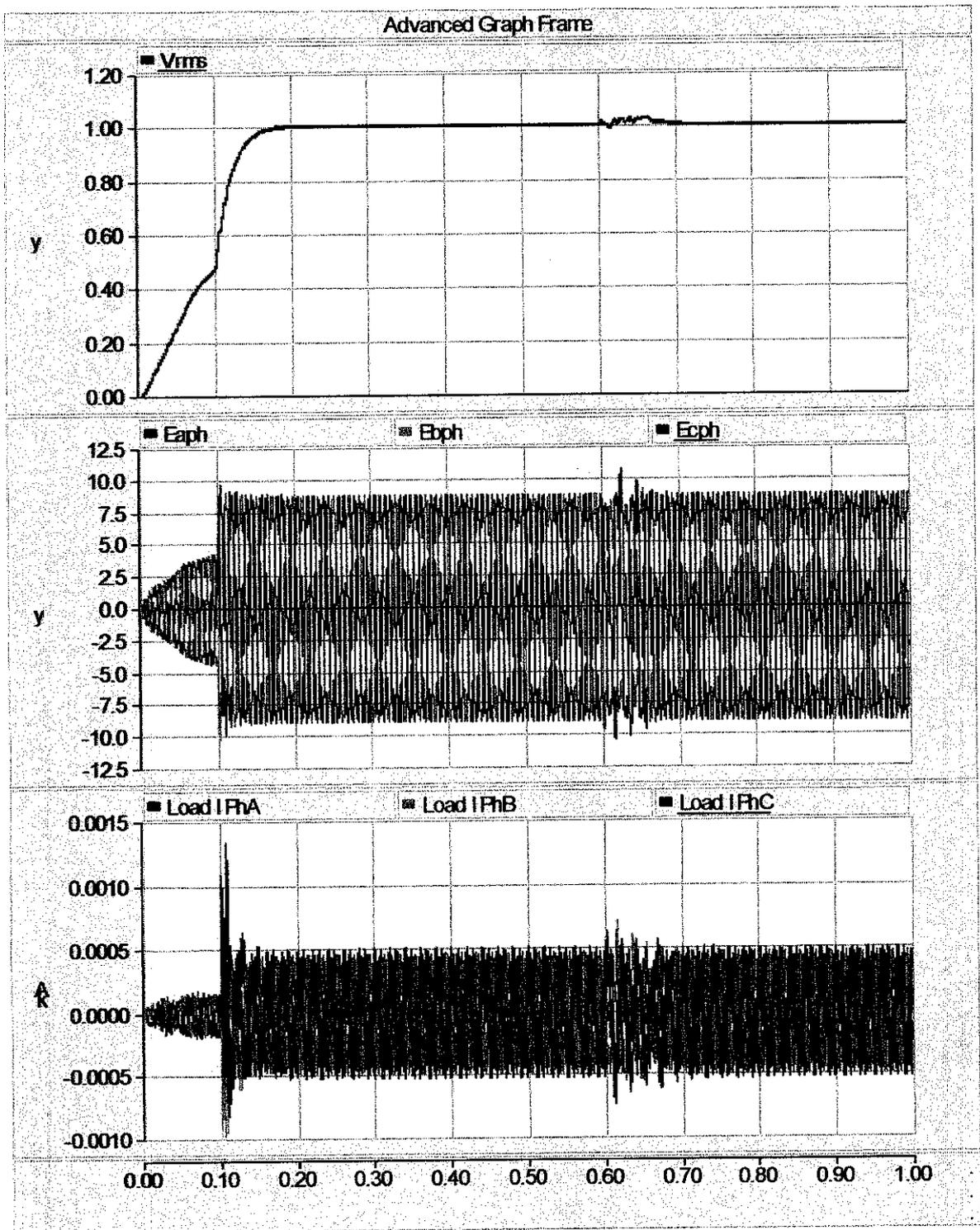


Figure 7.14: Line-to-line fault with DVR in operation.

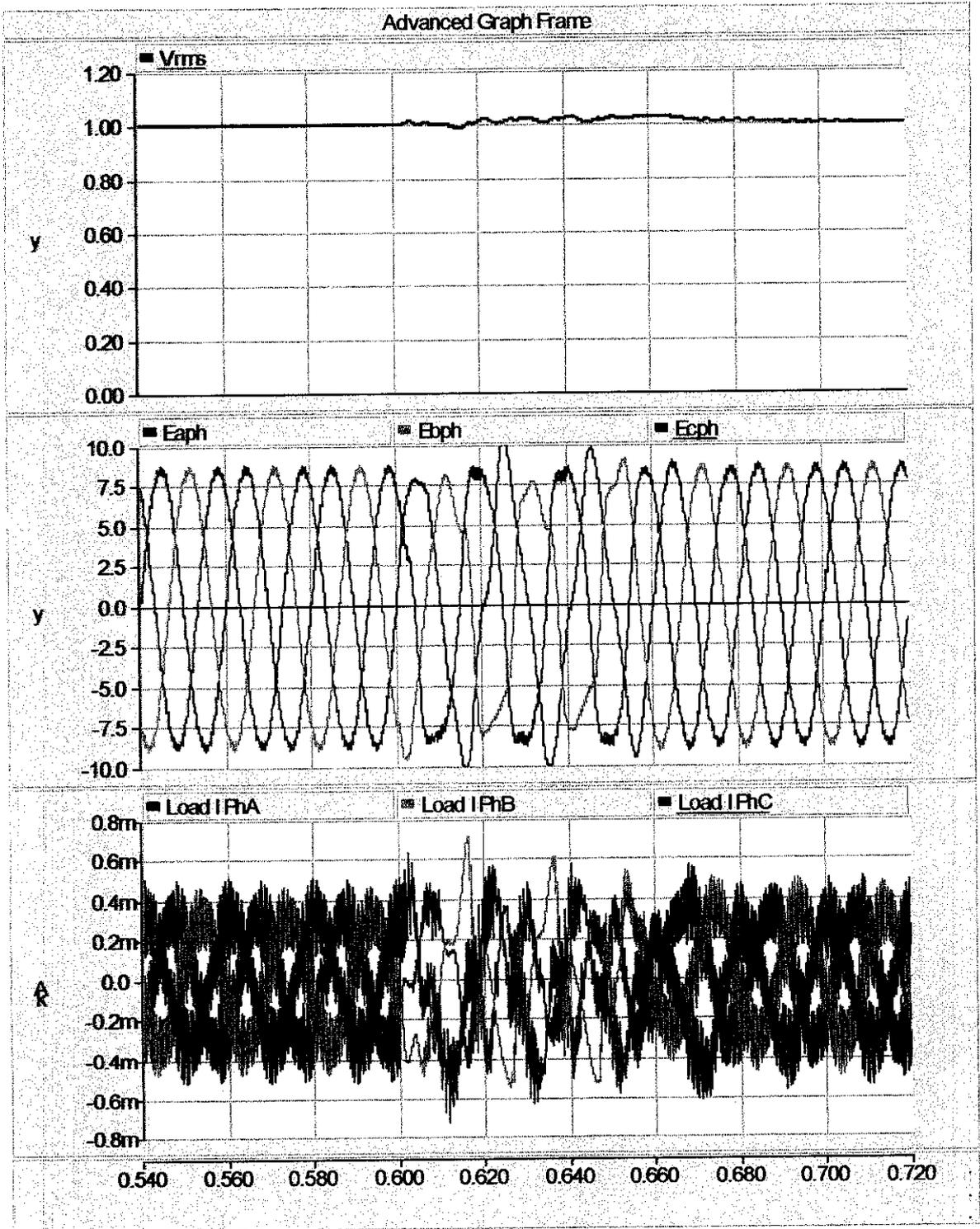


Figure 7.15: Line-to-line fault with DVR in operation extended view

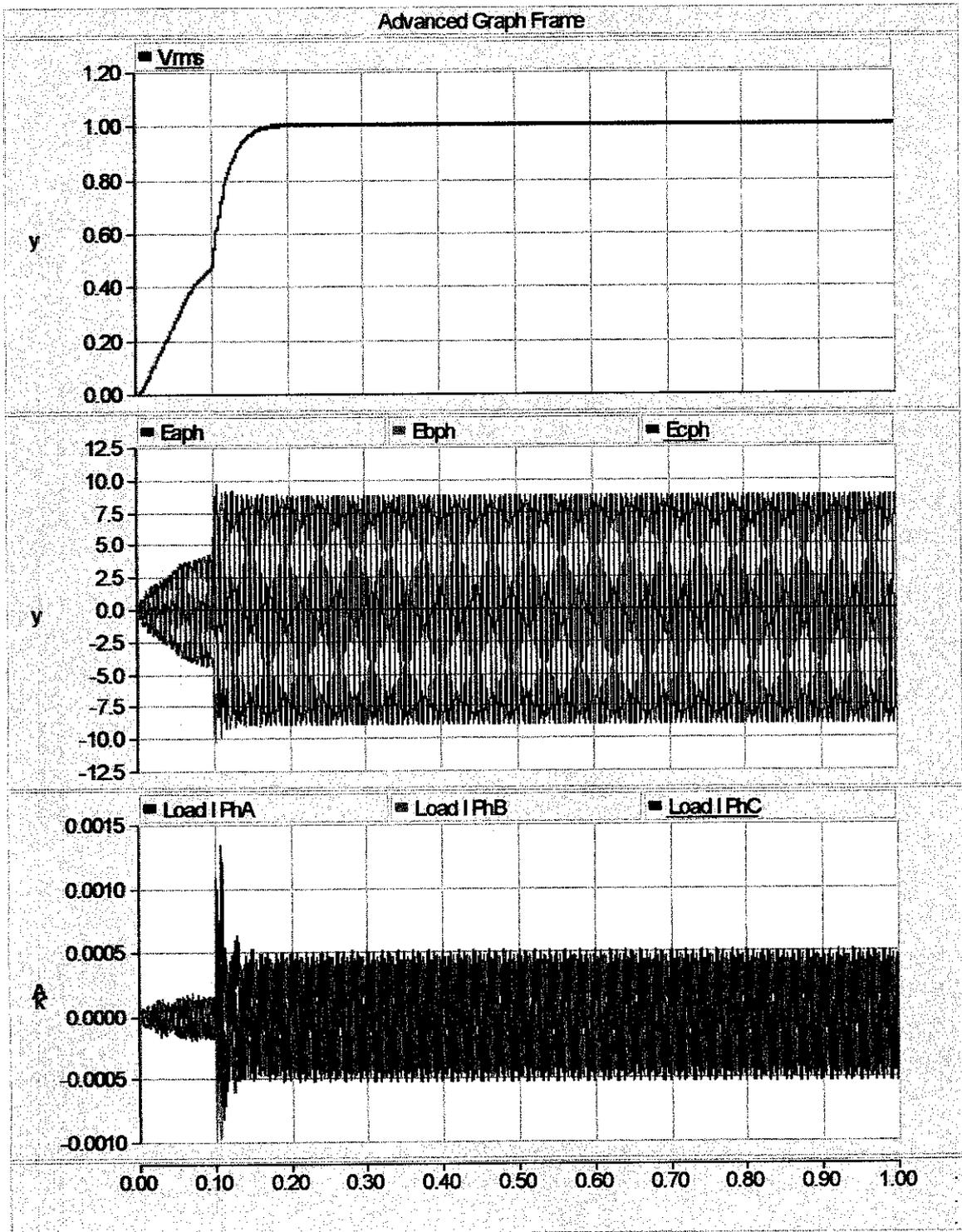


Figure 7.16: Upstream voltage before fault

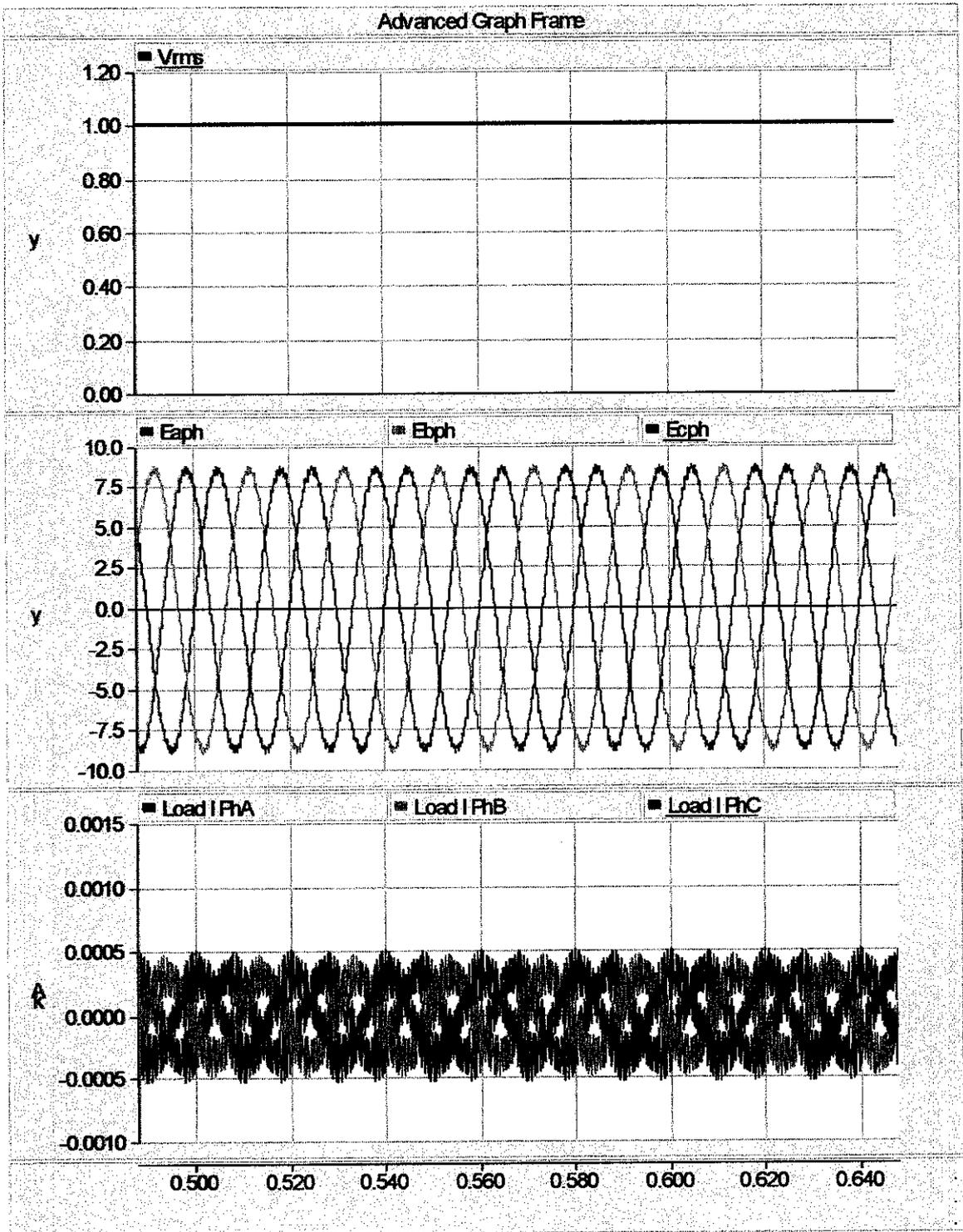


Figure 7.17: Voltage at load end before fault and without DVR

CHAPTER 8
CONCLUSION AND RECOMMENDATIONS

CHAPTER 8

CONCLUSION AND RECOMMENDATIONS

The topic of this thesis is modeling and simulation of power quality disturbances and the mitigation of voltage sags. The main interest in this project is the use of Dynamic Voltage Restorer (DVR) to mitigate the voltage sags. This chapter gives a summary of the thesis as well as conclusions from the research work and some recommendations.

8.1 Summary

Voltage sag is a short duration reduction in rms voltage primarily caused by faults on the power system or starting large motors.

In order to decrease the problems caused by voltage sags three different ways can be considered:

- decrease the probability that a voltage sag will occur
- decrease the magnitude and duration of the voltage sag
- decrease the impact of a voltage sag

To decrease the probability of voltage sags, over-head lines can be replaced by cables. The number of faults induced by lightning can be reduced by use of surge arresters, wooden cross arm on transmission and distribution lines and improve the earthing system.

Installing custom power device is another way of lowering the severity of voltage sags. The Dynamic Voltage Restorer (DVR) is a mitigation device to compensate voltage sag. The impact from voltage sags on equipments can be reduced if the end-user equipment has the ride through capability to tolerate voltage sags.

8.1.1 Network splitting

Different topologies have been discussed including network splitting or splitting the buses to decrease the magnitude and duration of voltage sags. If the faulted parts can be isolated fast, the severity of the fault can be reduced.

Reconnection of a generator near sensitive loads increases the short-circuit capacity of the system and makes voltage sags less severe.

8.1.2 The Ipoh Hospital case study

The Ipoh Hospital distribution system has been chosen for the voltage sag study where the voltage sag can disturb the life saving equipments and cause economical losses and hazards to hospital staff and the public. The major part of the voltage sags comes from the feeding network. The Dynamic Voltage Restorer (DVR) is connected on the 11KV feeder supply to Ipoh hospital, in reducing the voltage sags, that affect the operation of sensitive loads in the hospital as well as at the source.

Real time measurement with Reliable Power Meter (RPM) recorder was installed to record the events to study the impact of voltage disturbances on the sensitive equipments. Power analysis summary relating to Ipoh hospital distribution system is shown in Appendix E.

Simulation was done using two software packages. PSS/ADEPT was used to show the voltage sag magnitude at various nodes under fault conditions. PSCAD was used to model and simulate sag waveform under various fault conditions in the system including the mitigation of voltage sag using Dynamic Voltage Restorer (DVR).

8.2 Recommendations

An interesting area for research will be incorporating both the low and high voltage custom power device as a unit to mitigate voltage sag and also study the influence of transition and harmonics. We can also determine the active and reactive power injection of DVR for estimating the optimum size of the DVR energy storage.

8.3 Conclusion

Voltage sags are the most severe type of power quality disturbances that often affect the performance of modern electrical equipments. To mitigate the impact of voltage sags in the most cost effective manner, the severity of the voltage sags at the point of interest needs to be determined. Monitoring power quality is a common way of obtaining the severity of voltage sags. Simulation by method of fault position is a voltage-sag prediction method. However, to facilitate accurate modeling of fault conditions on a complicated network stochastic prediction methods or method of critical distance can be applied.

For this project, the effectiveness of Dynamic Voltage Restorer (DVR) is evaluated on utility feeder supplying the Ipoh hospital, under various fault conditions, the distribution system is likely to face. The various features and technology involved in the DVR system design and detailed block schematic DVR design has been presented. This design is useful in control and simulation studies of the DVR system. Both the voltage-mode and current-mode control PWM scheme has been discussed. The evaluation is based on simulations using PSS/ADEPT and PSCAD/EMTDC software packages.

REFERENCES

References

- [1] Dungun R.C, Beaty H.W, "Electrical Power Systems Quality", New York: McGraw-hill, 1996.
- [2] Math H.J. Bollen, "Understanding Power Quality Problems": Voltage sags and Interruptions, New York, IEEE press, 2000.
- [3] Philippe Ferracci, Power Quality Notes: no. 199, ECT 199(e) October 2001.
- [4] Vic Gosbell, "Understanding Power Quality" Technical Note No.1 June 1998.
- [5] John H. Waggoner, "Power Quality and Harmonics", Energy User News, 2000.
- [6] Electricity Supply Application Handbook by TNB
- [7] SARFI, Technical paper, file://A:SARFI htm. 04/22/2002.
- [8] Vic Gosbell, University of Wollongong, "Voltage Sag measurement and Characterization", Technical Note No.4, June 2001.
- [9] Brooks D.L., Dugan R.C, "Indices for Assessing Utility Distribution System RMS Variation performance", Electrotek Concepts, Inc.
- [10] Manitoba HVDC Research Centre Inc., PSCAD/EMTDC Manual.
- [11] PSS/ADEPT™, <http://www.shawgrp.com/PTI/software/adept/index.cfm>.
- [12] Yop Chung, "Control and Analysis of zero sequence components in DVR system", IEEE, 2001. <http://www.ee.snu-ac.kr/paper/publications>.
- [13] Ambra Sannino, "Mitigation of Voltage Sags and Short Interruptions through Distribution System Design", University of Palermo, Italy, 2001. <http://www.elkraft.chalmers>.
- [14] Nick Jenkins, Goran Strbac, "An investigation of Network Splitting for Fault Level Reduction", UMIST, UK, Working paper No.25, January 2003.
- [15] B.M. Bird, K.G. KING, D.A.G. PEDDER, "An Introduction to Power Electronics", John Wiley & Sons, 1993
- [16] Muhammad Harunur Rashid, "Power Electronics Circuits Devices and Application", Prentice-Hill International, Inc. 1993
- [17] Olimpo Anaya Lara, "Modeling and Analysis of Custom Power Systems by PSCAD/EMTDC", IEEE Transactions on Power Delivery, Vol.17, No.1, January 2002. [http://www.cedraft-grenable.fr/applications/power systems simulator](http://www.cedraft-grenable.fr/applications/power%20systems%20simulator).

- [18] Bowest Pty Ltd, <http://www.bowest.com.au/library/electric.htm1#09>.

PUBLICATIONS

PUBLICATIONS

1. "Power Quality Disturbances" Bulletin Institution of Engineers, Malaysia (IEM) Perak Branch, 2002.
2. Presentation "Modeling, Simulation and Analysis of Power Quality Disturbances" Tenaga Nasional Berhad Conference (TNB), February 2004.
3. "Modeling, Simulation and Analysis of Power Quality Disturbances" paper acceptance to International Association of Science and Technology for Development (IASTED) Conference, 2004.
4. "Modeling, Simulation and Analysis of Power Quality Disturbances" paper acceptance to International Conference on Electrical, Electronic and Computer Engineering (ICEEC), 2004.
5. "Simulation and Mitigation of Power Quality Disturbances using DVR", International Journal of Power and Energy System, ACTA Press USA Sept 2004.

APPENDIX

Appendix A

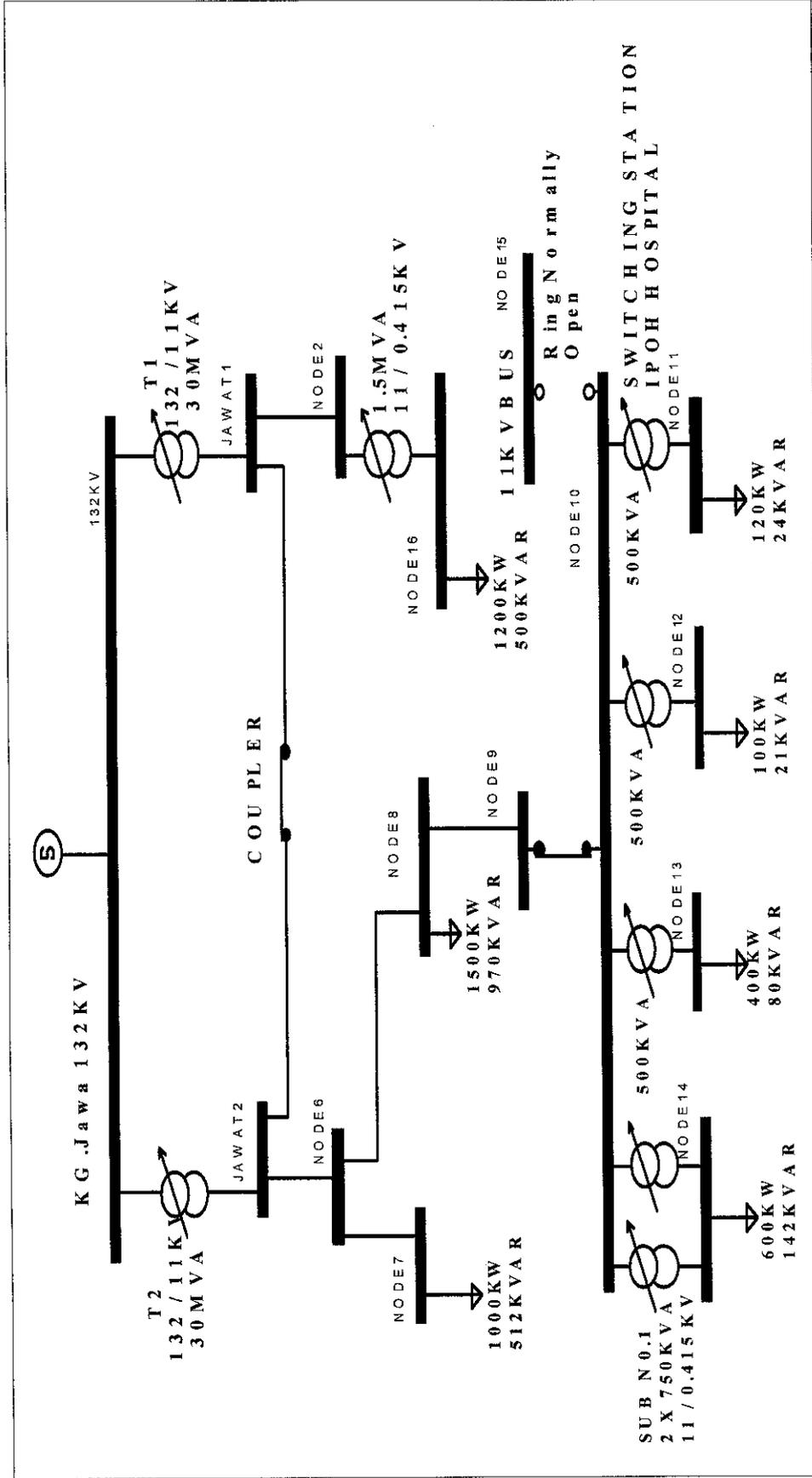
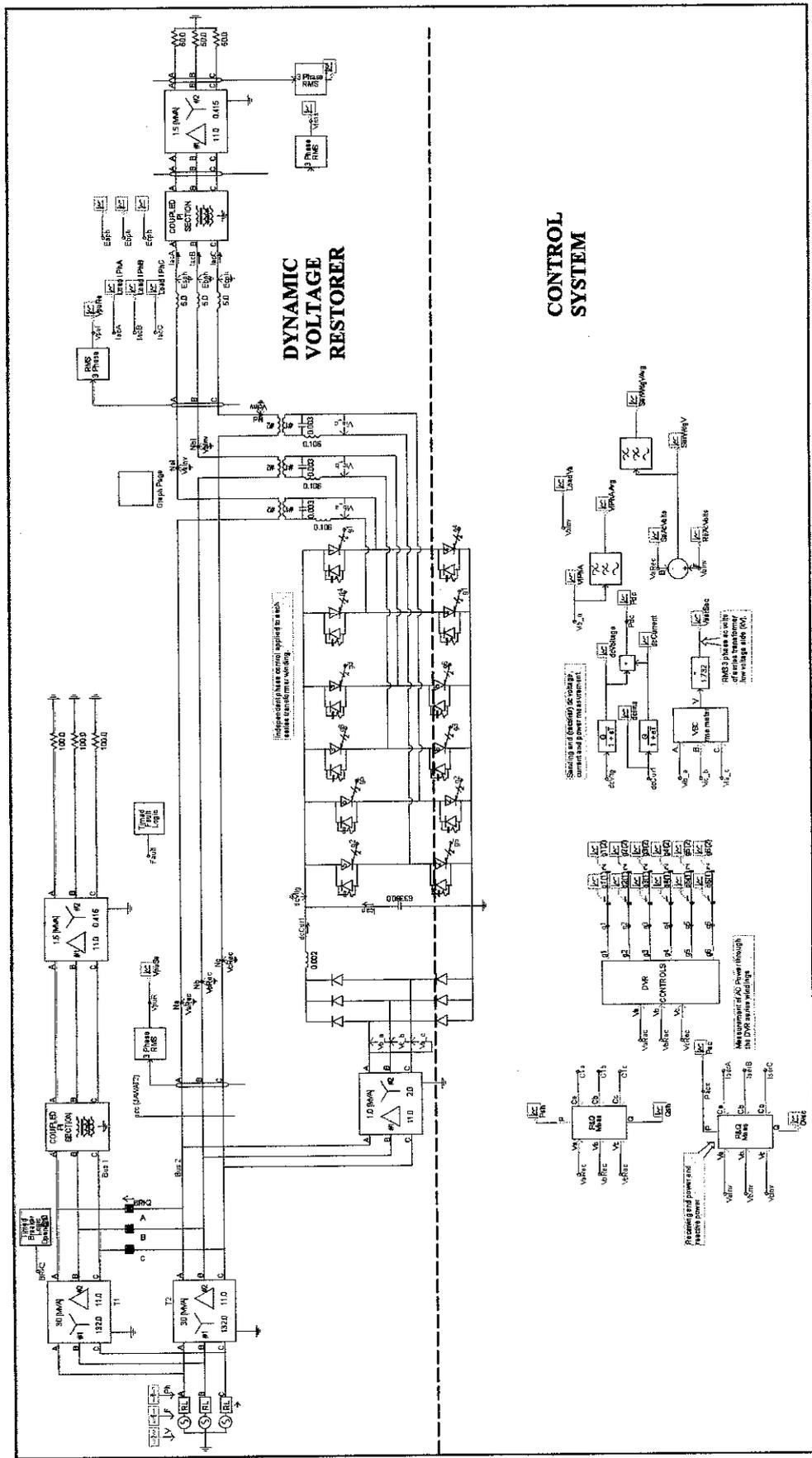


Figure 7.2: Ipoh hospital distribution system in PSS / ADEPT

Appendix B

Figure 7.3: Ipoh hospital distribution system in PSCAD



Appendix C

Table 7.4: Single Phase-to-Ground Fault on Phase A at Bus JawaT2

	JawaT2	Node 6	Node 7	Node 8	Node 9	Node 10	Node 11	Node 12	Node 13	Node 14
Phase A	0V	0V	0V	0V	0V	0V	249V 1.0pu	249V 1.0pu	249V 1.0pu	249V 1.0pu
Phase B	8287V 1.3pu	8065V 1.3pu	8065V 1.3pu	7982V 1.3pu	7959V 1.3pu	7959V 1.3pu	178V 0.7pu	178V 0.7pu	178V 0.7pu	178V 0.7pu
Phase C	11594V 1.8pu	11416V 1.8pu	11404V 1.8pu	11326V 1.8pu	11291V 1.8pu	11291V 1.8pu	241V 1.0pu	241V 1.0pu	241V 1.0pu	241V 1.0pu

Table 7.5: Double Line-to-Ground Fault on Phase AB at Bus JawaT2

	JawaT2	Node 6	Node 7	Node 8	Node 9	Node 10	Node 11	Node 12	Node 13	Node 14
Phase A	0V	0V	0V	0V	0V	0V	203V 0.9pu	203V 0.9pu	203V 0.9pu	203V 0.9pu
Phase B	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V
Phase C	9474V 1.5pu	9248V 1.5pu	9236V 1.5pu	9148V 1.5pu	9113V 1.4pu	9113V 1.4pu	203V 0.9pu	203V 0.9pu	203V 0.9pu	203V 0.9pu

Table 7.6: Line-to-line Fault on Phase AB at Bus JawaT2

	JawaT2	Node 6	Node 7	Node 8	Node 9	Node 10	Node 11	Node 12	Node 13	Node 14
Phase A	3245V 0.5pu	3130V 0.5pu	3123V 0.5pu	3078V 0.5pu	3060V 0.5pu	3060V 0.5pu	209V 0.9pu	209V 0.9pu	209V 0.9pu	209V 0.9pu
Phase B	3245V 0.5pu	3130V 0.5pu	3123V 0.5pu	3078V 0.5pu	3060V 0.5pu	3060V 0.5pu	0V	0V	0V	0V
Phase C	6491V 1.0pu	6259V 1.0pu	6247V 1.0pu	6157V 1.0pu	6121V 1.0pu	6121V 1.0pu	209V 0.9pu	209V 0.9pu	209V 0.9pu	209V 0.9pu

Appendix D

System Base kVA: 100000.00

IPOH HOSPITAL DISTRIBUTION SYSTEM POWER FLOW

Current: Amps

Voltage: KV LL

Power: Watts, vars

Name	1st Node	2nd Node	Phase	Library Ref	Maximum Current	Minimum Voltage	Total Branch Power		Total Distance
							P	Q	
T1	KgJawa132KV	JawaT1	ABC	132T11M30	140	11.383	-2,566,245.07	-1,046,002.08	0.0000
Switch2	JawaT1	JawaT2	ABC	BREAKER	74	11.383	-1,358,077.03	-540,699.89	0.0000
T2	JawaT2	KgJawa132KV	ABC	132T11M30	140	132.000	-2,566,244.41	-1,046,005.64	0.0000
UG	JawaT2	Node6	ABC	A11UG185	217	10.987	3,921,853.90	1,564,876.79	5.0000
Line1	Node6	Node7	ABC	A11UG185	59	10.966	-1,002,308.70	-486,606.50	6.0000
UGCABLE	Node6	Node8	ABC	A11UG185	160	10.812	2,783,673.32	1,156,947.36	8.0000
Cable4Line2	Node8	Node9	ABC	A11UG185	68	10.763	1,239,185.27	245,752.77	10.0000
Switch1	Node9	Node10	ABC	USER	68	10.763	-1,233,816.74	-294,221.01	10.0000
Tran6	Node10	Node11	ABC	11T433M0.5	163	0.433	-120,676.23	-25,274.76	10.0000
Tran4	Node10	Node12	ABC	11T433M0.5	136	0.433	-100,470.35	-21,883.11	10.0000
Tran3	Node10	Node13	ABC	11T433M0.5	543	0.434	-407,469.59	-94,198.40	10.0000
Tran1	Node10	Node14	ABC	11T433M0.7	410	0.434	-302,600.28	-76,432.37	10.0000
Tran2	Node14	Node10	ABC	11T433M0.7	410	10.763	-302,600.28	-76,432.37	10.0000
Cable1	JawaT1	Node2	ABC	A11UG185	67	11.334	1,205,700.48	483,473.45	2.0000
Tran9	Node2	Node16	ABC	11T433M1.5	1,765	0.425	-1,200,536.52	-537,541.70	2.0000

Appendix E

Transformer Status Report

System Base kVA: 100000.00

Voltage: Volts LN

Name	Tapped Node	Reg Node	Type	Tap (A)	Tap (B)	Tap (C)	At Regulated Node		
							Va	Vb	Vc
T1	KgJawa132KV	JawaT1	Y-D +30	0.96250	0.96250	0.96250	6,571.819	6,571.819	6,571.819
T2	KgJawa132KV	JawaT2	Y-D +30	0.96250	0.96250	0.96250	6,571.819	6,571.819	6,571.819
Tran5	Node10	Node11	D-Y +30	0.93125	0.93125	0.93125	249.868	249.868	249.868
Tran4	Node10	Node12	D-Y +30	0.93125	0.93125	0.93125	250.163	250.163	250.163
Tran3	Node10	Node13	D-Y +30	0.91250	0.91250	0.91250	250.595	250.595	250.595
Tran1	Node10	Node14	D-Y +30	0.92500	0.92500	0.92500	250.347	250.347	250.347
Tran2	Node10	Node14	D-Y +30	0.92500	0.92500	0.92500	250.347	250.347	250.347
Tran6	Node2	Node16	D-Y +30	0.99375	0.99375	0.99375	245.521	245.521	245.521

Appendix F

Maximum Fault Current

Fault resistance: ohms

System Base KVA: 100000.00

Current: Amps Thevenin Impedance: pu

Node	Base Voltage (kV) LL	Ph	3ph-g	Ph-g	Ph-g Z	Ph-ph	Ph-ph-g (A) (B) (C)	3ph un-gmnd	Thevenin Impedance				X/R Ratio	
									R1	X1	R0	X0	X1/R1	X0/R0
JawaT1	11.00	AB	21,086.52	6,607.12	1,112.54	18,261.49	19,885.66 19,885.66 19,885.66	21,086.52	0.03531	0.25514	2.13688	0.58908	7.22600	0.27567
JawaT2	11.00	AB	21,086.52	6,607.12	1,112.54	18,261.49	19,885.66 19,885.66 19,885.66	21,086.52	0.03531	0.25514	2.13688	0.58908	7.22600	0.27567
KgJawa132KV	132.00	AB	5,100.76	5,673.32	5,045.19	4,417.42	5,458.95 5,458.95 5,458.95	5,100.76	0.01441	0.08453	0.01032	0.05889	5.86733	5.70638
Node10	11.00	AB	2,851.14	3,380.28	959.24	2,469.15	3,812.68 3,812.68 3,812.68	2,851.14	1.57177	0.87978	0.22506	1.31069	0.55974	5.82385
Node11	0.42	AB	11,860.53	0.00	0.00	10,271.72	10,271.52 10,271.52 10,271.52	11,860.53	6.76165	10.19310	-44.29694	0.00000	1.50749	0.00000
Node12	0.42	AB	11,856.98	0.00	0.00	10,268.65	10,268.45 10,268.45 10,268.45	11,856.98	6.75411	10.21982	-181.80163	0.00000	1.51313	31937875.18162
Node13	0.42	AB	12,082.85	0.00	0.00	10,464.26	10,464.05 10,464.05 10,464.05	12,082.85	6.91139	9.86086	-44.49817	0.00000	1.42676	0.00000
Node14	0.42	AB	27,821.39	0.00	0.00	2,4095.06	24,094.03 24,094.03 24,094.03	27,821.39	3.34308	4.01465	65.71832	0.00000	1.20088	0.00000

Maximum Fault Current

Fault resistance: ohms

System Base KVA: 100000.00

Current: Amps Thevenin Impedance: pu

Node	Base Voltage (kV) LL	Ph	3ph-g	Ph-g	Ph-g Z	Ph-ph	Ph-ph-g (A) (B) (C)	3ph un-grmd	Thevenin Impedance				X/R Ratio		
									R1	X1	R0	X0	X1/R1	X0/R0	
Node15	11.00	AB	0.00	0.00	0.00	0.00	0.00 0.00 0.00	0.00	826446.28099	0.00000	826446.28099	0.00000	0.00000	0.00000	0.00000
Node16	0.42	AB	52,579.03	0.00	0.00	45,539.57	45,534.76 45,534.77 45,534.77	52,579.02	0.46508	2.67054	-0.18669	0.00000	5.74212	0.00000	
Node2	11.00	AB	10,250.90	5,110.69	1,155.64	8,877.55	9,651.05 9,651.05 9,651.05	10,250.90	0.35594	0.38939	0.63267	2.09693	1.09398	3.31440	
Node6	11.00	AB	5,294.82	2,136.75	801.29	4,585.45	4,914.14 4,914.14 4,914.14	5,294.82	0.81089	0.56817	5.53345	0.59020	0.70068	0.10666	
Node7	0.42	AB	4,519.24	1,629.50	715.96	3,913.78	4,154.62 4,154.62 4,154.62	4,519.24	680.37234	445.80318	5275.61448	435.84712	0.65523	0.08262	
Node8	11.00	AB	3,513.27	2,416.31	837.64	3,042.58	3,361.91 3,361.91 3,361.91	3,513.27	1.26089	0.75257	3.39427	0.94959	0.59686	0.27976	
Node9	11.00	AB	2,851.14	3,380.28	959.24	2,469.16	3,812.68 3,812.68 3,812.68	2,851.14	1.57177	0.87978	0.22506	1.31069	0.55974	5.82383	

Appendix G

1.0 Symmetrical Components

In a three phase system, the line currents I_a , I_b and I_c can be expressed as the sum of:

- a set of balanced positive phase sequence currents I_{a1} , I_{b1} , I_{c1} .
- a set of balanced negative phase sequence currents I_{a2} , I_{b2} , I_{c2} .
- a set of identical zero phase sequence currents I_{a0} , I_{b0} , I_{c0} .

The positive, negative and zero sequence currents are calculated from the line current using:

$$I_{a1} = (I_a + \beta I_b + \beta^2 I_c) / 3$$

$$I_{a2} = (I_a + \beta^2 I_b + \beta I_c) / 3$$

$$I_{a0} = (I_a + I_b + I_c) / 3$$

The positive, negative and zero sequence currents are combined to give the line currents using:

$$I_a = I_{a1} + I_{a2} + I_{a0}$$

$$I_b = I_{b1} + I_{b2} + I_{b0} = \beta^2 I_{a1} + \beta I_{a2} + I_{a0}$$

$$I_c = I_{c1} + I_{c2} + I_{a0} = \beta I_{a1} + \beta^2 I_{a2} + I_{a0}$$

The neutral current I_n is equal to the total zero sequence current:

$$I_n = I_{a0} + I_{b0} + I_{c0} = 3I_{a0}, I_{a0} \text{ is the earth fault current of the system.}$$

Similarly, phase-to-earth voltages V_{ae} , V_{be} , V_{ce} , the residual voltage V_r is equal to the total zero sequence voltage:

$$V_r = V_{a0} + V_{b0} + V_{c0} = 3V_{a0} = V_{an} + V_{bn} + V_{cn} = 3V_{ne}$$

V_{ne} is the neutral displacement voltage of the system.

$$\beta = -1/2 + j\sqrt{3}/2$$

$$\beta^2 = -1/2 - j\sqrt{3}/2$$

$$j = 1 \angle 90^\circ$$

Similarly,

- for a positive-sequence phase voltage $V_{a1} = E_a - I_{a1}Z_1$, where Z_1 is the positive-sequence impedance and E_a is the induced voltage.
- the negative-sequence voltage at phase a is $V_{a2} = -I_{a2}Z_2$, where Z_2 is the negative-sequence impedance.

- the zero-sequence voltage is $V_{a0} = -I_{a0}Z_0$, where Z_0 is the zero-sequence impedance.

$$V_{a0} + V_{a1} + V_{a2} = E_a - I_{a1}Z_1 - I_{a2}Z_2 - I_{a0}Z_0$$

$$\text{But since } V_a = V_{a0} + V_{a1} + V_{a2} = 0$$

$$\text{and } I_{a1} = \frac{E_a}{Z_1 + Z_2 + Z_0} = \frac{1}{3} I_a$$

$$\text{and } I_a = \frac{3E_a}{Z_1 + Z_2 + Z_0}$$

For a line-to-line fault say (bc) phases,

$$I_{a1} = -I_{a2}$$

$$V_{a1} = V_{a2}$$

$$E_a - I_{a1}Z_1 = -I_{a2}Z_2 = I_{a0}Z_0$$

$$I_{a1} = \frac{E_a}{Z_1 + Z_2}$$

For double line-to-ground fault say (bc) phases,

$$I_{a0} = -\frac{E_a - I_{a1}Z_1}{Z_0} \quad \text{and} \quad I_{a2} = \frac{E_a - I_{a1}Z_1}{Z_2}$$

$$I_a = -\frac{E_a - I_{a1}Z_1}{Z_0} + I_{a1} - \frac{E_a - I_{a1}Z_1}{Z_2} = 0$$

$$I_{a1} = \frac{E_a}{Z_1 + \frac{Z_0 Z_2}{Z_0 + Z_2}}$$

The denominator shows that Z_0 and Z_2 are connected in parallel, and this parallel combination is connected in series with Z_1 .

2.0 Simplified calculation of balanced voltage sags

In the case of balanced voltage sag caused by a symmetrical three-phase fault, the calculation of the sag in different parts of the electrical network can be performed using a single-phase equivalent voltage-divider model. A simple example of such a model is shown in Figure A2.1.

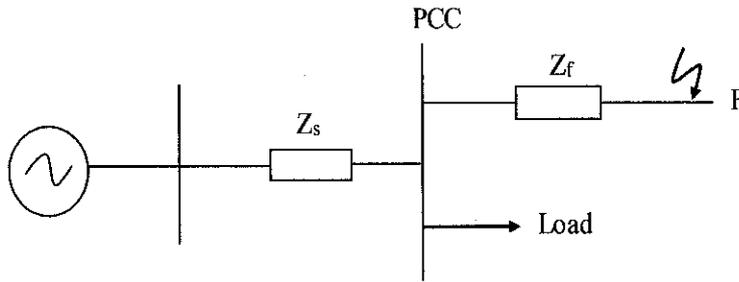


Figure A2.1: Voltage divider general model for calculation of voltage sag

In Figure A2.1, Z_f is the feeder impedance, Z_s is the source impedance and PCC is the point-of-common coupling. Both impedances are complex numbers, the resulting magnitude drop at the point-of-coupling (PCC) during the fault is

$$V_{\text{sag}} = \frac{Z_f}{Z_s + Z_f} \text{ pu}$$

The pre-fault voltage is assumed to be $1 \angle 0^\circ$. The magnitude of sag depends on the distance between the fault and PCC and the fault level at PCC. Fault level is a measure of network robustness. A high fault level is a good indicator of the strength of the system, close proximity to generating stations or a highly interconnected system. A high fault level implies low impedance between source and load and hence is associated with good system voltage profiles and low magnitudes of voltage sags when they occur. It also has a beneficial influence on the speed of operation of protective devices under fault conditions.

Date and Time	03/26/02 08:16:19
Phone Number	
Contact	
Memo	
Problem Description	Tripping/malfunction
Date First noticed	03/25/02
Problem Frequency	Very frequent
How problem exhibits itself	Unknown
Problem Cost	
Location Information	
Name	GH Ipoh 04/23/02 09:11
Power Type	Three phase wye
Feed Phase	Unknown
Phone	
Date and Time	05/10/02 12:26:02
Nominal Voltage	240 Volts
Nominal Frequency	50 Hz

Report Parameters

This report was prepared on 06/27/03 by Engineering Services of Reliable Power Meters.

The following limits were used in analyzing the results.

Maximum Phase Voltage.	254 V
Minimum Phase Voltage.	208 V
Maximum Neutral Voltage.	3 V
Maximum Impulse Voltage.	500 V
Maximum. Waveshape Voltage.	10 V
Maximum Frequency Deviation.	.02 Hz
Minimum Power Factor.	.85
Maximum Voltage T.H.D.	5 %
Maximum Current T.H.D	20 %

Maximum Voltage Imbalance. 2 %

Maximum Current Imbalance. 5 %

Any values outside these limits are noted in the report. Values within the limits are considered to be within a safe operating range. These limits have been programmed by Engineering Services.

Initial Conditions

A summary of all the electrical parameters at this location is presented in the tables and graphs below. Parameters marked with an ‘*’ lie outside the limits defined above.

Initial Power measurements for GH Ipoh:GH Ipoh 04/23/02 09:11 , 05/10/02 at 12:26:02

Measurement	Phase A	Phase B	Phase C	Neutral	Ground
True RMS. Voltage	245.5V	245.1V	244.7V	768.2mV	
Max. Peak to Peak Voltage	691.0V	689.9V	688.0V		
True RMS. Current	797.2A	801.1A	767.1A	25.51A	13.09mA
Max. Peak to Peak Current	2.268kA	2.280kA	2.189kA		
Fundamental RMS. Voltage	245.4V	245.1V	244.6V		
Voltage Angle	0°	240.2°	120.3°		
Fundamental RMS. Current	797.9A	800.0A	766.1A		
Current Angle	166.0°	44.68°	286.9°		
Fundamental Impedance	307.6m Ohms	306.3m Ohms	319.3m Ohms		
Impedance Angle	193.9°	195.5°	193.3°		
Voltage Imbalance	0.16%				
Current Imbalance	2.77%				
Total Voltage Harmonics	2.083%	1.938%	1.884%	602.0%	
Total Current Harmonics	4.007%	3.796%	3.388%	348.9%	882.4%
True VA	N/A	N/A	N/A	N/A	
True VARS.	N/A	N/A	N/A	N/A	
True Watts	N/A	N/A	N/A	N/A	
Distortion	N/A	N/A	N/A	N/A	
True Power Factor	N/A*	N/A*	N/A*	N/A	
Fundamental VA	N/A	N/A	N/A	N/A	
Fundamental VARS.	N/A	N/A	N/A	N/A	
Fundamental Watts	N/A	N/A	N/A	N/A	
Fundamental Power Factor	N/A	N/A	N/A	N/A	

The first 16 harmonics for Phase A voltage are shown below:

Harmonic	Amplitude	Phase	Percent
0	274.6mV	180°	0.079%
1	347.1V	352.8°	100%
2	152.5mV	357.1°	0.044%
3	1.285V	354.0°	0.370%
4	91.55mV	268.5°	0.026%
5	6.409V	146.2°	1.846%
6	0V	359.0°	0%
7	2.835V	13.51°	0.816%
8	110.0mV	212.9°	0.031%
9	976.6mV	179.3°	0.281%
10	0V	359.4°	0%
11	328.7mV	337.6°	0.094%
12	0V	359.5°	0%
13	172.7mV	314.5°	0.049%
14	0V	359.5°	0%
15	345.7mV	134.6°	0.099%
16	0V	359.6°	0%
Odd Harmonics	2.081%		
Even Harmonics	0.086%		
Total Harmonics	2.083%		

The first 16 harmonics for Phase B voltage are shown below:

Harmonic	Amplitude	Phase	Percent
0	244.1mV	180°	0.070%
1	346.6V	233.1°	100%
2	152.5mV	177.1°	0.044%
3	697.2mV	334.8°	0.201%
4	185.6mV	79.10°	0.053%
5	5.951V	268.8°	1.716%
6	30.51mV	179.0°	0.008%
7	2.867V	241.2°	0.827%
8	122.0mV	359.2°	0.035%

9	818.9mV	152.7°	0.236%
10	110.0mV	235.7°	0.031%
11	330.1mV	123.1°	0.095%
12	0V	359.5°	0%
13	129.5mV	224.5°	0.037%
14	0V	359.5°	0%
15	345.7mV	134.6°	0.099%
16	0V	359.6°	0%
Odd Harmonics	1.936%		
Even Harmonics	0.092%		
Total Harmonics	1.938%		

The first 16 harmonics for Phase C voltage are shown below:

Harmonic	Amplitude	Phase	Percent
0	122.0mV	0°	0.035%
1	346.0V	113.1°	100%
2	61.03mV	87.13°	0.017%
3	396.7mV	335.4°	0.114%
4	195.4mV	307.2°	0.056%
5	5.951V	21.47°	1.719%
6	110.0mV	212.7°	0.031%
7	2.430V	128.0°	0.702%
8	61.03mV	89.28°	0.017%
9	772.7mV	170.2°	0.223%
10	0V	359.4°	0%
11	409.5mV	242.9°	0.118%
12	0V	359.5°	0%
13	96.56mV	71.12°	0.027%
14	0V	359.5°	0%
15	302.5mV	134.6°	0.087%
16	0V	359.6°	0%
Odd Harmonics	1.881%		
Even Harmonics	0.101%		
Total Harmonics	1.884%		

The first 16 harmonics for the neutral voltage are shown below:

Harmonic	Amplitude	Phase	Percent
0	1.482V	0°	2.846k%
1	52.06mV	145.8°	100%
2	24.87mV	271.5°	47.76%
3	187.3mV	163.3°	359.9%
4	18.78mV	154.6°	36.08%
5	33.36mV	147.8°	64.08%
6	20.54mV	290.8°	39.45%
7	6.877mV	325.4°	13.20%
8	20.98mV	269.2°	40.30%
9	183.2mV	344.8°	351.9%
10	17.27mV	5.767°	33.17%
11	48.63mV	78.16°	93.40%
12	13.48mV	314.5°	25.90%
13	24.87mV	122.0°	47.76%
14	15.72mV	283.6°	30.21%
15	96.36mV	320.2°	185.0%
16	9.726mV	10.95°	18.68%
Odd Harmonics	572.6%		
Even Harmonics	185.6%		
Total Harmonics	602.0%		

Voltage Events

The following summarizes the results of the Power Quality monitoring survey from 04/23/02 09:11:50 through 05/21/02 09:11:50. It is intended to present an overview of the power quality at GH Ipoh:GH Ipoh 04/23/02 09:11. The table below is a listing of the most significant events.

Event Description	No.	Amp.	Duration	Date and Time
Phase A Largest RMS. Event	420	0V	1.074 hr	May 01 2002 08:30:15
Phase A Largest Waveshape Event	260	200.8V	20 ms	Apr 28 2002 08:50:45
Phase A Longest Waveshape Event	360	227.0V	1.42 sec	May 01 2002 01:40:13

Phase A Largest Impulse Event	N/A			
Phase A Longest Impulse Event	N/A			
Phase B Largest RMS. Event	381	0V	1.074 hr	May 01 2002 08:30:15
Phase B Largest Waveshape Event	281	186.6V	20 ms	Apr 29 2002 11:27:46
Phase B Longest Waveshape Event	521	232.9V	1.04 sec	May 03 2002 17:46:34
Phase B Largest Impulse Event	N/A			
Phase B Longest Impulse Event	N/A			
Phase C Largest RMS. Event	482	0V	1.074 hr	May 01 2002 08:30:15
Phase C Largest Waveshape Event	312	125.0V	100 ms	May 01 2002 01:36:56
Phase C Longest Waveshape Event	742	232.8V	1.04 sec	May 03 2002 17:46:34
Phase C Largest Impulse Event	N/A			
Phase C Longest Impulse Event	N/A			
Neutral Largest RMS. Event	3	2.929V	10.735 day	Apr 07 2002 09:11:54
Neutral Largest Waveshape Event	N/A			
Neutral Longest Waveshape Event	N/A			
Neutral Largest Impulse Event	N/A			
Neutral Longest Impulse Event	N/A			

Solutions Table:

The following table provides a general overview of the types of mitigation devices available for specific power quality phenomena. Often times the need for choosing the right mitigation device depends upon existing system parameters. This information in correlation with monitoring data allows for the implementation of the most economical and feasible electrical solutions.

Disturbance Type	P1159 Category	Specific Phenomena	Solution
Type I – Transients	Impulsive	Lightning, Electro-static Discharge	Filters Isolation Transformers
	Oscillatory	Line/Load switching, power electronic device operation	Low-impedance Power Conditioners (LIPCs) On-Line UPS
Capacitor switching		Surge Protective Devices (SPDs)	
		Ferroresonance Transformer energization	Line Reactor Constant Voltage Transformers (high frequency)
Type II – (0.5 cycles to 2 s)	Instantaneous and Momentary Short Duration Variations	System faults	Constant Voltage Transformers Energy Storage Technologies Magnetic Synthesizers Motor Generator Standby Power Supply Static Transfer Switch Static Voltage Regulator UPS System
Type III – (> 2 s)	Temporary Short Duration Variations (3s to 1 min)	System Protection, Maintenance	Energy Storage Technologies Motor Generator UPS System
	Sustained Interruption Undervoltage Overvoltage	Motor Starting, Load Variations, Load Dropping	Backup Generator Constant Voltage Transformers Energy Storage Technologies Voltage Regulators