SOLID-STATE BASED THERMOELECTRIC DEVICES FOR COOLING AND HEATING

By

FATEN BT HJ MOHD SAID

FINAL REPORT

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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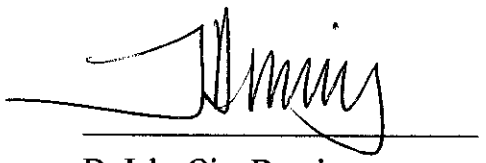
Approved:



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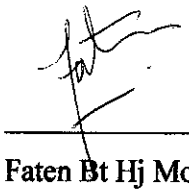
December 2005

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



Faten Bt Hj Mohd Said

ABSTRACT

The project is basically to build an appropriate circuit for solid state thermoelectric cooler or heater. The circuitry is used to control the connection in cold mode and hot mode. The peltier device is fabricated by combining the standard n- and p- channel semiconductor material with a two-element field emission device inserted into each of the two channels to eliminate the solid-state thermal conductivity. In general, two important components building up the thermoelectric cooler or heater is the temperature controller using a microcontroller and peltier device that consists of an n-type and p-type semiconductors of bismuth-telluride ($Bi\ Te_3$) connected by H-bridge circuitry. Both elements must be connected in such a way as to produce a heat sink and heat source that are portable and using small amount of power in the atmosphere of a car. For the microcontroller to work, a specific program is loaded and programmed inside the memory of the PIC 16F877. The objectives of this project are to have theoretical review on thermoelectric devices, search and learn the method of developing the device. The activities are mainly focused on design and simulation. All findings and the detailed analysis including key elements of the project, which is to decide the parameters, and the design procedure that should be used, will be conducted as to follow the overall concept of the project.

ACKNOWLEDGEMENTS

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LIST OF ABBREVIATIONS

$BiTe_3$	- Bismuth – Telluride
Thermoelectric	- Thermoelectric devices are made up of an N and P type semiconductors that are joined together by metal contact to form a junction
Peltier effect	- The semiconductor device for thermoelectric
De	- Difference in energy for thermoelectric
Semiconductor	- solid or liquid material, able to conduct electricity at room temperature more readily than an insulator, but less easily than a metal
Programming language	- High Language use in programming PIC
TEC	- Thermoelectric cooler
CFC	- Chlorofluorocarbon, a usu. gaseous compound of carbon, hydrogen, chlorine, and fluorine, used in refrigerants, aerosol propellants, etc., and thought to harm the ozone layer.

CHAPTER 1
INTRODUCTION

1.1 Background of Study

Solid-state thermoelectric devices are made up of N and P-type semiconductors that are joined together by metal contact to form a junction. They have a dual purpose: electric generation on one side and cooling/heating on the other. Cooling or heating is achieved by applying electric current. Thermoelectric materials have very attractive features such as small size, simplicity and reliability. Further more a thermoelectric micro cooler is a potential candidate for decreasing the operating temperature locally as well as absorbing the heat. The aim of this project is to design and construct a thermoelectric cooling device based on bulk semiconductor materials made form bismuth-telluride that is doped appropriately to make P or N type semiconductor. Such a device contains no moving parts or harmful refrigerants such as CFCs. Without moving parts, thermoelectric coolers are inherently more reliable and require little to no maintenance. The lack of refrigerants carries obvious environmental and safety benefits. This also allows for the manufacture of tiny thermoelectric coolers making them the most suitable choice for today's microelectronics. For this project, the thermoelectric device used is the peltier effect device. The Peltier effect is the driving force behind the thermoelectric cooler or TEC for short. The Peltier effect is caused by the fact that an electric current is accompanied by a heat current in a homogeneous conductor even at constant temperature. Therefore, when an electric current passes through the junction of two dissimilar metals, a cooling or heating effect occurs. The desired direction of heat flow can be controlled by altering the direction of the current flows.

1.2 Problem Statement

Thermoelectric device is a device that can be use as cooler/heater or as an electric generator. The project focused mainly on designing the appropriate circuit in order to implement the use of the thermoelectric device as cooler or heater. The proper method used to implement and designing a cooler or heater is measured in proper steps. The methodology used on designing the proper circuit based on brain storming and having the appropriate review and literature on the thermoelectric device and the temperature sensor. The step continues on searching and learning the appropriate method on designing the suitable circuit. The design stage was constructed after the circuit chosen and the simulation is finalized. In order to satisfy the need of the project, a need of good planning was conducted especially in deciding the devices should be used for obtaining the excess heat and suitable parameters, the designing of the thermoelectric module and focusing every aspect and important elements that should be considered.

1.3 Objectives of the Study

The objectives of this project are:

- To have a theoretical review on the thermoelectric device
- To search and learn the method of developing the thermoelectric circuit
- To design and simulate the proper circuit for the thermoelectric circuit
- To construct a proper circuit for Thermoelectric cooling or heating device

CHAPTER 2
LITERATURE AND THEORY

2.1 Thermoelectric Devices

The proposed thermoelectric device consists of a standard solid-state thermoelectric cooler and two field emission devices (see Figure 2.1). The N-type semiconductor is in thermal contact with the cold source while the P-type semiconductor is in thermal contact with the hot source. In steady state, there is a continuous current with electrons emitted from the N-type semiconductor entering the hot source, while electrons emitted from the P-type semiconductor enter the cold source. The difference in energy, *De*, of the two field emitted electrons is defined as

$$De = (\varepsilon_n) - (\varepsilon_p) \qquad (2.1)$$

where (ε_n) and (ε_p) are the average energies of the field electrons emitted from the N- and P-type semiconductors, respectively. The two breaks in the path do not allow phonon conduction and there is no other thermal flow other than that associated with the electric or field emission current. Thus, the net energy flow from the cold source to the hot source is just *De*. For the typical P–N junction, the energy levels of the conduction band of the N-type semiconductor are generally higher than that of the P-type semiconductor. This implies that *De* is positive. Thus, the field emission from the semiconductor used as a cooling process. It is instructive to describe the energy changes in the transport of the (electron) current through the device. This qualitative analysis is done to distinguish between the electrical potential energy gains or losses due to field acceleration and the ohmic effects, and the thermal energy transported between the cold and hot reservoirs due to the energy exchange processes [1].

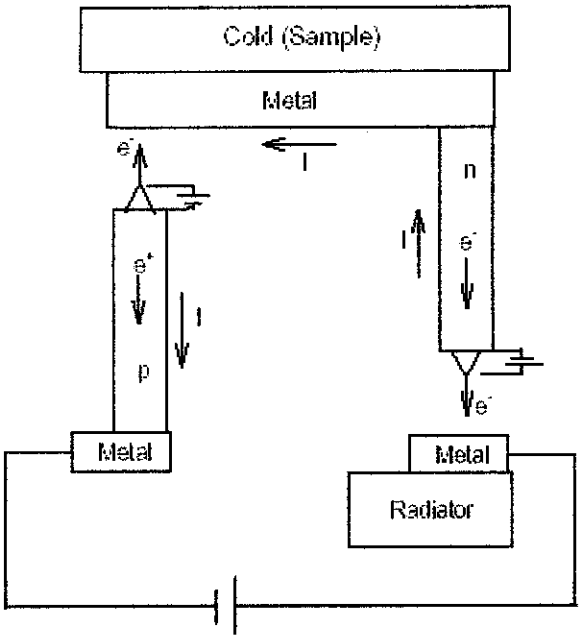


Figure 2.1: Field emission enhanced semiconductor thermoelectric cooler.[1]

The field electrons from the N-type semiconductor have higher energy than those from the P-type semiconductor, which is the principle of cooling in this refrigerator.

2.2 Peltier Effect

In good thermoelectric coolers, the cooling term, which is related to the entropy transport parameter, is on the order of about 50–60 meV per electron at room temperature [2]. By contrast, the cooling device here is shown to have an energy transport (i.e., heat) per electron of 500 meV or so depending on concentration and field. Nevertheless, we use the designation of a thermoelectric cooler because the device proposed uses the electric field to transport energy (i.e., heat) from a cold source to a hot source via N- and P-type carriers. It is instructive to describe the energy changes in the transport of the (electron) current through the device. This qualitative analysis is done to distinguish between the electrical potential energy gains or losses due to field acceleration and the ohmic effects, and the thermal energy transported between the cold and hot reservoirs due to the energy exchange processes.

There has been a resurgence of interest in thermoelectric due to environmental concerns and development in new superconductors, alloy films and complex materials [6]. Most useful thermoelectric cooler materials have a value of *ZT* (dimensionless figure of merit) between 0.01 and 1.3 . Although there is no theoretical limit to the value of *ZT* , the value of *ZT* has not been significantly increased in spite of continuous efforts since the early 1960s . This is due to the fact that all good thermoelectric materials also have relatively good thermal conductivity resulting in backflow of heat from the hot to the cold plate. The presence of these field emission sources in the semiconductor paths constitute thermal breaks without significantly affecting the electric/thermoelectric behavior of the cooler. Thus, this composite thermoelectric device has the property of a good electric conductor with little or no phonon conduction.

A Thermoelectric module is a very small, very light and completely silent solid state device that can operate as a heat pump or as an electrical power generator with no moving parts. When used to generate electricity, the module is called a thermoelectric generator (TEG). When used as a heat pump, the module utilizes the Peltier effect to move heat and is called a thermoelectric cooler (TEC). Peltier effect is the phenomenon used in the thermoelectric refrigeration, with the rate of reversible heat absorption. Figure 2.2 shows the peltier effect in thermoelectric couple. Then current passes through the junction of the two different types of conductors it results in a temperature change [7]. Figure 2.3 shows the combined thermoelectric couples of N-type and P-type semiconductor.

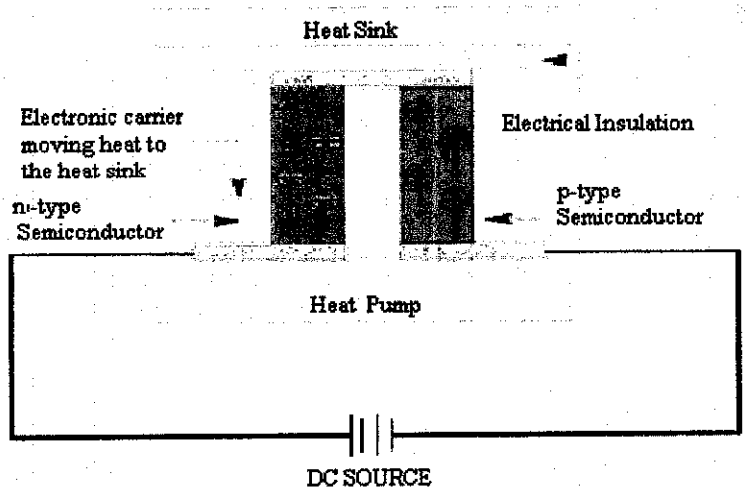


Figure 2.2: Thermoelectric Couple [7].

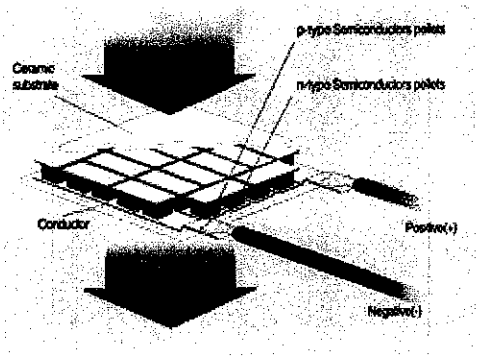


Figure 2.3: Peltier device [7].

The effectiveness of a thermoelectric cooler is given a relative measure called the figure of merit, designated as *ZT*. Taking into account the geometric factors and material properties of the system, the *ZT* has been defined as

$$ZT = \frac{S^2 T}{\rho \kappa} \text{ or } ZT = \frac{S_M^2 T}{R_M K_M} \qquad (2.2)$$

Where S is the Seebeck coefficient, ρ is the electrical resistivity, κ is the thermal conductivity, K_M is the thermal conductance in *watts* / ^oK, R_M is the module's resistance in ohm, S_M is the seebeck coefficient of the module in *volts*/^oK and T is the temperature.

2.3 H-Bridge Circuit

To perform a dual-purpose thermoelectric device for cooling and heating mode, a different position in contacting positive and negative connection must be performed. Based on clockwise and counterclockwise circuitry, the H-bridge connection comes in handy. The circuit uses Darlington power transistors to amplify the current provided to the connection connected to the thermoelectric and also to reduce cost and simplify the circuit. Forward losses are typically 1 to 2 volts, and since the current must pass through two transistors, expect losses to total up to 4 volts at maximum current. The 4 Darlington transistors need to be heatsunk based on the expected current and duty cycle.

2.3.1 Voltage divider

Figure 2.3.1.1 shows the connection of voltage divider to perform lower input voltage. This voltage divider produces an output voltage, Vo, that is proportional to the input voltage, Vs. The output voltage is measured using a voltmeter. The input voltage is the voltage of the voltage source. The constant of proportionality is called the gain of the voltage divider. The value of the gain of the voltage divider is determined by the resistances, R1 and R2, of the two resistors that comprise the voltage divider.

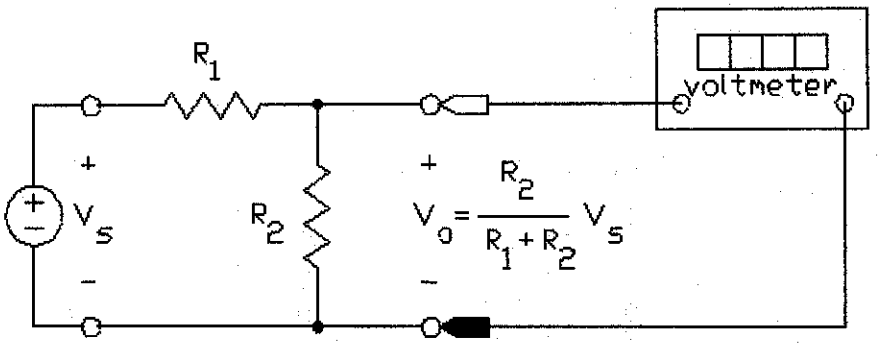


Figure 2.4: Voltage divider

The gain, g, of the voltage divider is given by

$$g = \frac{V_o}{V_s} = \frac{R_2}{R_1 + R_2} \tag{2.3}$$

$$0 \le g \le 1 \tag{2.4}$$

The design equations to gain appropriate resistor on the circuit

$$R_1 = R_2 \frac{1-g}{g} \tag{2.5}$$

$$R_2 = R_1 \frac{g}{1-g} \tag{2.6}$$

2.3.2 Transistor

In order to make the peltier to act as a cooler and a heater, the circuit must be constructed in forward and reverse connection. The H – bridge connection is the most appropriate circuit for this type of condition. It is because the transistor act as a

switch in clockwise connection and counter clockwise connection. Figure 2.5 shows the bipolar junction transistor.

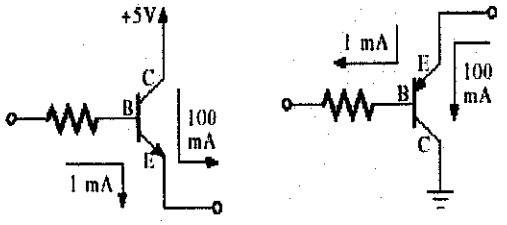


Figure 2.5: BJT transistor

The work of the transistor as a switch will be used to control the thermoelectric device in two-direction circuit. The transistor is a three-layer semiconductor device consisting two N- and one P- or two p- and one n-type layer of material. The former is called an *NPN* transistor, while the latter is called the *PNP* transistor. For the biasing, the terminals have been indicated as emitter, collector and base. To show the calculation, by applying Kirchoff's law we obtain

$$I_E = I_C + I_B \tag{2.7}$$

The important basic relationship for a transistor

$$\left.\begin{aligned} V_{BE} &= 0.7V \\ I_E &= (\beta + 1)I_B \cong I_C \\ I_C &= I_B \end{aligned}\right\} \tag{2.8}$$

Figure 2.6 shows fixed bias circuit on the transistor. When a current is provided to the collector, and to the base, it will act as a switch.

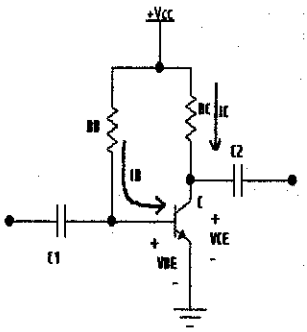


Figure 2.6: fixed bias circuit

Forward bias of base emitter

$$\left.\begin{aligned} V_{CC} - I_B R_B - V_{BE} &= 0 \\ V_{CE} &= V_{CC} - I_C R_C \\ I_B &= (V_{CC} - V_{BE})/R_B \\ V_{CE} &= V_C - V_E \end{aligned}\right\} \qquad (2.9)$$

Collector emitter loop for the use of the transistor

$$\left.\begin{aligned} V_{CE} &= V_C \\ I_C &= \beta I_B \\ V_{BE} &= V_B - V_E \\ V_{CE} + I_C R_C - V_{CC} &= 0 \\ B_{BE} &= V_B \end{aligned}\right\} \qquad (2.10)$$

For the transistor to act as a switch, the transistor will be open and close like a switch. Figure 2.7 shows condition in cut-off or as an open switch.

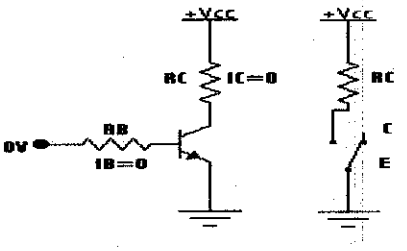


Figure 2.7: Cut-off transistor

The transistor is in the cutoff region when the base-emitter junction is not forward bias. Neglecting leakage current, all the current are zero, and V_{CE} is equal to V_{CC}

Figure 2.8 shows the saturation condition of the transistor. The saturation will make the current flow to the transistor and act as a close switch. When the base-emitter junction is forward bias and there is enough base current, the transistor is saturated.

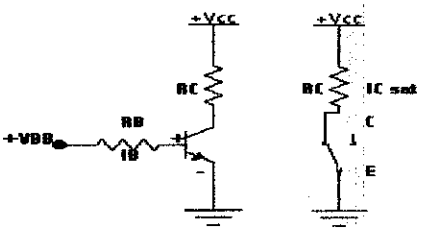


Figure 2.8: Saturation transistor

The formula for collector saturation current is

$$Ic\ sat = (Vcc - Vcesat)\ /Rc \qquad (2.11)$$

Since V_{CE} sat is very small compared to V_{CC}, it can usually be neglected. The minimum value of base current needed to produce saturation is

$$I_B\ min = Ic\ sat\ /\ \beta DC \qquad (2.12)$$

I_B should be significantly greater than I_B min to keep the transistor well in saturation. Figure 2.9 shows the connection on darlington transistor. Darlington transistor amplify the current by amplifying the gain.

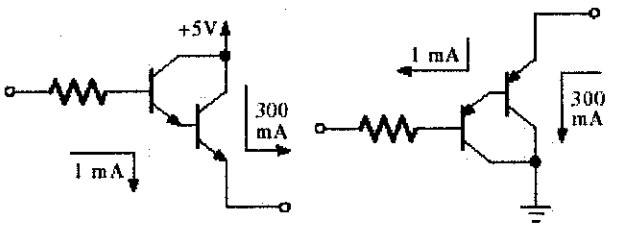


Figure 2.9: Darlington transistor

A single transistor permits the small current from a logic gate (such as an output of a microprocessor) to control a much higher current. A "Darlington pair" (two transistors connected as shown) can deliver an even higher output current.the darlington have gain twice the normal transistor

$$\beta_{total} = \beta_1 \times \beta_2 \qquad (2.13)$$

Table 2.1: Truth Table Of H-Bridge Circuit

Input		output	
A	B	A	B
0	0	float	
1	0	1	0
0	1	0	1
1	1	1	1

Table 2.1 shows the logic use in the thermoelectric circuit. When switch A input is given, the output A will be out. When the switch B input is given, the switch A will

be close and the output B will be produced. The connection of the H-bridge circuit is shown in figure 2.10 by using the logic input.

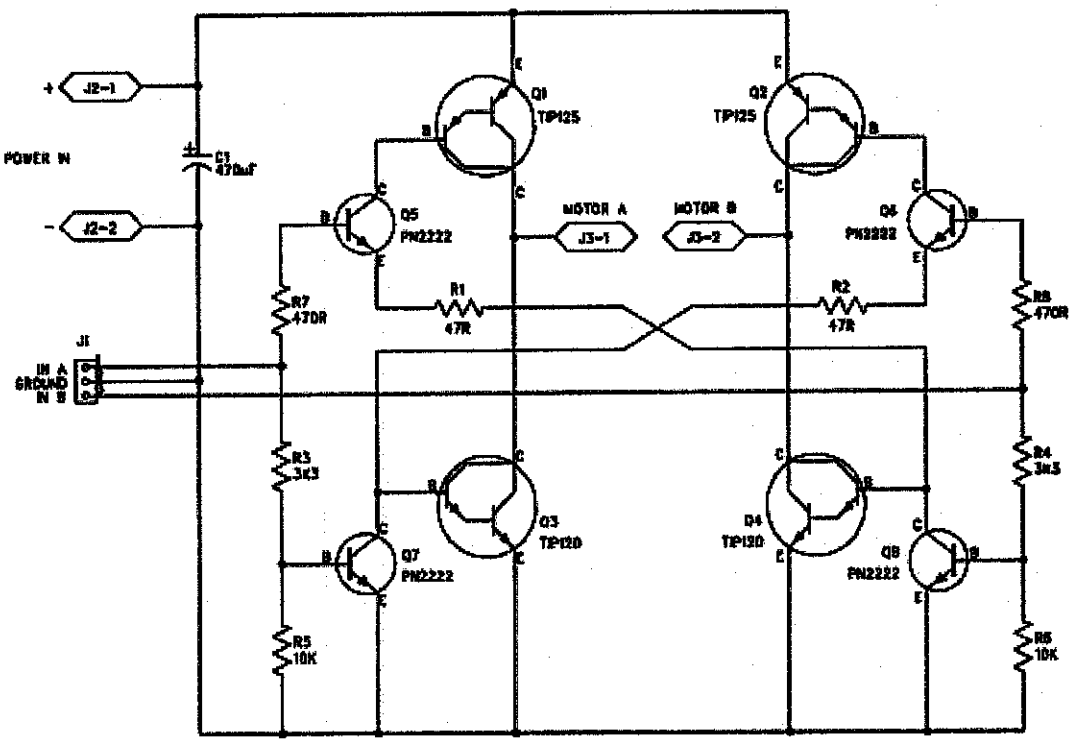


Figure 2.10: H-Bridge Circuit [9]

From figure 2.10, operation with logic signals greater than the peltier supply voltage is allowed and absorbed by R7 and R8. The circuit is really intended to be operated with CMOS logic levels, logic high being about 4 volts.

Transistors Q1,2,3 and 4 must be heatsunk. Insulators should be used, or two separate heatsinks isolated from each other and the rest of the world. Note that Q1 and Q3 are grouped together and share common collectors and can share a heatsink. The same is true for Q2 and Q4.

Operation over 3khz will lead to higher losses. If it is required to run at higher frequency, additional pinch-off resistors can be added to Q1,2,3 and 4, supplementing the internal resistors. A good value would be 1k, and the resistors should be soldered from base to emitter.

To reduce RF emissions, keep the wires between the circuit and the motor short. No freewheel diodes are required, they are internal to the TIP series Darlington transistors.

Drive the circuit from 5-volt logic. Drive levels higher than 5 volts will tend to heat up R1 and 2. This is OK for short periods of time.

Power supply voltage is 5 to 40 volts. Output current up to 5 amps is allowed if the power supply voltage is 18 volts or less. Peak current must be kept below 8 amps at all times [9].

Not shown in the schematic are the internal pinch-off resistors (5K and 150 ohms) and the damper diode that are built into all TIP12x series transistors which can be seen in figure 2.11.

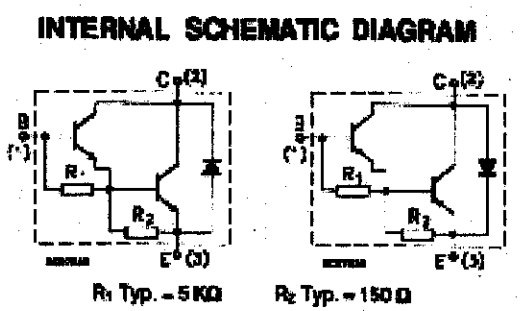


Figure 2.11: Internal Schematic Diagram [9]

2.4 Temperature Control

The temperature sensor is read by A/D converter in PIC 16F877. A/D converter converts the 10 milliVolts per degree Fahrenheit into a corresponding 8-bit binary number. There is an internal voltage divider utilized in this project made up of two 2.2k ohm resistors to produce a V_{ref} equal to ½ the supply voltage for the A/D. Since the temperature sensor outputs 10milliVolts per degree Fahrenheit two degrees will have to pass in order for the binary output to change with a LSB of 20mV. This translates into a temperature accuracy of 2 degree Fahrenheit for the Portable Solid State Temperature Regulated Cooler/Heater.

Figure 2.12 shows the flow diagram of the temperature control process for this project. The signal from LM35DZ sensor will detect the heat, and the voltage signal will be changed to digital using analog to digital converter. The wave will then be sent to the microcontroller, which is programmed to regulate the temperature. The microcontroller will act as the controller of the temperature. When the temperature is decreased or increased above or below the set point, the system will be repeated and

the driver will be on. The system will be rotated with the outside force. The user will choose between cold and hot mode situation. In order to do that, the controller must set two set point for the temperature to be controlled.

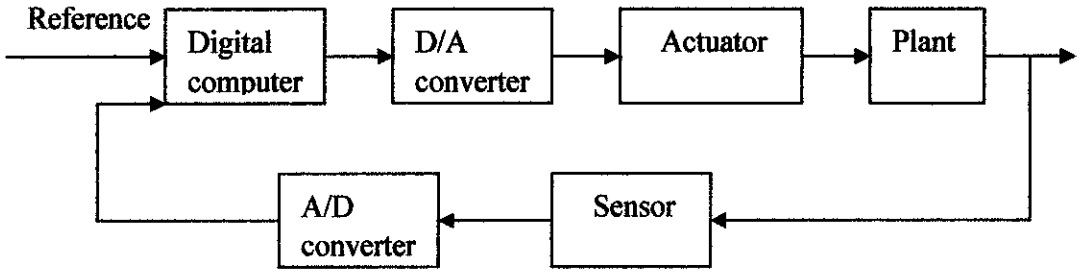


Figure 2.12: Digital Control systems

2.4.2 Temperature Sensor

Figure 2.13 shows the LM35 3 pins sensor. LM35The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±1/4°C at room temperature and ±3/4°C over a full -55 to +150°C temperature range.

Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 μA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a -55° to +150°C temperature range, while the LM35C is rated for a -40° to +110°C range (-10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package [11].

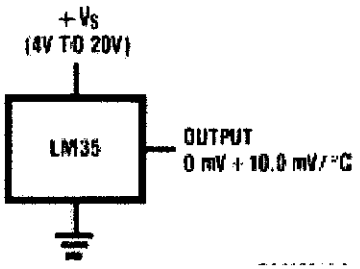


Figure 2.13: LM35 3 pin sensor

2.4.3 Microcontroller

Microcontrollers are usually programmed using the assembly language. The language consists of various mnemonics which describe the instructions. An assembler language is unique to a microcontroller and the assembly language of a certain microcontroller can not be used for any other type of microcontroller. Although the assembly language is very fast, it has some major disadvantages. Perhaps the most important disadvantage is that the assembly language can become very complex and difficult to maintain. It is usually a very time consuming task to develop large projects using the assembly language.

Microcontrollers can be programmed using the CCS compiler. This compiler generates native machine code which can directly be loaded into the memory of the target microcontroller. The CCS compiler is used to compiled the program using C language.

2.4.4 Clock Generator – Oscillator

Oscillator circuit is used for providing a microcontroller with a clock. Clock is needed so that microcontroller could execute a program or program instructions. PIC16F877 can work with four different configurations of an oscillator. Since configurations with crystal oscillator and resistor-capacitor (RC) are the ones that are used most frequently, these are the only ones we will mention here. Microcontroller type with a crystal oscillator has in its designation XT, and a microcontroller with resistor-capacitor pair has a designation RC. This is important because you need to mention the type of oscillator when buying a microcontroller [12].

The XT oscillator is used to control the frequency of the microcontroller PIC 16F877. Crystal oscillator is kept in metal housing with two pins where you have written down the frequency at which crystal oscillates. One ceramic capacitor of 30pF whose other end is connected to the ground needs to be connected with each pin. Oscillator and capacitors can be packed in joint case with three pins. Such element is called ceramic resonator and is represented in charts like the one below. Center pins of the element is the ground, while end pins are connected with OSC1 and OSC2 pins on the microcontroller. When designing a device, the rule is to place an oscillator nearer a microcontroller, so as to avoid any interference on lines on which microcontroller is receiving a clock.[12]

CHAPTER 3
METHODOLOGY / PROJECT WORK

3.1 Project Planning

The project will follow the procedure indicated in the flow chart shown in figure 3.1. The project consists of five major stages. Starting with planning, the brainstorming is conducted on the first stage. On the analysis stage, the suitable device will be chosen and the literature reviews are gathered. The design stage will be implemented to verify the circuit is working properly. If the simulation is not satisfy, the device will be analyze and modified until the final approach can be conducted. The implementation of the project is the final stage of the project.

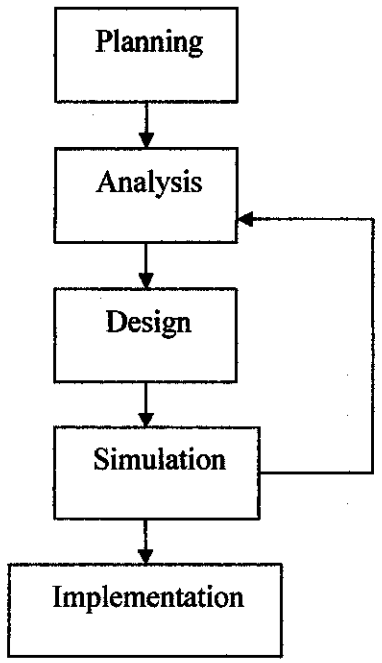


Figure 3.1: Methodology flow diagram

3.2 Planning

A lot of information is gained through this process and it helps a lot in the progress of the design. The literature review have been divided into two types; peltier and temperature controller. By dividing the circuit, the project become easier to understand and much easier to design. The advancement of this project is done by weekly basis as can be seen in the attached Gantt Chart (**APPENDIX A**).

3.3 Analysis

The example of templates from the existing design is studied to come out with the conceptual design of the thermoelectric cooling device. This task is done by numerous researches from the relevant websites and books from the library.

3.4 Design

The design of the H- Bridge circuit are done using p-spice. It is based on rotation controller circuit. The temperature controller is using the PIC 16F877 microcontroller. Figure 3.2 shows the working procedure of the thermoelectric circuit based on the temperature process of the project.

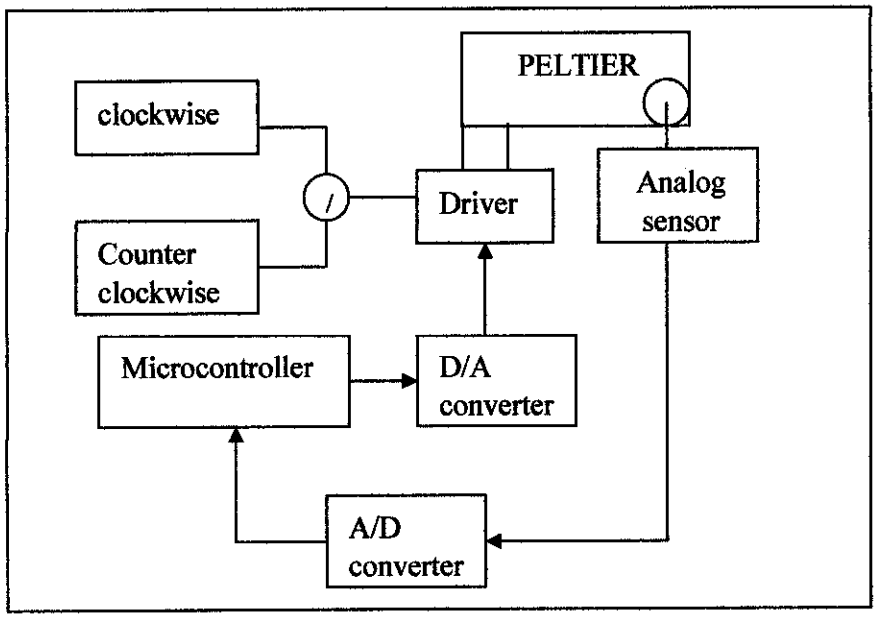


Figure 3.2: The temperature process

The driver of the device is the H- Bridge circuit. The driver will be controlled by the user whether clockwise or counterclockwise position. The driver will make the peltier device to work and send temperature sensor will sense the circuit heat loss and give the voltage flow to the microcontroller. Inside the microcontroller, the microcontroller will interpret the analog signal and convert it to the digital device to control it. The microcontroller will change it back to analog device and make sure the driver interrupted by sending signal to be stop automatically when the heater reach the appropriate heat.

3.5 Simulation

3.5.1 H-bridge circuit

The H-bridge circuit is designed and simulate in the P-spice software. The concept of it is the circuit is designed so that it can receive two types of power supply assigned by the user.

For positive voltage, the peltier will act as the cooler as the heat will be sink. The semiconductor will absorb heat and leave the plate cool. For simulation, instead of using the peltier, the student have change it into LED for easier simulation. The first LED will be on and the second LED will be off.

For negative voltage, instead of sinking the heat, the peltier will produce heat. As it produce heat, it will make the plate hot instead of cold. For simulation, the second LED will be on and the first LED will be off.

3.5.2 Temperature control circuit

The temperature control circuit will be using PIC 16F877. The PIC has the built in analog to digital converter. PIC program for the temperature controller can be loaded up on the computer and the program can be written on it. When writing is finished, it is ready to be assembled. This converts what have been written into a series of numbers, which the computer understands and will be able to use to finally 'blow' the PIC. This new program consisting solely of numbers is called the hex code or hex

file- a hex file will have .hex after its name. The 'complicated' PIC language is all a raw program consists of numbers. So, the assembler, a piece of software which comes with the PICSTART or MPLab package-called MPASM (DOS version) or WinASM (Windows version) – translates the words into numbers.

If however it fails to recognize one of the 'words' then it will register an error- things which are definitely wrong. It may register a warning, which is something that is probably wrong. The other thing it may give is a message something which isn't wrong, but shows it has had to think a little bit more than usual when 'translating' that particular line.

Once the program has been assembled into a series of numbers, they get fused into ROM (Read Only Memory) of the PIC when we blow the PIC 16F877 and they stay there until we erase it from the PIC.

3.6 Design

The design stage will be implemented when all the simulation have worked properly. Table 3.1 shows the list of hardware and software used for the implementation of thermoelectric cooler or heater.

Table 3.1: List of Hardware and Software requirements

	Hardware requirements:	**Software requirements**
1.	Printed Circuit Board (PCB)	Electronic Work Bench (EWB)
2.	Microcontroller (PIC16F877)	P-spice
3.	Crystal Oscillator	Multisim
4.	Peltier	CCS Compiler - Microchip PIC C programming software
5.	LM35DZ temperature sensor	WARP-13 – Microchip PIC Programmer
6.	resistors, capacitors, relay, transistors	

CHAPTER 4
RESULTS AND DISCUSSION

4.1 H-Bridge Circuit

The peltier device can perform as cooler or heater when the polarity of the device changed from positive to negative or negative to positive. To perform in such a way, the peltier device is connected using the H-Bridge circuit. The H-bridge circuit used to control the output of the peltier module. This circuit is supplied with the 12V. The H-bridge is set up so that the output voltage can be turned on and off and also to switch directions with the control of two logic bits.

The circuit uses Darlington power transistors to reduce cost. The function can be seen from the logic given shown on table 4.1. When input A is given, the output from the circuit will be shown in output A by indicating the LED red as in hot mode. If the input A is closed and the input B switch is on, the output B will be produced as in cold mode by indicating the green LED.

Table 4.1: H-bridge circuit logic

Input A (switch 1)	Input B (switch2)	Output A (D1)	Output B (D2)
0	0	0	0
0	1	0	1(cold)
1	0	1(hot)	0
1	1	nil	nil

In order to reach the resistor value that could satisfy the H-bridge circuit, the transistor condition in saturation are calculated. The calculation is shown in the load analysis in figure 4.1.

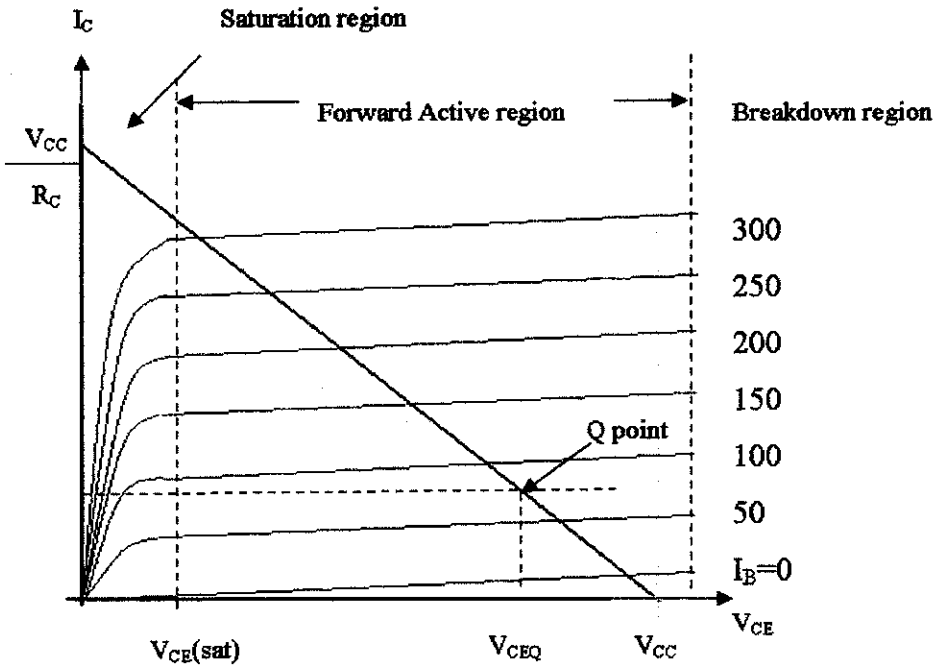


Figure 4.1: load-line analyses

From the graph it shows that at Q point, the I_B min is about $64.13\mu A$. from the Q point the maximum resistor that can be hold in the circuit is lower than 67K. Therefore, the resistor chosen is 10K, 3.3K and 47 ohm. the resistor chosen satisfied the voltage and current need to control the peltier device.

In order to use different voltage in one power supply, a voltage divider circuit is used. By trying an error in order to find the appropriate value for reducing the voltage from 12 V to 5 V.

By using the formula in equation 2.3 the gain that have been calculated is

$$g = \frac{V_o}{V_s} = \frac{5}{12} = 0.41667$$

The gain to reduce the voltage from 12 voltage to 5V is approximately 0.41667. From the equation 2.4, the gain must be less than 1 and must be more than 0 to have to satisfy the suitable gain.

$$0 \leq 0.41667 \leq 1$$

For randomly choosing some value of R_2, the equation had been chosen. In term to show that the value is accurate, the simulation had been done. The nearest value that can be reached the 5V voltage is when R_2 is equal to 100. Using equation 2.5 and 2.6, the value of R_1 is equal to 140. Figure 4.2 shows the construction of the circuit on the connection of voltage divider.

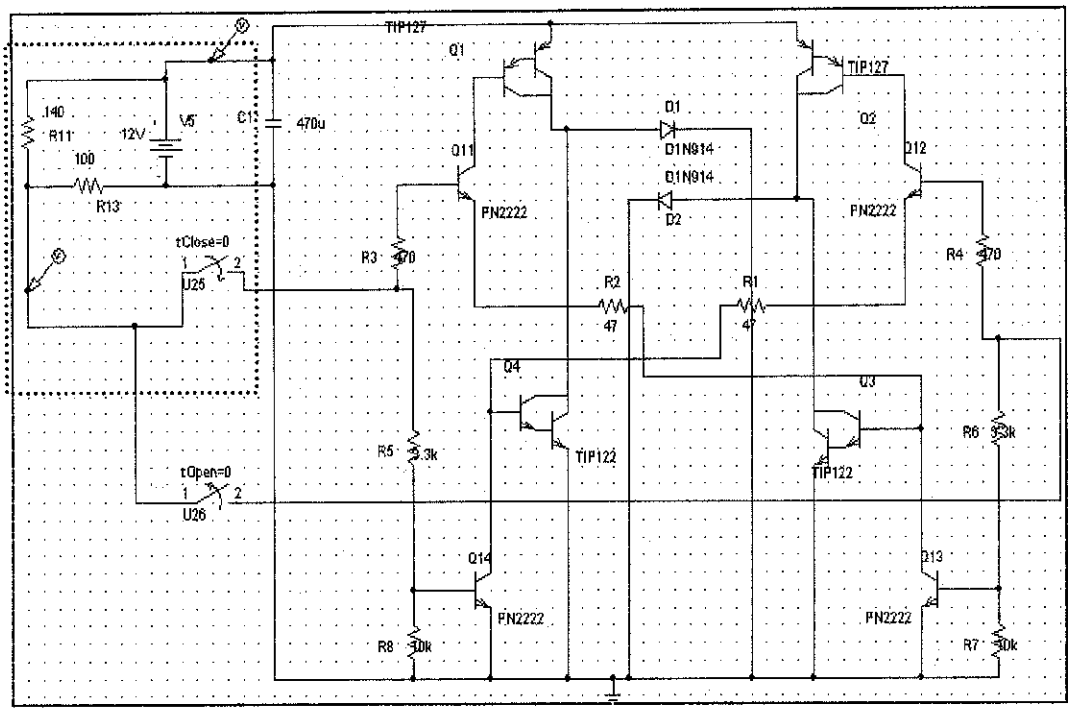


Figure 4.2: H-Bridge schematic

Figure 4.3 shows the simulated voltage divider waveform that satisfied the R_1 and R_2 value. By simulating the circuit from figure 4.2 and measuring the voltage of the output of the circuit, the outcome of the output is nearly to 5V.

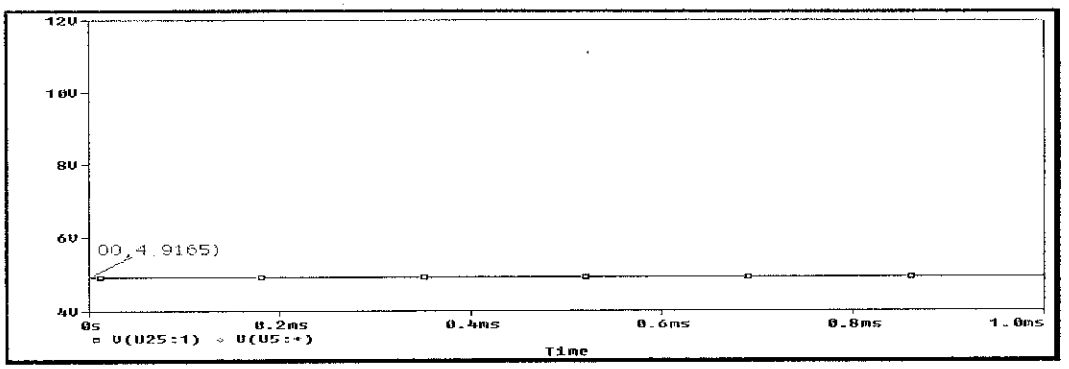


Figure 4.3: waveform for voltage divider

The graph shows voltage versus time for the voltage divider measurement. The purple line indicating the voltage of the output on the circuit connecting to the microcontroller. The V_o is equal to 4.9165 which is very near to 5V. Figure 4.4 shows the experimental measurement on the circuit. The measurement has satisfied the voltage requirements for the circuit.

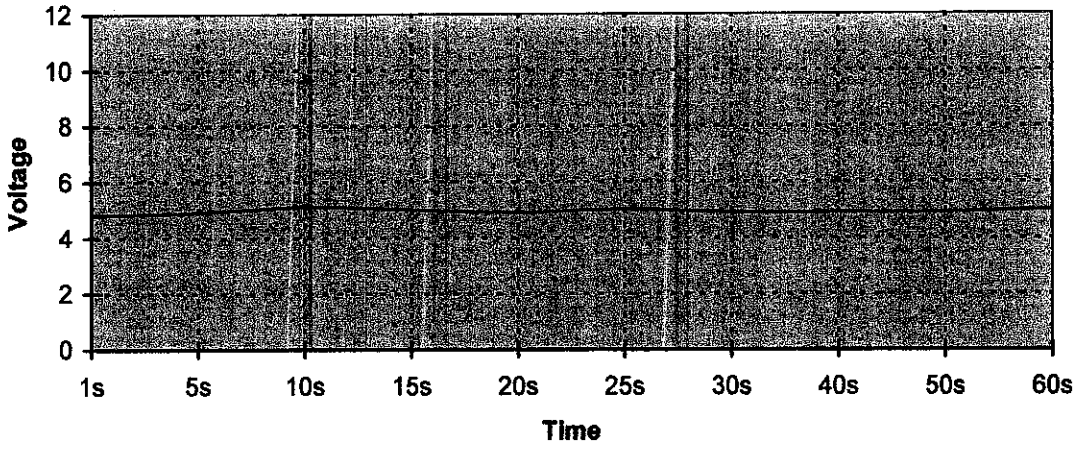


Figure 4.4: Experimental measurement on voltage divider

As the resistor have satisfied the need of reducing the voltage, the resistors chosen are R_1 is equal to 140 Ω and R_2 is equal to 100 Ω. The V_{out} at the changing direction will be approximately 5V to the microcontroller. The voltage in the base transistor will be 5 voltage also as the base transistor will need low voltage and current to satisfy the need on cut-off and the saturation time.

4.1.2 Transistor PN2222

Figure 4.5 shows the Transistor PN 2222 used in the circuit connection and how it is connected to the circuit. The red dotted line box indicating the PN2222 connection. The PN2222 is used in this circuit in order to make the circuit more reliable in amplifying the current through the Darlington transistor. The amplified currents are used to make the peltier working accordingly as it need more current. From the circuit simulation, the power from the PN2222 transistor is measured

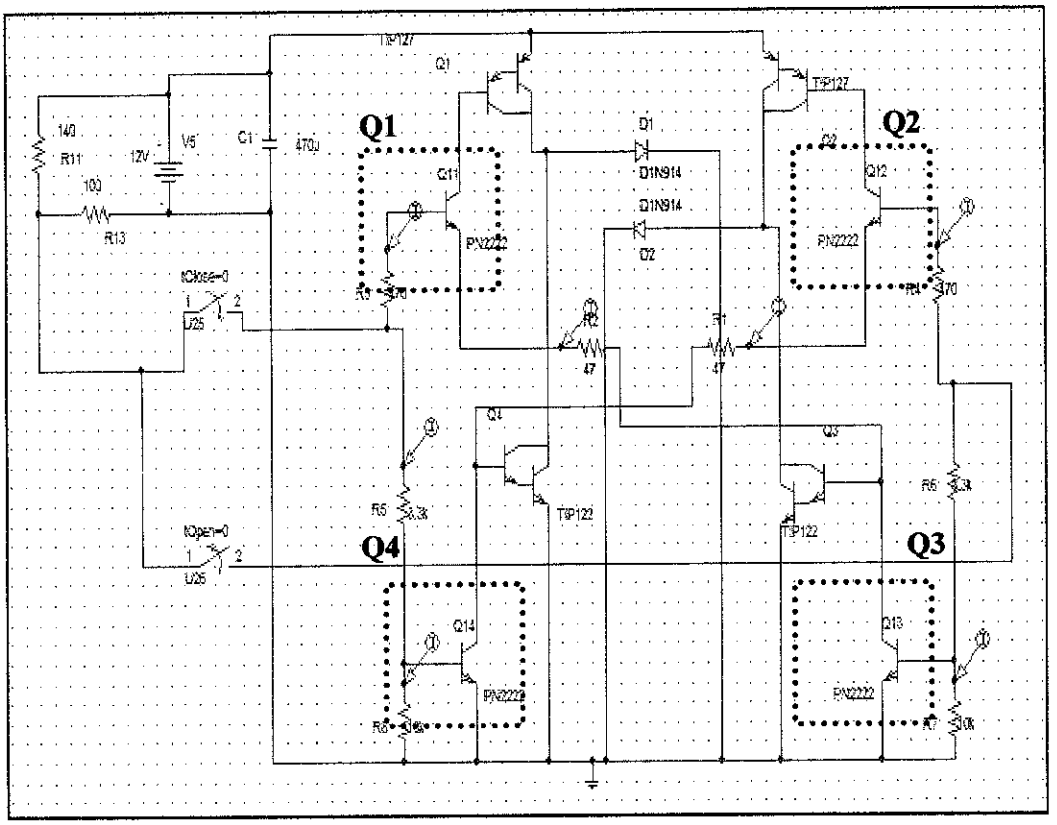


Figure 4.5: H- bridge schematic on PN 2222

In order to satisfy the value is PN2222 that will not exceed the maximum rating, the value is measured. The maximum rating for the PN 2222 is :-

- Collector-Base Voltage 60 V
- Collector-Emitter Voltage 30 V
- Emitter-Base Voltage 5 V
- Collector Current 600 mA
- Junction Temperature 150 °C
- Storage Temperature -55 ~ 150 °C

The construction of the circuit is simulated in the p-spice program and producing the waveform shown in figure 4.6. The circuit have been simulated to show the power used in the transistor.

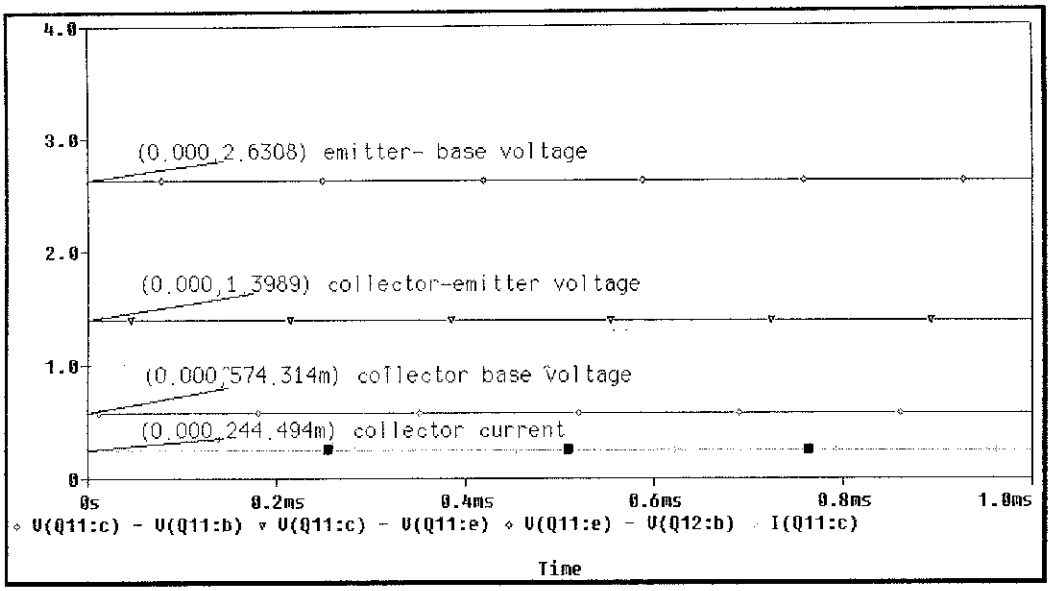


Figure 4.6: Waveform on the power dissipation on transistor PN 2222 of Q1

The waveform shown in figure 4.6 is the transistor in Q1. In counterclockwise connection, the switch 1 is open. The transistor is used to amplified the current through the Darlington transistor. The Collector-Base Voltage in the circuit is 574.314 mV, Collector-Emitter Voltage is 1.3989 V, Emitter-Base Voltage 2.6308 V, Collector Current 244.494 mA .

Figure 4.7 shows the experimental result from the actual circuitry. The value is a bit higher than the experimental results. The graph shows that the value is higher than the experimental results.

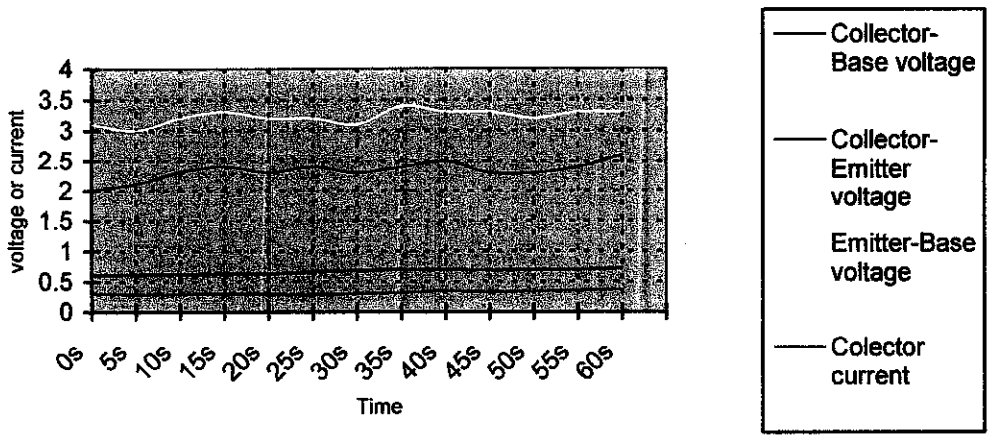


Figure 4.7: Experimental measurement in Transistor Q1 PN 2222

The Collector-Base Voltage in the circuit is 0.62 mV, Collector-Emitter Voltage is 2.3 V, Emitter-Base Voltage 3.01 V, Collector Current 300 mA. It produce such a way because there are some heat produce from the circuit and decapitated in side the transistor making the power goes higher to decapitated.

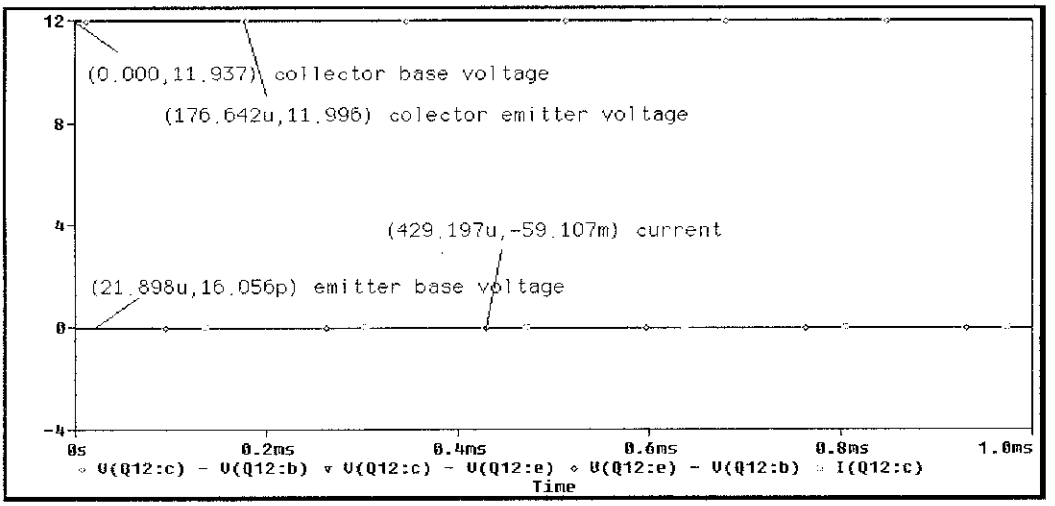


Figure 4.8: Waveform on the power dissipation on transistor PN 2222 of Q2

The waveform shown in figure 4.8 is the transistor in Q2. In counterclockwise connection, the switch 1 is open. The transistor is used to amplify the current through the Darlington transistor. Figure 4.9 shows the actual results on the maximum rate of the circuit.

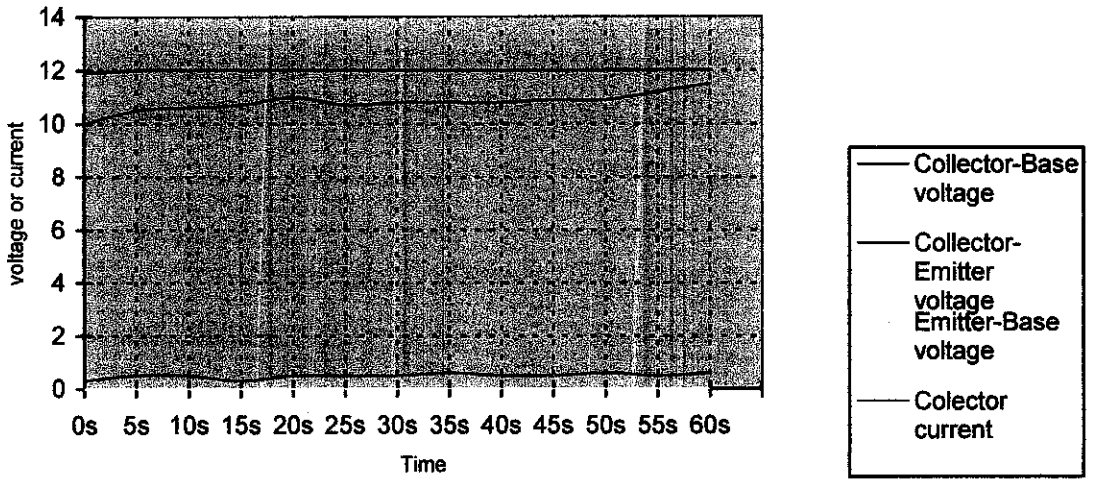


Figure 4.9: Experimental measurement in Transistor Q2 PN 2222

From the experimental result, The Collector-Base Voltage in the circuit is 12 V, Collector-Emitter Voltage is 10.8 V, Emitter-Base Voltage 0 V, Collector Current 0 mA. The collector emitter has one V differences. It is because there are heat produce through the circuit and decapitated the voltage and current.

The waveform shown in figure 4.10 is the transistor in Q3. In counterclockwise connection, the switch 1 is open.

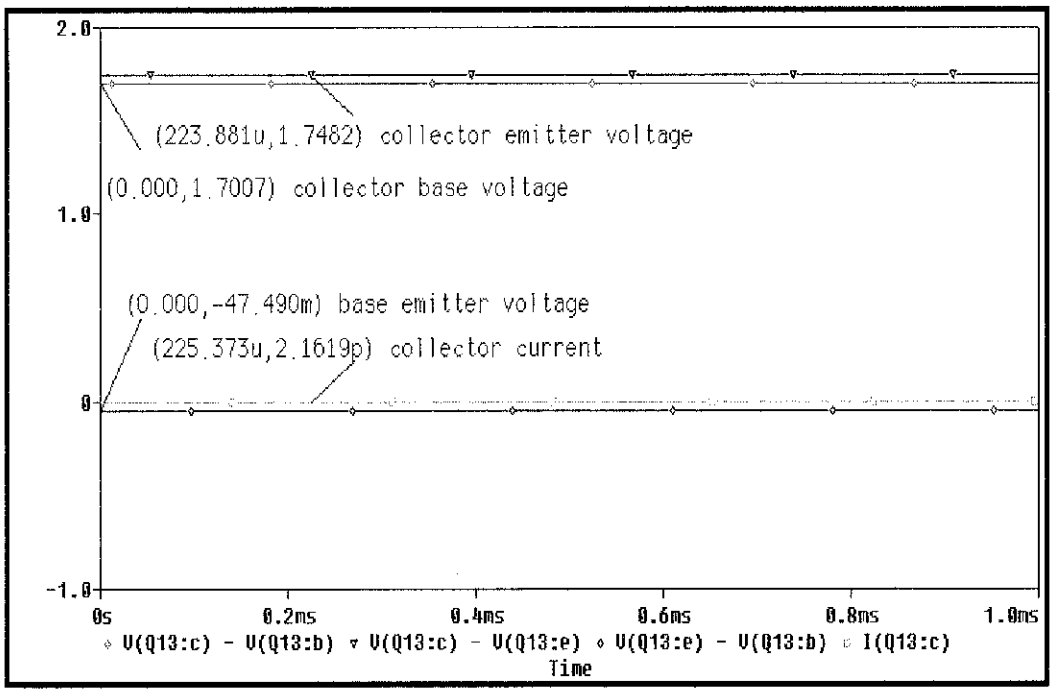


Figure 4.10: Waveform on the power dissipation on transistor PN 2222 of Q3

The transistor is used to amplify the current through the Darlington transistor. The Collector-Base Voltage in the circuit is 1.7007 V, Collector-Emitter Voltage is 1.7482 V, Emitter-Base Voltage 47.490 mV, Collector Current 2.169 ρA. Figure 4.11 shows the experimental connection of Q3 transistor when switch 1 is open. The voltage and the current is low because in counterclockwise connection there no power through the circuit.

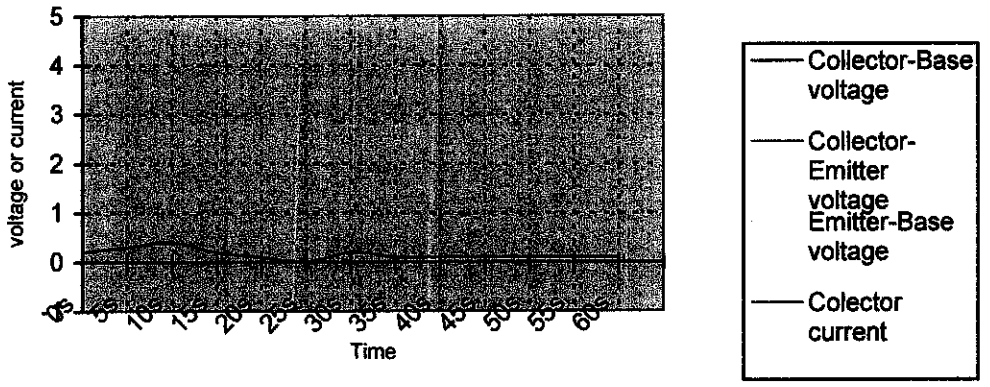


Figure 4.11: Experimental results on transistor Q3 PN 2222

The waveform shown in figure 4.12 is the transistor in Q4. In counterclockwise connection, the switch 1 is open. The transistor is used to amplify the current through the Darlington transistor. The Collector-Base Voltage in the circuit is 704.120 mV, Collector-Emitter Voltage is 4.0559 mV, Emitter-Base Voltage 708.176 mV, Collector Current 499.502 A

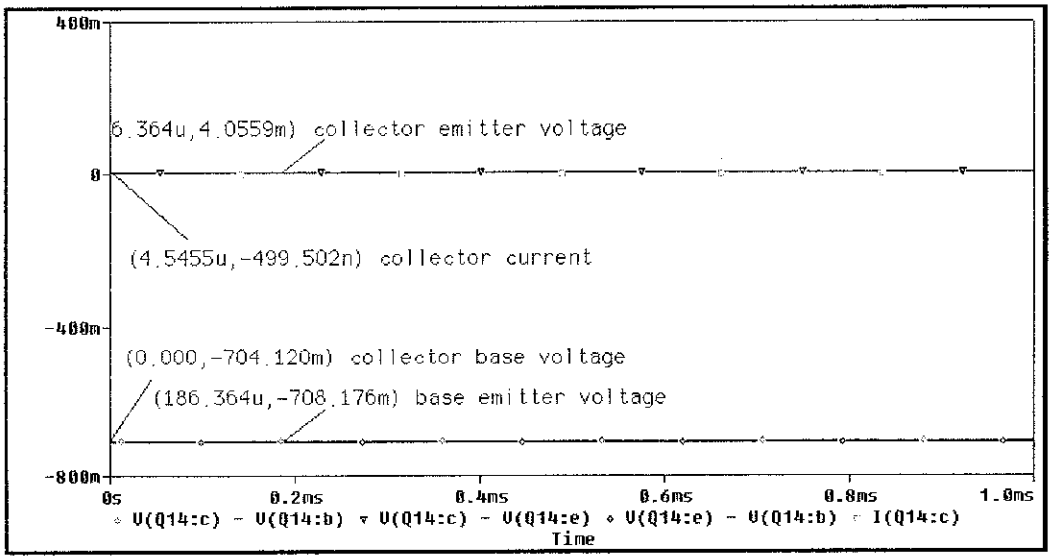


Figure 4.12: Waveform on the power dissipation on transistor PN 2222 of Q4

Figure 4.13 shows the actual connection for the Q4 transistor of PN 2222. From the experimental result, The Collector-Base Voltage in the circuit is 11.9 V, Collector-

Emitter Voltage is 11.028 V, Emitter-Base Voltage 0 V, Collector Current 0 mA. The collector emitter has one V differences. It is because there are heat produce through the circuit and decapitated the voltage and current the same as Q2 connection.

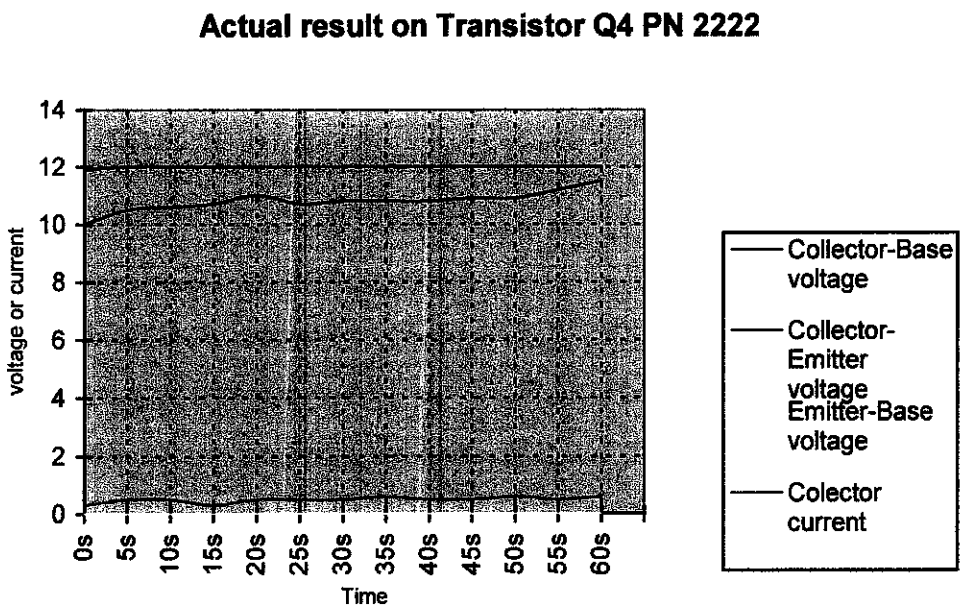


Figure 4.13: Experimental results on transistor Q4 PN 2222

From the data sheet, the maximum rating is justified. Therefore, the PN2222 can be used for this project.

4.1.3 Transistor TIP 120 and TIP 125

Figure 4.14 shows the connection of the darlington transistor. TIP 120 is an NPN transistor and the TIP 125 is a PNP transistor. TIP 125 will be used as the current through the peltier device and lastly through the TIP 120 and to the ground. These transistors used as it is very convenient for power linear and as a good switching device. The switching device is applied for the peltier to act in dual performance as it can be used as a heater or a cooler.

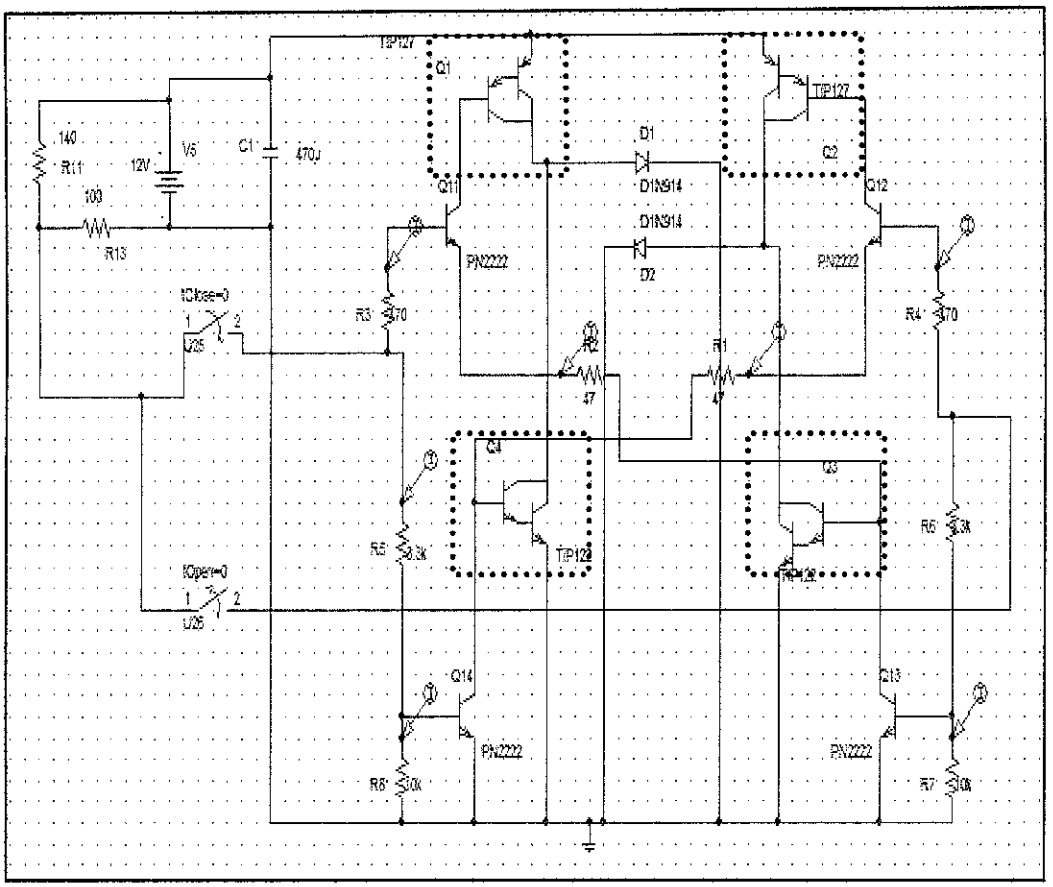


Figure 4.14: H- bridge schematic on TIP 120 and 125

From the circuit simulation, the power from the power transistor is measured. Figure 4.15 shows the power from the circuit. The power is to measure if the transistor can be safely used in the circuit

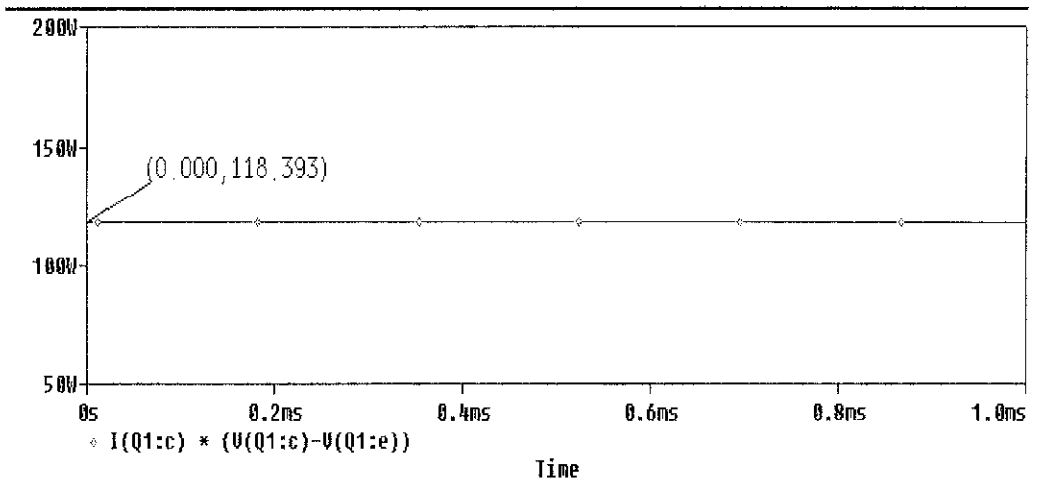


Figure 4.15: Waveforms for power transistor TIP 120 and 125

The power in the transistor is 118.4 watts. The thermal resistor for the transistor TIP 120 and 125 in the ambient temperature is max 62.5 °C/W. The heat sink rating for the transistor.

Thermal power to be dissipated, $P = I_C \times V_{CE} = 118.4$ watts. The maximum operating temperature (Tmax) for the transistor the ambient temperature from the data sheetis 150°C. The maximum ambient (surrounding air) temperature (Tair). If the heat sink is going to be outside the case Tair = 25°C is reasonable, but inside it will be higher (perhaps 40°C) allowing for everything to warm up in operation. By working out the maximum thermal resistance (Rth) for the heat sink using: Rth = (Tmax - Tair) / P that is equal to 1.059°C/W. A heat sink is chosen with a thermal resistance which is less than the value calculated above (lower value means better heat sinking) 1°C/W would be a sensible choice to allow a safety margin. A 1°C/W heat sink dissipating 118.4W will have a temperature difference of $1 \times 118.4 = 118.4$°C so the transistor temperature will rise to 25 + 118.4 = 138.4°C (safely less than the 150°C maximum).

4.1.4 Resistor

The resistor is used to make sure the circuit is safe and have enough resistance. In order to make sure the current and the voltage used is not exceed the limit of the resistor, the resistor is chosen on the limit of the resistor on the circuit for the actual design. Figure 4.16 shows the resistor that is used to connect to the transistor .

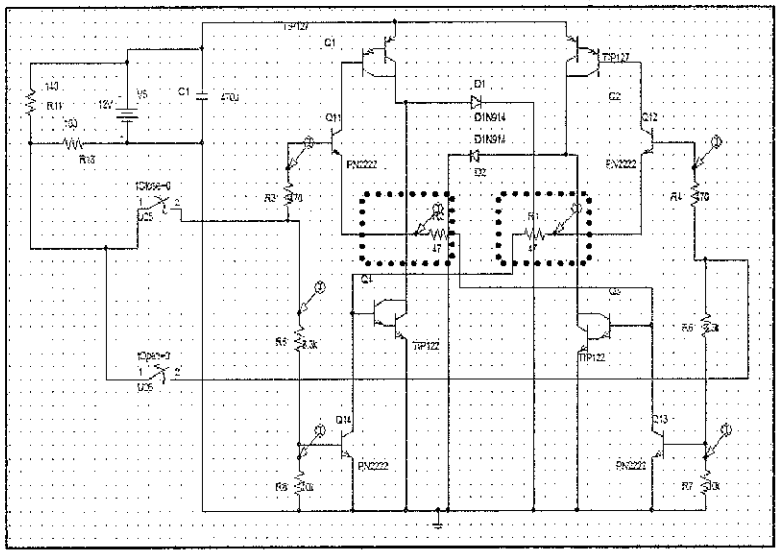


Figure 4.16: H- bridge schematic on R1 and R2

From the simulation, the waveform produce is shown in figure 4.17. The power from the circuit is being produce from R1 and R2.

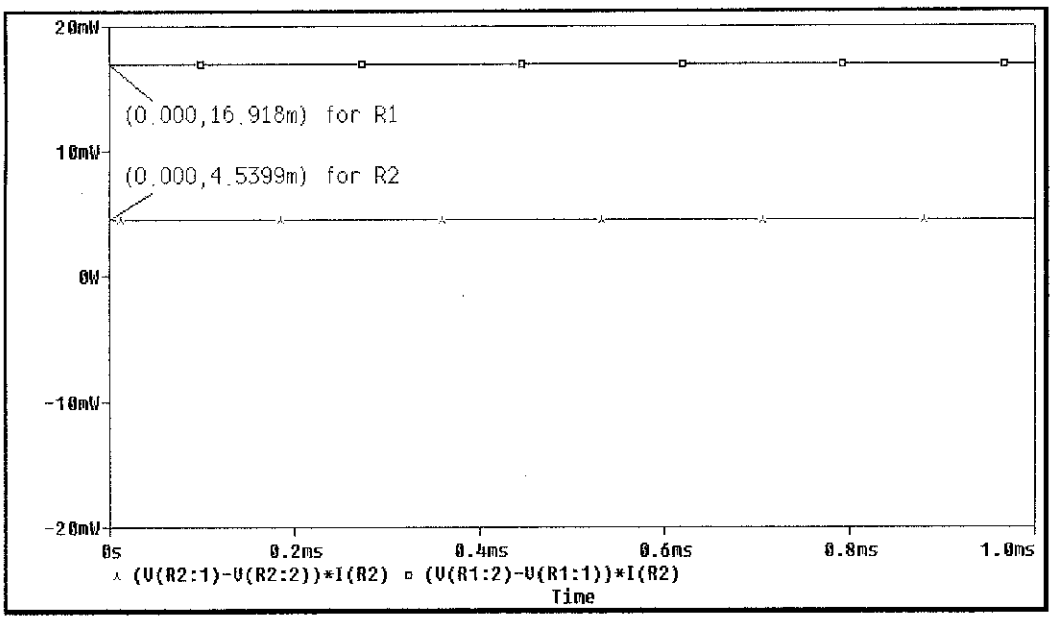


Figure 4.17: Waveforms for R1 and R2

From the simulation, the power R1 and R2 measured when the circuit is in clockwise connection that is when the switch 1 is closed. The power produce from R1 is 16.918 mW and from R2 is 4.5399 mW. The resistor is using low power. The resistor that can be used without exceeding the power limit is resistor ¼ watt because the power is lower than 250 mW in R1 and R2.

Figure 4.18 shows the connection of R3 and R4. The connection is between the switch and the transistor Q1 and Q2

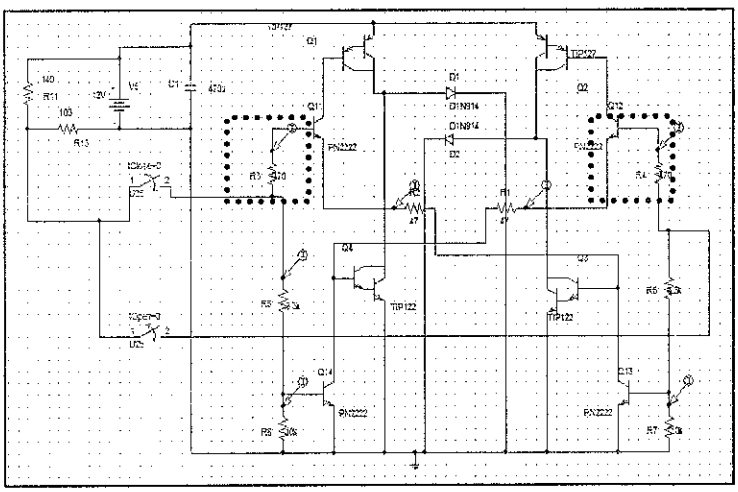


Figure 4.18: H- bridge schematic on R3 and R4

To show the power produce, the simulation is taken. Figure 4.19 shows the waveform of R3 and R4.

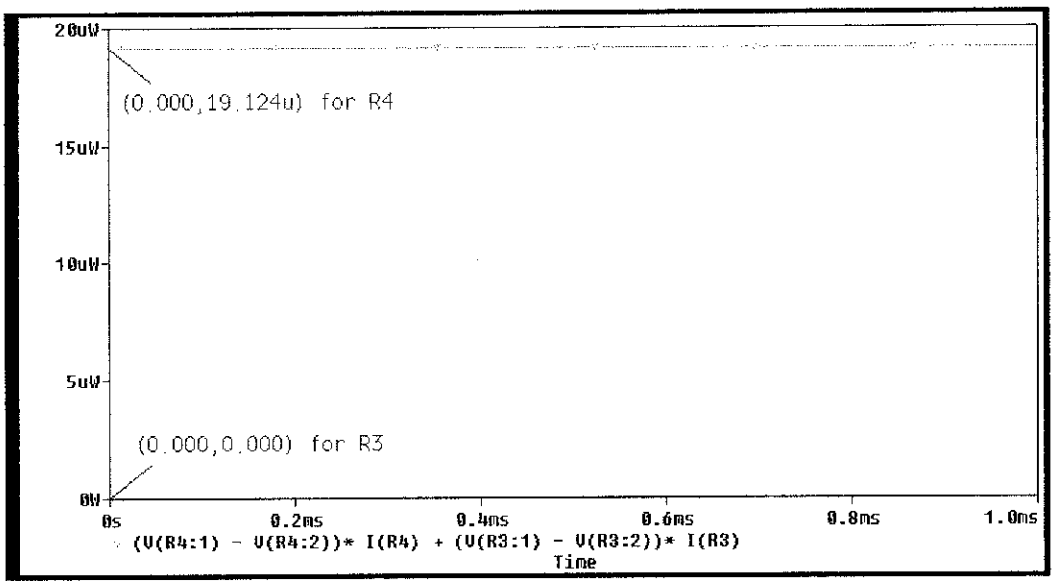


Figure 4.19: Waveforms for R3 and R4

From the simulation, figure 4.19 shows the power R3 and R4 measured when the circuit is in clockwise connection that is when the switch 1 is closed. The power measured from R3 is 0 W and R4 is 19.124 μW. The resistor that can be used without exceeding the power limit is resistor ¼ watts because the power is lower than 250 mW in R3 and R4.

Figure 4.20 shows the connection of R5 and R6 in the circuit. The resistor is connected from switch to the transistor.

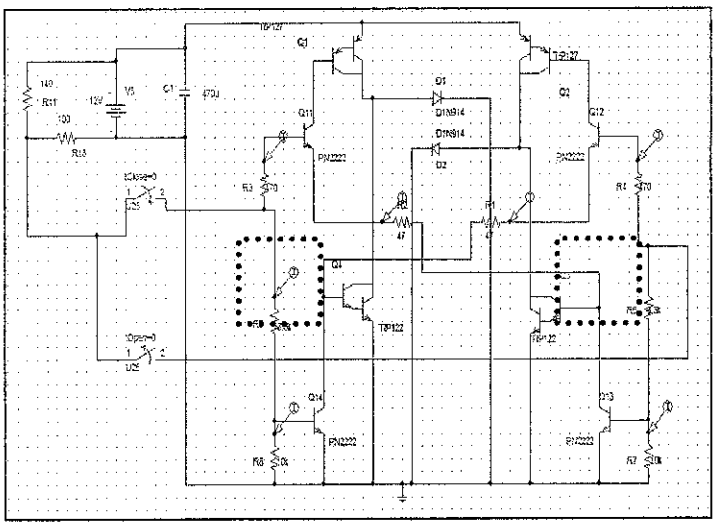


Figure 4.20: H- bridge schematic on R5 and R6

Figure 4.21 shows the simulation result from the measurement of R5 and R6.The waveform indicating the power measured in R5 and R6.

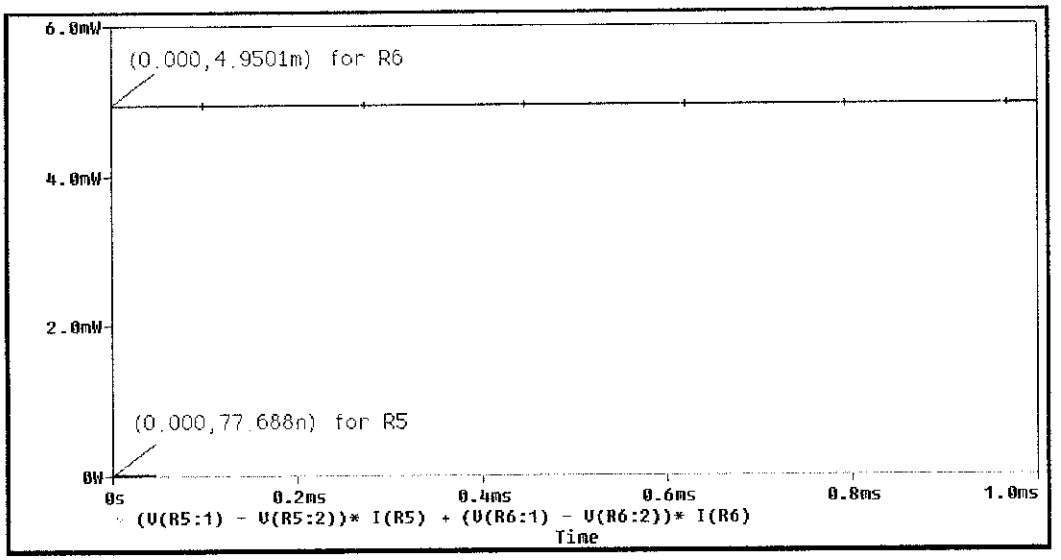


Figure 4.21: Waveforms for R5 and R6

From the simulation, the power R5 and R6 measured when the circuit is in clockwise connection that is when the switch 1 is closed. The power produce in the circuit for R5 is 77.688 ηW and R6 is 4.9501 mW. The resistor that can be used without exceeding the power limit is resistor ¼ watts because the power is lower than 250 mW in R5 and R6.

Figure 4.22 shows the connection of R7 and R8. the connection of the reisitor is between the transistor to the ground. From the circuit simulation, the power is measured from R5 and R6.

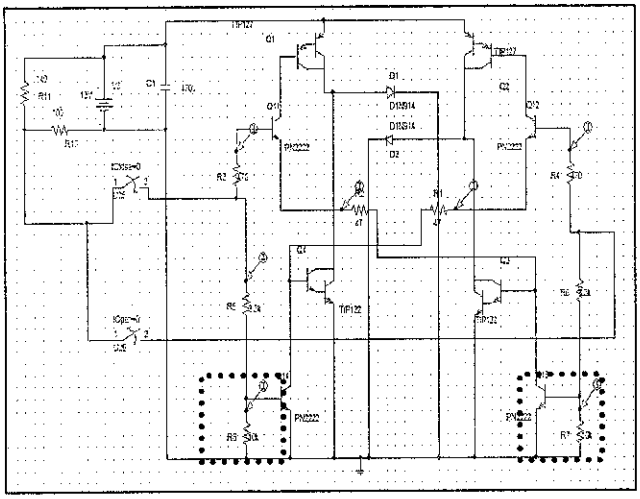


Figure 4.22: H- bridge schematic on R7 and R8

Figure 4.23 shows the simulation result from the measurement of R7 and R8.

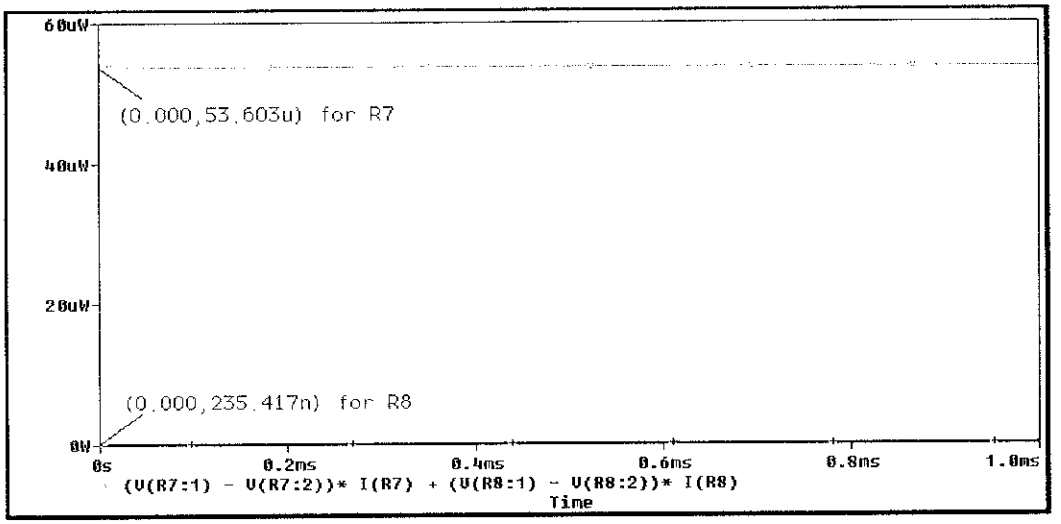


Figure 4.23: Waveforms for R7 and R8

From the simulation, the power R7 and R8 measured when the circuit is in clockwise connection that is when the switch 1 is closed. The power in the circuit for R7 is 53.603 μW and R8 is 235.417 ηW. The resistor that can be used without exceeding the power limit is resistor ¼ watts because the power is lower than 250 mW in R7 and R8.

Figure 4.24 shows the resistor connected in the H-bridge circuitry. The resistor had not exceeded high in power that shows not more than 250 mW in every resistors. It indicates that the circuitry can use ¼ watt resistors.

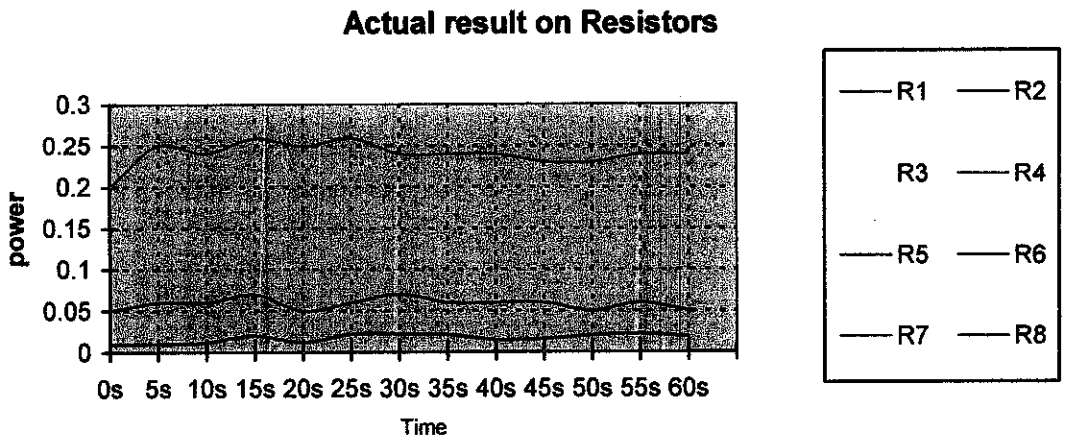


Figure 4.24: Resistors experimental measurements

4.1.5 H-Bridge in clockwise operation

The peltier have two functions. That is to operate as cooler and to operate as heater. When the peltier act as the heater, the H-Bridge circuit will be connected on switch 1, which will indicate the H-bridge will operate in clockwise operation. The connection of the peltier will be shown in diode operation that will be connected to the peltier later on. Figure 4.25 shows the flow of the circuit in clockwise rotation.

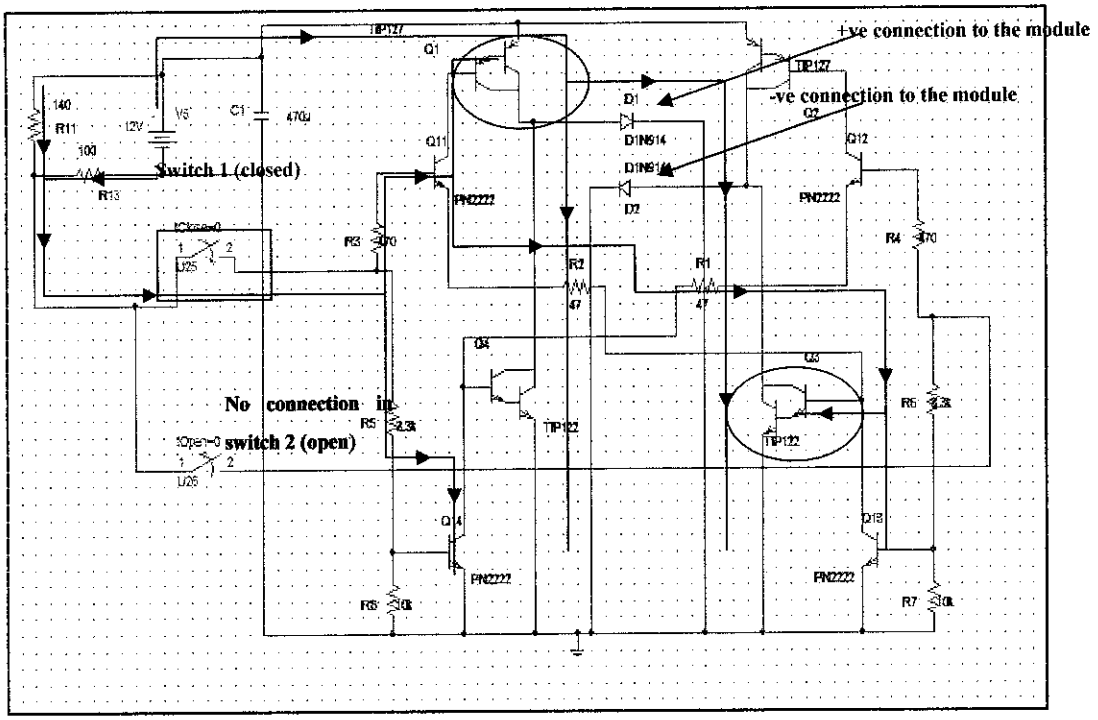


Figure 4.25: Voltage and current flow of h-bridge circuit in clockwise rotation

From figure 4.25, when the switch 1 is on, the +5 voltage of supply from the PIC (will be connected later on) will flow through switch 1. The switch 1 are connected to transistor Q11 PN2222. The PN2222 is the transistor that will act as the current amplifier to amplified the current flow to the transistor darlington TIP 125 that is Q1 from the base in order to switch on the Q1 transistor and to switch on the transistor from Q13 to Q3. The V_{in} will supply the $+12V$ to the Q1 and Q3. The voltage will flow through the base is 7.25V and Q3 for 2.3V supply. The connection is connected such that the peltier module will act as a heater. The red LED will be on to indicate the hot operation.

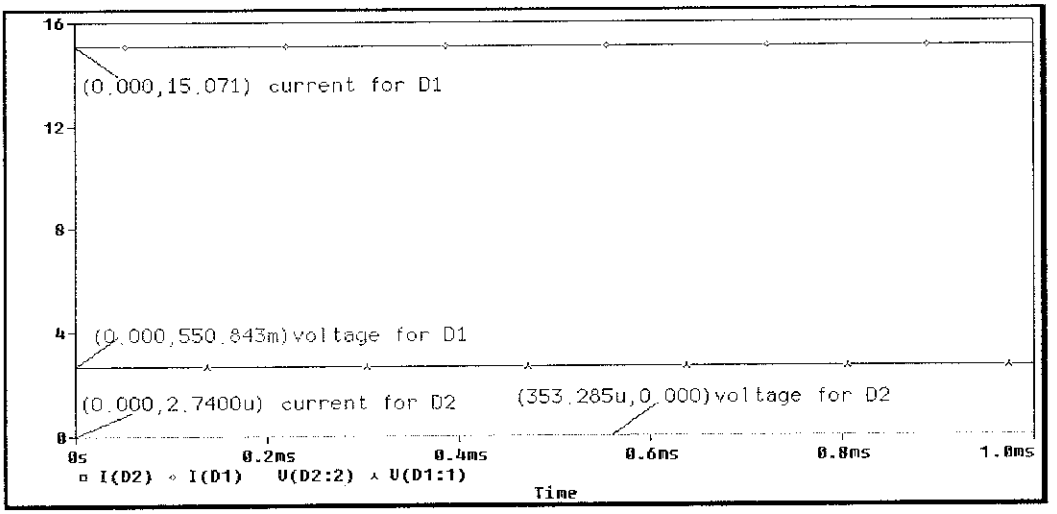


Figure 4.26: Waveform of h-bridge circuit in clockwise rotation

Figure 4.26 shows the simulation on the operation of H-bridge can be seen from the waveform for clockwise rotation indicating the peltier module as a heater. When the switch 1 is on, the D1 will have higher voltage (2.27*V*) than D2 (0.5*V*) to make the peltier flow the voltage from positive to negative side. The voltage from diode 2 is low, to make sure that the peltier module will not be supplied with appropriate voltage from D2 and will flow 1 direction from D1 to D2 and D2 will be connected to the ground. The voltage supplied to the peltier will be 2.27-0.5 = 1.77*V*. The current supplied are higher because of the darlington transistor used. The current is high to make sure that the supplied current can give appropriate power supplied to the peltier module so that the peltier module can function accordingly theoretically. The current flow from D1 is 10.887 A will be supplied through the peltier module to flow in clockwise direction produce hot temperature to the peltier. From D2, there is still a small amount of current flow (1.15μA) but it cannot drive the peltier module in other direction. The current supplied to the load is 10.887*A*-1.15μA = 10.8869*A*. The power produce inside the peltier is $P = 10.887 \times 1.77 = 19.3 Watts$.

4.1.6 H-Bridge in counter-clockwise operation

For the peltier to act as cooler, the connection is connected counterclockwise. The H-Bridge will be used as it can rotate the connection in clockwise mode and otherwise.

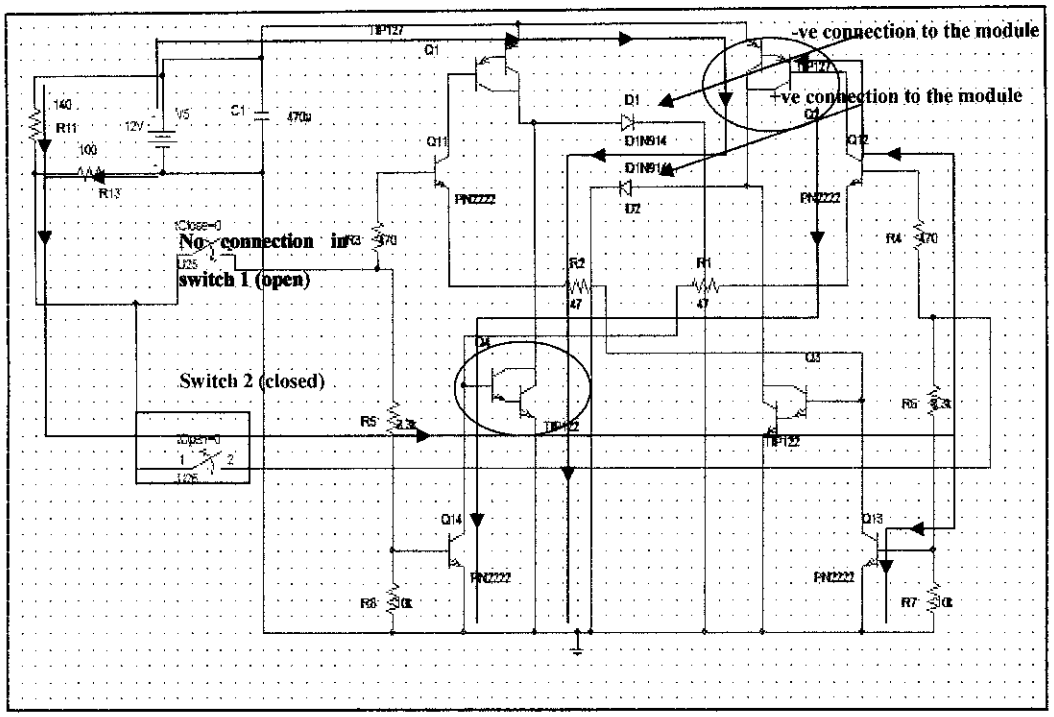


Figure 4.27: Voltage and current flow of h-bridge circuit in counter-clockwise rotation

Figure 4.27 shows the connection of H-bridge in counterclockwise to indicate the cold operation of the peltier module. When the switch 2 is closed, the PIC(not connected yet in this circuit) will supply $+5V$ to the circuit connected to the transistor PN2222 shown as Q12. The transistor will amplified the current to give a sufficient current to the darlington transistor Q2 to switch on. When the transistor is on, the voltage from V_{CC} will flow to Q2 and through the D2. The D2 is the connection to the peltier module and will act as cooler because the peltier will absorb heat instead of releasing the heat. As the voltage and current flow from the D2 is higher, the peltier will be driven as cooler. the green LED will indicate that the peltier are in cold state. As ther is no sufficient current flow through Q11 and Q13, the darlington transistor of Q1 and Q3 will be off.

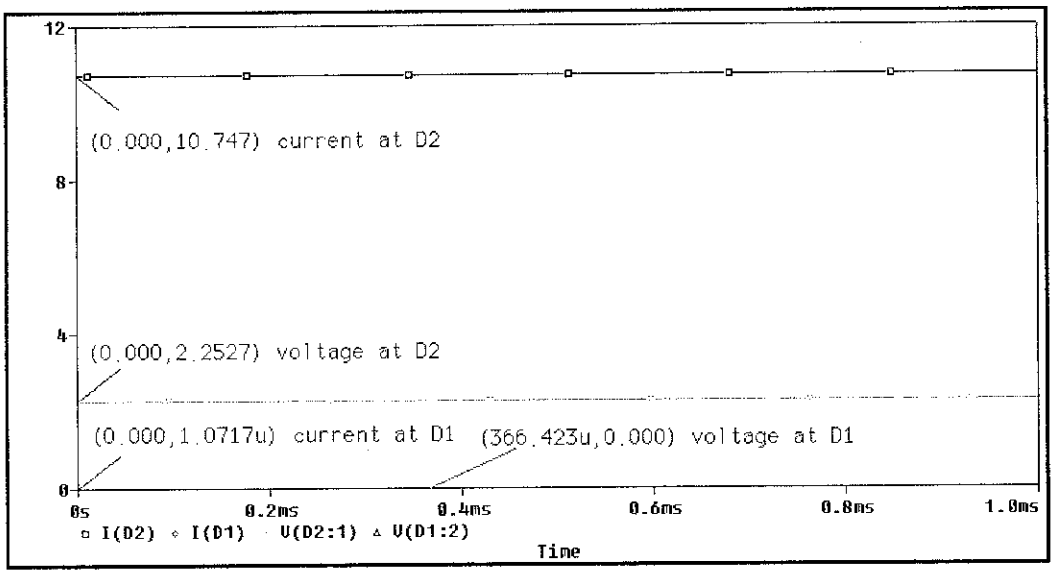


Figure 4.28: Waveform of h-bridge circuit for counterclockwise

The H-bridge circuit shown is in counterclockwise mode to make the peltier be driven as a cooler. When switch 2 is on, the switch 1 will be off. The $+5V$ from the PIC (not connected yet in this circuit) will flow through switch 2 to the Q12 to switch on the Q2. It will allow voltage from the V_{in} to flow through. Figure 4.28 shows the waveform of H-bridge circuit in counterclockwise connection. The voltage flow through D1 is $0V$ that is small amount to give a counter clockwise rotation. From D2 the voltage flow is $2.2527V$ that will driven the peltier different way of flow and act as a cooler. The voltage difference in the peltier is $2.267V$-$0V$ = $2.2527V$. the current flow through D2 is bigger than it flow through D1 to make the same effect as in voltage flow. From D1 is $0\,A$ and from D2 is $10.747A$ current flow to the peltier. The current difference in peltier is $10.747A$ -$0A$ = $10.747A$. When the direction rotate, instead of the peltier pumping the heat, the peltier will sunk heat and releases it at opposite side from the clockwise rotation. The phenomena occurred would make the peltier to act as a cooler. The power produce from the peltier is $P = 2.2527 \times 10.747 = 24.20 Watts$

4.2 Temperature Controller

The temperature controller will consist of temperature sensor, and microcontroller. In order to control the peltier to the desired temperature, the microcontroller used to control it. The temperature sensor will sense the temperature using LM35, the

temperature are sense by sensing the heat that will be send as voltage signal to the microcontroller. When the temperature is still at given range that is between 10°C to 60°C, the PIC will send an appropriate voltage to the H-bridge circuit to drive the peltier in clockwise direction or counterclockwise. Every 1°C 10 mV will be produced inside the temperature sensor. The temperature will increase the voltage output from room temperature 27°C until 60°C in hot mode and from room temperature 27°C until 10°C in cold mode.

4.2.1 Microcontroller

The microcontroller are use to control the temperature to the exact desired temperature for the peltier to be working. The working inside the PIC will be shown in the flow diagram given in figure 4.29.

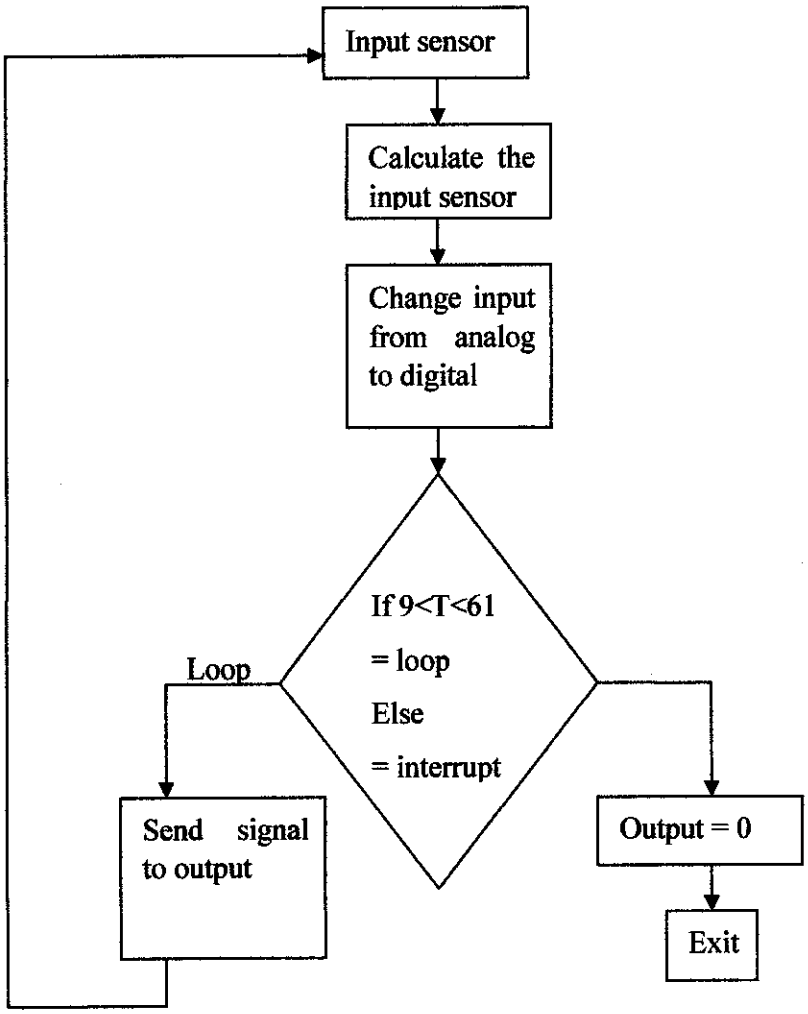


Figure 4.29: Microcontroller flow diagram

PIC 16F877 microcontroller provides two PWM outputs, known as CCP1 (Pin 17) and CCP2(Pin 16). The PWM output CCP1 and CCP2 (Pin 16). The PWM output CCP1 is controlled using timer 2 and register PR2, setup time by division 2, CCP_1_low, setup ADC ports.The period of the PWM outputs CCP1 is set by loading value into register PR2 and then selecting a clock multiplier value of either 1,4,or 16 PWM period is set by PWM period= (PR2 + 1) x 4 x Tosc (clock multiplier) Where T_{osc} is the microcontroller clock period (0.250us with a 4Mhz crystal. In this project the clock multiplier chosen is 4. PWM period = (294 + 1) x 4 x 0.250 x 4 The complete program of controller is defined and the program is shown in appendix E . The PWM mode is enabled and the clock multiplier is set to 4. The PIC will detect the interrupt time as in the voltage from the temperature sensor.

The working of the program starts when the circuit is on. The temperature sensor will sense the heat from the thermoelectric and send the signal to the PIC16F877. The PIC will translate the analog digital and change to digital to control the circuit. When the temperature has been detected, exceeded or lower, the PIC will be interrupted and will be off to restart. Figure 4.30 shows the 8-bit binary input from the sensors. The analog input will be divided to 256 to convert to digital input in 8 bit binary. Every bit will consists of 2.34 mV signal send in. If the signal is more than 100mV and less than 600mV, the H-bridge circuit will be on.

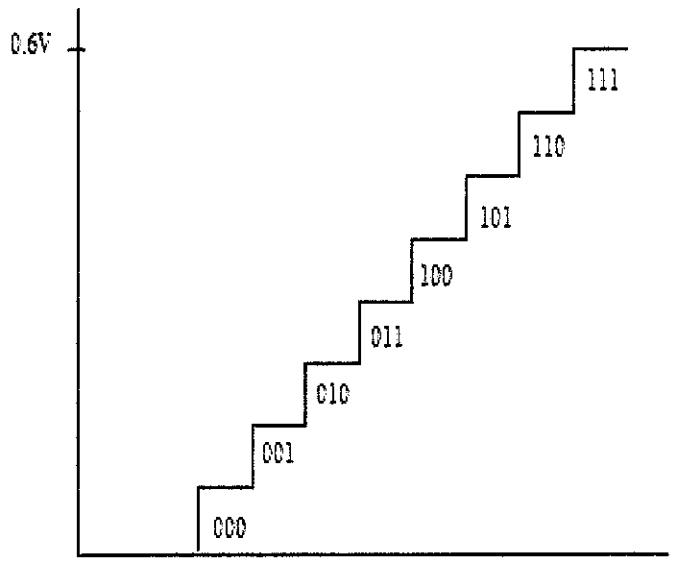


Figure 4.30: 8 bit binary input from the sensor

Figure 4.31 shows the connection of the microcontroller and the temperature sensor. The digital input from the microcontroller will be send to the H-bridge circuit to switch on the circuit. As the voltage and current from the microcontroller is low, in order to amplify the output power from the microcontroller, a darlington transistor is used by applying 5 V from the circuit. The coding of the microcontroller is shown in appendix F

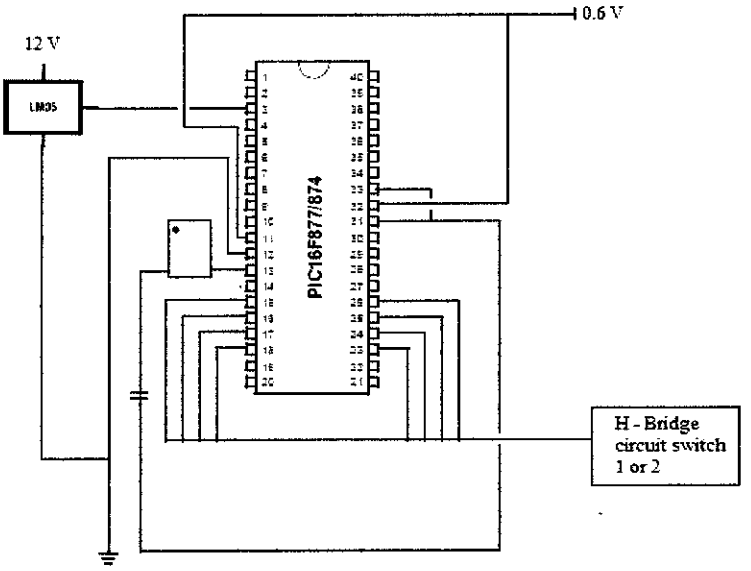


Figure 4.31: Microcontroller temperature sensor circuitry

4.3 Thermoelectric Devices for Cooling and Heating circuitry

Figure 4.32 shows the final circuitry for the thermoelectric device. The connection between the h-bridge circuit and the microcontroller is combined and the design is implemented.Te set up are set . A DC power supply has to be used to move heat in one direction or the other about 12 volts DC that is an ideal supply for the Cooler/Heater. The implementation can be use inside a car connected to the 12V voltage plug for the cooler/heater purpose.

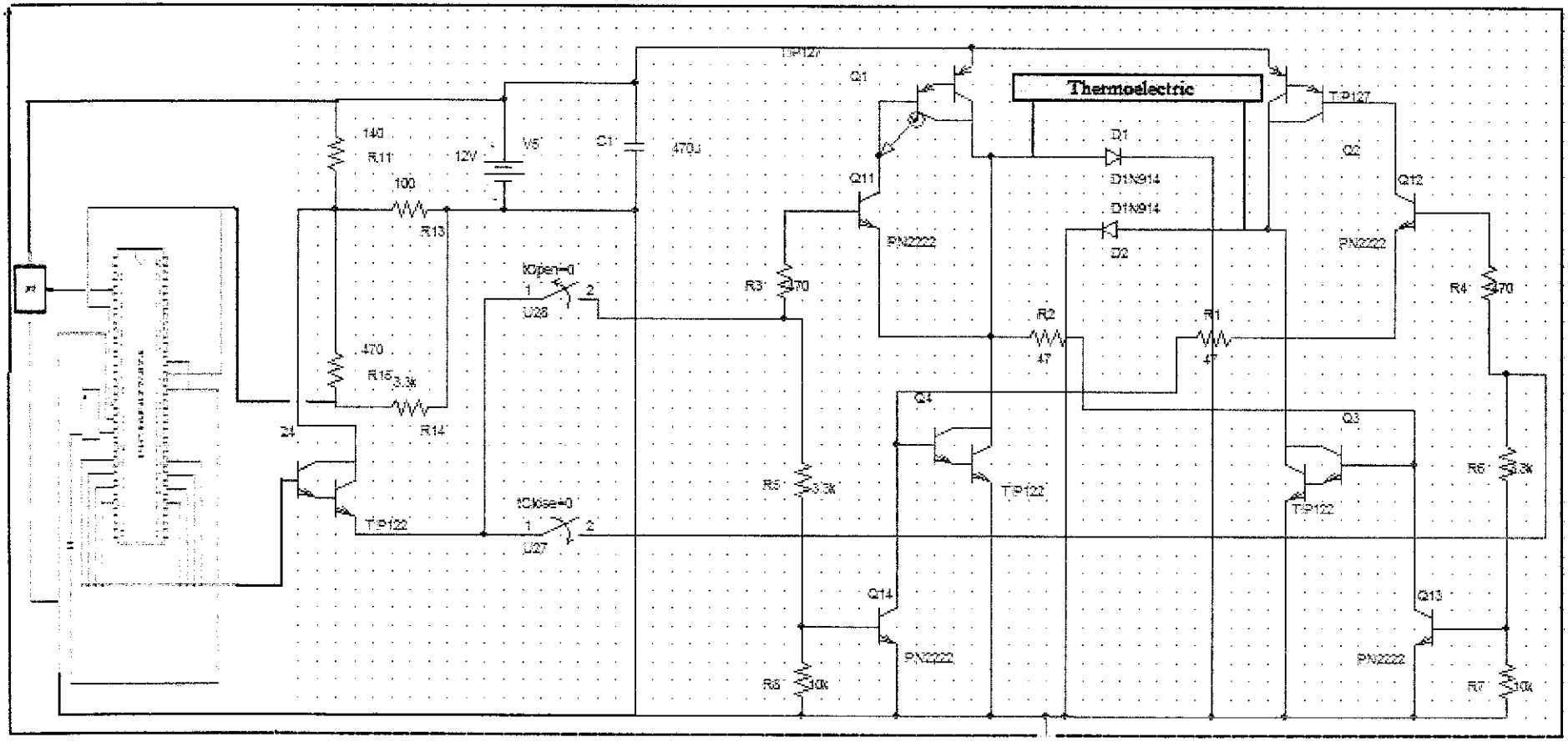


Figure 4.32: Thermoelectric Devices for Cooling and Heating circuitry

The temperature sensor used is a LM35DZ. It is located between the insulator and the container. This solid-state sensor outputs 10milliVolts per degree Fahrenheit. The temperature sensor is read by a A/D converter in PIC 16F877. The A/D converter converts the 10 milliVolts per degree Fahrenheit and send the output that will be used in the H-bridge circuit.

The peltier are connected using the H Bridge circuit. The PIC will provide appropriate voltage to the H-bridge circuit that will drive the peltier. The PIC will act as a switch on and off for the peltier to effect. The cold and hot part of the peltier will be controlled manually by the user. The control of the hot and cold part are indicated by the H-bridge circuit. When switch is toggle to switch 1, the circuit will work in clockwise flow. The peltier will act as a heater. When the switch been change to switch2, the H-bridge circuit will move in opposite direction and the peltier will act as cooler. There are LEDs (light emitting diodes) in parallel to output of the H-bridge in order to indicate the direction of the heat being pumped. The RED LED indicates that the H-bridge is in HOT mode. The GREEN LED indicates that the H-bridge is in COLD mode.

CHAPTER 5
CONCLUSION AND RECOMMENDATION

5.1 Conclusion

In conclusion, the solid-state thermoelectric device circuitry has been constructed. The capability of the thermoelectric device as a cooler and heater have been defined theoretically. Two important components making up the thermoelectric cooler or heater are the temperature controller using a microcontroller together with a temperature sensor and the H-bridge circuit that will drive the thermoelectric device in cold state or hot state. Both elements are connected in such a way as to produce a heat sink and heat source that are portable and use small amount of power in the atmosphere of a car. For the microcontroller to work, a specific program is loaded and programmed inside the memory of the PIC16F877. The method of developing the device have been searched and learned thoroughly. The simulation of the project have been successfully implemented. The final product of hardware have been constructed and it is working according to the specification.

5.2 Recommendation

For further improvement of the project, a suitable compartment that can maintain and insulate heat may be designed. The compartment can be use as storage for the beverages in order to maintain the coldness or hotness as desired by the user. It is also recommended to design a proper heat sink system for the peltier device to move the heat from- the insulated compartment to the outside environment as the peltier device absorb heat faster than sinking the heat.

REFERENCES

[1] Theoretical analysis of a feld emission enhanced semiconductor thermoelectric cooler by Moon Chung a,1, N.M. Miskovsky a, P.H. Cutler a, Nalin Kumar b, V. Patel bhe

[2] Mahan GD. Thermoelectrics. Solid State Phys 1998;51:81.

[3] Tuomi D. Thermoelectricity VIII. The thermal conductivity quality factor, QðKÞ, a semicondutor characterization tool. J Electrochem Soc 1984;131(10):2319–24.

[4] Mahan GD. Figure of merit for thermoelectrics. J Appl Phys 1989;65(4):1578–83.

[5] Mahan GD. Inhomogeneous thermoelectrics. J Appl Phys 1991;70(8):4551–9.

[6] Sofo JO, Mahan GD. Optimum band gap of thermoelectric material. Phys Rev B 1994;49(7):4565–70.

[7] http://www.inbthermoelectric.com/index.html

[8] Solid-State Cooling Devices *by* Jane Chen, Cyrus Wu

[9] http://www.bobblick.com

[10] Microcontroller Based Temperature Monitoring and control by Dogan Ibrahim

[11] www.semiconductor.com – LM35 Datasheet

[12] PIC Microcontroller – www.mikroelektronika.co.yu- PIC 16F877 Datasheet

[13] Electrical Technology – seventh edition – Hughes

[14] Electronic devices – fifth edition – Floyd

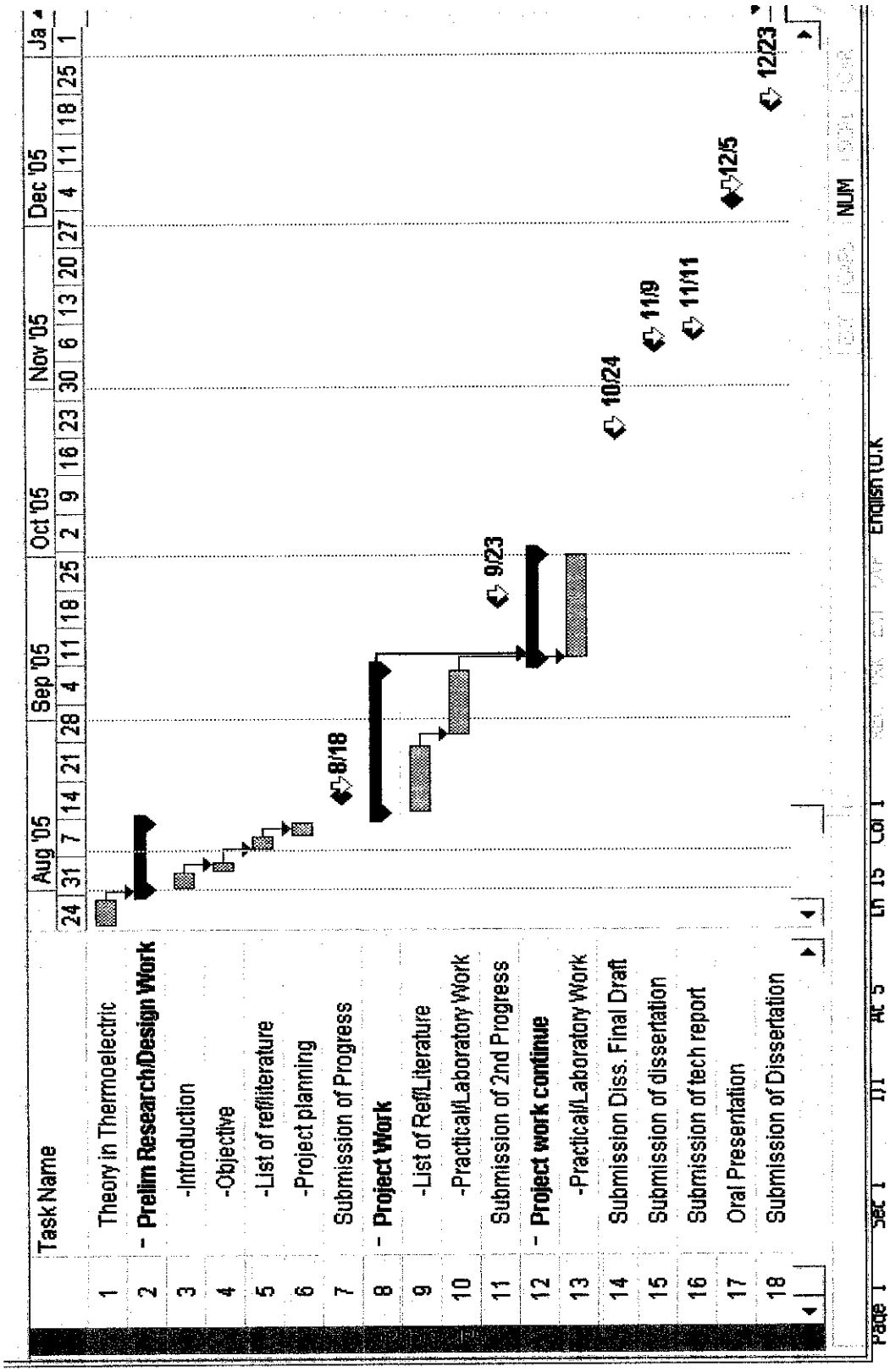
[15] Electronic devices and circuit theory – eighth edition – Robert L. Boylestad and Louis Nashelsky

APPENDICES

APPENDIX A

APPENDIX A

MILESTONE FOR FINAL YEAR PROJECT



APPENDIX B

APPENDIX B

TEMPERATURE SENSOR

National Semiconductor

November 2000

LM35
Precision Centigrade Temperature Sensors

General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Typical Applications

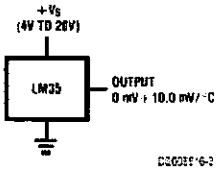
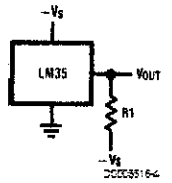


FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)

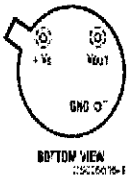


Choose R1 = −Vs/50 µA
VOUT = −1,500 mV at −150°C
= +250 mV at +25°C
= −550 mV at −55°C

FIGURE 2. Full-Range Centigrade Temperature Sensor

Connection Diagrams

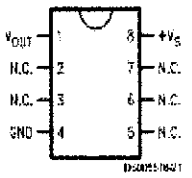
TO-46
Metal Can Package*



*Case is connected to negative pin (GND)

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

SO-8
Small Outline Molded Package



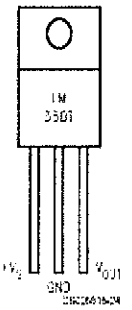
N.C. = No Connection

Top View
Order Number LM35DM
See NS Package Number M08A

TO-92
Plastic Package

Order Number LM35CZ,
LM35CAZ or LM35DZ
See NS Package Number Z03A

TO-220
Plastic Package*



*Tab is connected to the negative pin (GND).
Note: The LM35DT pinout is different than the discontinued LM35DP.

Order Number LM35DT
See NS Package Number TA03F

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temp.;	
TO-46 Package,	−60°C to +180°C
TO-92 Package,	−60°C to +150°C
SO-8 Package,	−65°C to +150°C
TO-220 Package,	−65°C to +150°C
Lead Temp.:	
TO-46 Package, (Soldering, 10 seconds)	300°C
TO-92 and TO-220 Package, (Soldering, 10 seconds)	260°C
SO Package (Note 12)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2500V
Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)	
LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35A			LM35CA			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	T_A=+25°C	±0.2	±0.5		±0.2	±0.5		°C
	T_A=−10°C	±0.3			±0.3		±1.0	°C
	T_A=T_{MAX}	±0.4	±1.0		±0.4	±1.0		°C
	T_A=T_{MIN}	±0.4	±1.0		±0.4		±1.5	°C
Nonlinearity (Note 8)	T_{MIN}≤T_A≤T_{MAX}	±0.18		±0.35	±0.15		±0.3	°C
Sensor Gain (Average Slope)	T_{MIN}≤T_A≤T_{MAX}	+10.0	+9.9, +10.1		+10.0		+9.9, +10.1	mV/°C
Load Regulation (Note 3) 0≤I_L≤1 mA	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		mV/mA
	T_{MIN}≤T_A≤T_{MAX}	±0.5		±3.0	±0.5		±3.0	mV/mA
Line Regulation (Note 3)	T_A=+25°C	±0.01	±0.05		±0.01	±0.05		mV/V
	4V≤V_S≤30V	±0.02		±0.1	±0.02		±0.1	mV/V
Quiescent Current (Note 9)	V_S=+5V, +25°C	56	67		56	67		µA
	V_S=+5V	105		131	91		114	µA
	V_S=+30V, +25°C	56.2	68		56.2	68		µA
	V_S=+30V	105.5		133	91.5		116	µA
Change of Quiescent Current (Note 3)	4V≤V_S≤30V, +25°C	0.2	1.0		0.2	1.0		µA
	4V≤V_S≤30V	0.5		2.0	0.5		2.0	µA
Temperature Coefficient of Quiescent Current		+0.39		+0.5	+0.39		+0.5	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy,	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		°C
LM35, LM35C	T_A=−10°C	±0.5			±0.5		±1.5	°C
(Note 7)	T_A=T_{MAX}	±0.8	±1.5		±0.8		±1.5	°C
	T_A=T_{MIN}	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D	T_A=+25°C				±0.6	±1.5		°C
(Note 7)	T_A=T_{MAX}				±0.9		±2.0	°C
	T_A=T_{MIN}				±0.9		±2.0	°C
Nonlinearity	T_{MIN}≤T_A≤T_{MAX}	±0.3		±0.5	±0.2		±0.5	°C
(Note 8)								
Sensor Gain	T_{MIN}≤T_A≤T_{MAX}	+10.0	+9.8, +10.2		+10.0		+9.8, +10.2	mV/°C
(Average Slope)								
Load Regulation	T_A=+25°C	±0.4	±2.0		±0.4	±2.0		mV/mA
(Note 3) 0≤I_L≤1 mA	T_{MIN}≤T_A≤T_{MAX}	±0.5		±5.0	±0.5		±5.0	mV/mA
Line Regulation	T_A=+25°C	±0.01	±0.1		±0.01	±0.1		mV/V
(Note 3)	4V≤V_S≤30V	±0.02		±0.2	±0.02		±0.2	mV/V
Quiescent Current	V_S=+5V, +25°C	56	80		56	80		µA
(Note 9)	V_S=+5V	105		158	91		138	µA
	V_S=+30V, +25°C	56.2	82		56.2	82		µA
	V_S=+30V	105.5		161	91.5		141	µA
Change of	4V≤V_S≤30V, +25°C	0.2	2.0		0.2	2.0		µA
Quiescent Current	4V≤V_S≤30V	0.5		3.0	0.5		3.0	µA
(Note 3)								
Temperature		+0.39		+0.7	+0.39		+0.7	µA/°C
Coefficient of								
Quiescent Current								
Minimum Temperature	In circuit of	+1.5		+2.0	+1.5		+2.0	°C
for Rated Accuracy	*Figure 1*, I_L=0							
Long Term Stability	T_J=T_{MAX}, for	±0.08			±0.08			°C
	1000 hours							

Note 1: Unless otherwise noted, these specifications apply: −55°C≤T_J≤+150°C for the LM35 and LM35A; −40°C≤T_J≤+110°C for the LM35C and LM35CA; and 0°C≤T_J≤+100°C for the LM35D. V_S=+5Vdc and I_{LOAD}=50 µA, in the circuit of *Figure 2*. These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1*. Specifications in **boldface** apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-220 package is 90°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mV/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

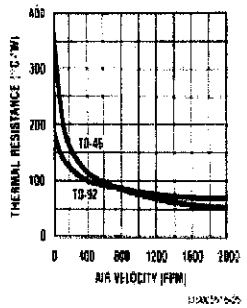
Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

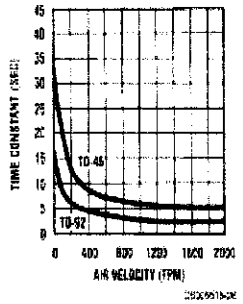
Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Typical Performance Characteristics

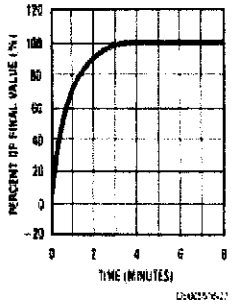
Thermal Resistance
Junction to Air



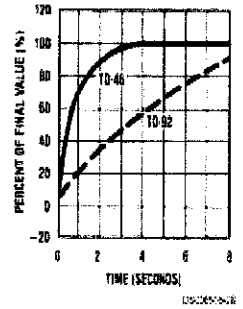
Thermal Time Constant



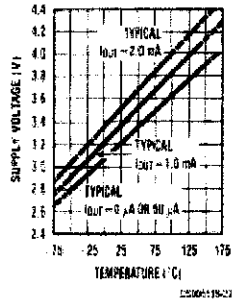
Thermal Response
in Still Air



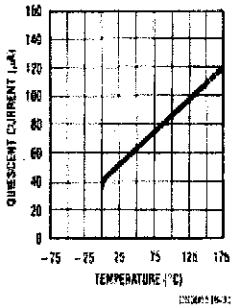
Thermal Response in
Stirred Oil Bath



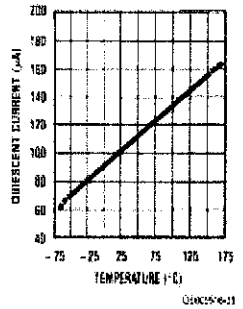
Minimum Supply
Voltage vs. Temperature



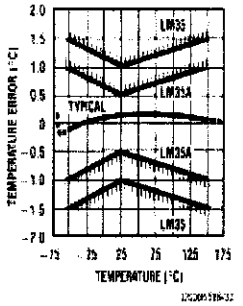
Quiescent Current
vs. Temperature
(In Circuit of *Figure 1.*)



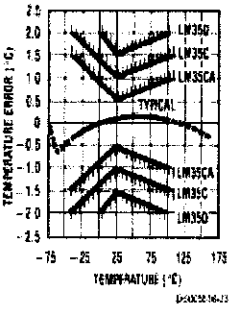
Quiescent Current
vs. Temperature
(In Circuit of *Figure 2.*)



Accuracy vs. Temperature
(Guaranteed)

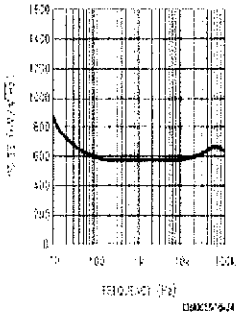


Accuracy vs. Temperature
(Guaranteed)

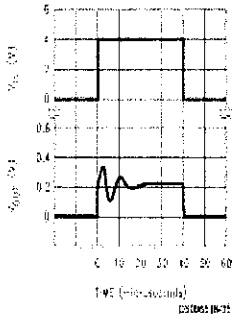


Typical Performance Characteristics (Continued)

Noise Voltage



Start-Up Response



Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is especially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

These devices are sometimes soldered to a small light-weight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

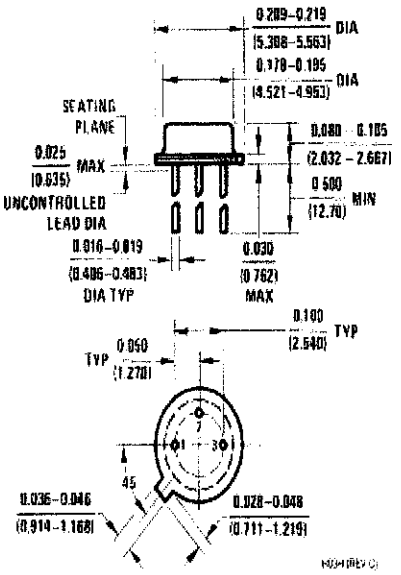
Temperature Rise of LM35 Due To Self-heating (Thermal Resistance, θ_{JA})

	TO-46, no heat sink	TO-46, small heat fin	TO-92, no heat sink	TO-92, small heat fin	SO-8, no heat sink	SO-8, small heat fin	TO-220, no heat sink
Still air	400°C/W	100°C/W	180°C/W	140°C/W	220°C/W	110°C/W	90°C/W
Moving air	100°C/W	40°C/W	90°C/W	70°C/W	105°C/W	90°C/W	26°C/W
Still oil	100°C/W	40°C/W	90°C/W	70°C/W			
Stirred oil	50°C/W	30°C/W	45°C/W	40°C/W			
(Clamped to metal, infinite heat sink)		(24°C/W)				(55°C/W)	

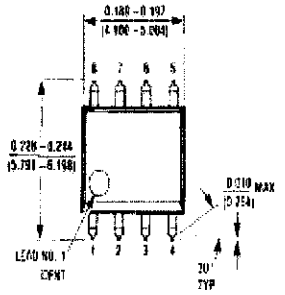
*Wakefield type 201 or 1" disc of 0.020" sheet brass, soldered to case, or similar.

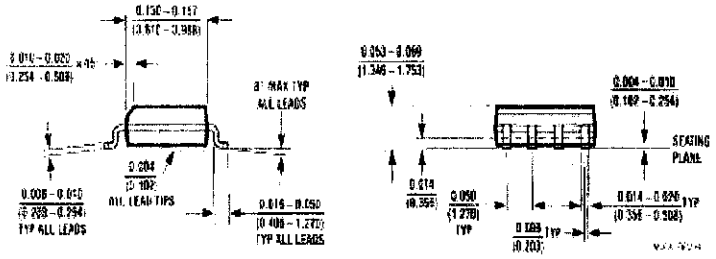
**TO-92 and SO-8 packages glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil, or similar.

Physical Dimensions inches (millimeters) unless otherwise noted



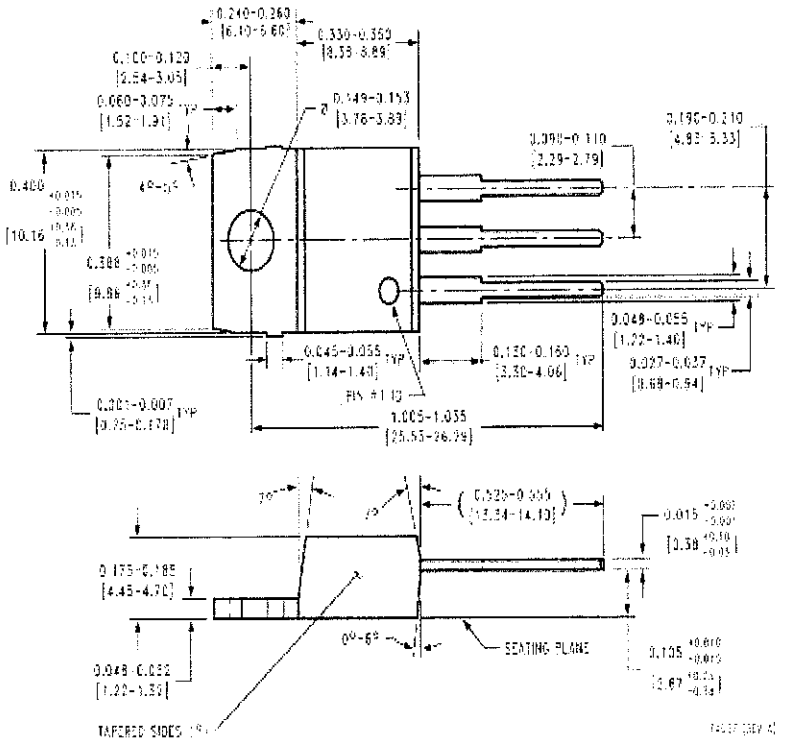
TO-46 Metal Can Package (H)
Order Number LM35H, LM35AH, LM35CH,
LM35CAH, or LM35DH
NS Package Number H03H





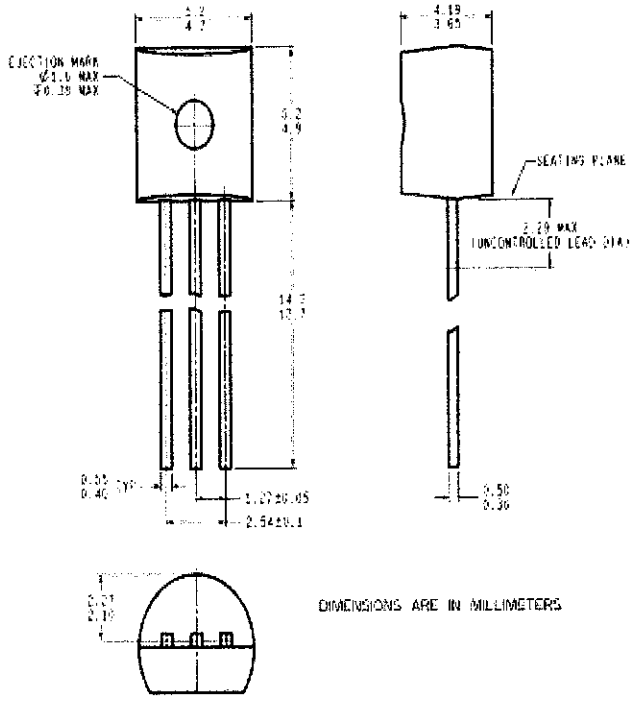
SO-8 Molded Small Outline Package (M)
Order Number LM35DM
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Power Package TO-220 (T)
Order Number LM35DT
NS Package Number TA03F

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



TO-92 Plastic Package (Z)
Order Number LM35CZ, LM35CAZ or LM35DZ
NS Package Number Z03A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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APPENDIX C

APPENDIX C

TIP 120 AND 125

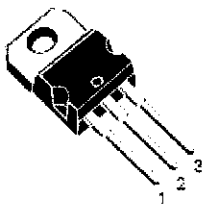
TIP120/121/122
TIP125/126/127

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

- STMicroelectronics PREFERRED SALESTYPES

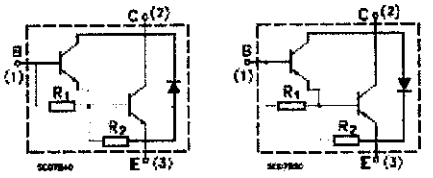
DESCRIPTION

The TIP120, TIP121 and TIP122 are silicon Epitaxial-Base NPN power transistors in monolithic Darlington configuration mounted in Jedec TO-220 plastic package. They are intented for use in power linear and switching applications. The complementary PNP types are TIP125, TIP126 and TIP127, respectively.



TO-220

INTERNAL SCHEMATIC DIAGRAM



R_1 Typ. = 5 KΩ R_2 Typ. = 150 Ω

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value			Unit
		NPN	TIP120	TIP121	TIP122	
		PNP	TIP125	TIP126	TIP127	
V_{CBO}	Collector-Base Voltage (I_E = 0)		60	80	100	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)		60	80	100	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)		5			V
I_C	Collector Current		5			A
I_{CM}	Collector Peak Current		8			A
I_B	Base Current		0.1			A
P_{tot}	Total Dissipation at $T_{case} \leq 25\ ^{\circ}C$ $T_{amb} \leq 25\ ^{\circ}C$		65 2			W W
T_{stg}	Storage Temperature		-65 to 150			°C
T_j	Max. Operating Junction Temperature		150			°C

* For PNP types voltage and current values are negative.

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.92	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	°C/W

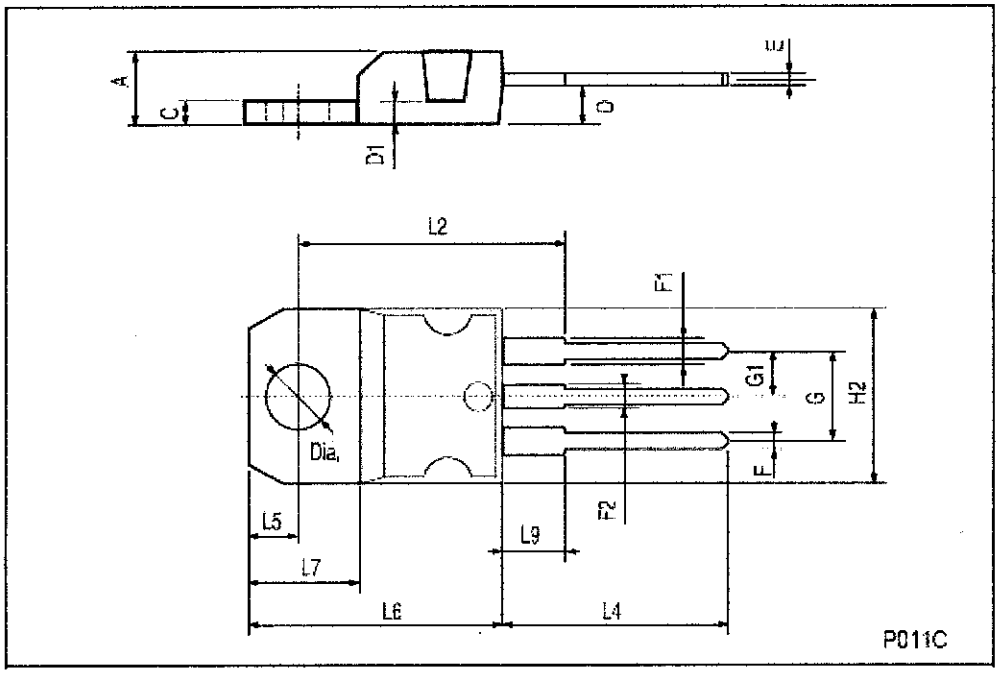
ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{CEO}	Collector Cut-off Current (I_B = 0)	for **TIP120/125**	V_{CE} = 30 V			0.5	mA
		for **TIP121/126**	V_{CE} = 40 V			0.5	mA
		for **TIP122/127**	V_{CE} = 50 V			0.5	mA
I_{CBO}	Collector Cut-off Current (I_E = 0)	for **TIP120/125**	V_{CB} = 60 V			0.2	mA
		for **TIP121/126**	V_{CB} = 80 V			0.2	mA
		for **TIP122/127**	V_{CB} = 100 V			0.2	mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V				2	mA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage (I_B = 0)	I_C = 30 mA					
		for **TIP120/125**		60			V
		for **TIP121/126**		80			V
		for **TIP122/127**		100			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 3 A	I_B = 12 mA			2	V
		I_C = 5 A	I_B = 20 mA			4	V
$V_{BE(on)}$*	Base-Emitter Voltage	I_C = 3 A	V_{CE} = 3 V			2.5	V
h_{FE}*	DC Current Gain	I_C = 0.5 A	V_{CE} = 3 V	1000			
		I_C = 3 A	V_{CE} = 3 V	1000			

* Pulsed: Pulse duration = 300 µs, duty cycle < 2 %
For PNP types voltage and current values are negative.

TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



APPENDIX D

APPENDIX D

PN2222

FAIRCHILD
SEMICONDUCTOR®

PN2222

General Purpose Transistor

TO-92

1. Emitter 2. Base 3. Collector

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	60	V
V_{CEO}	Collector-Emitter Voltage	30	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	800	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

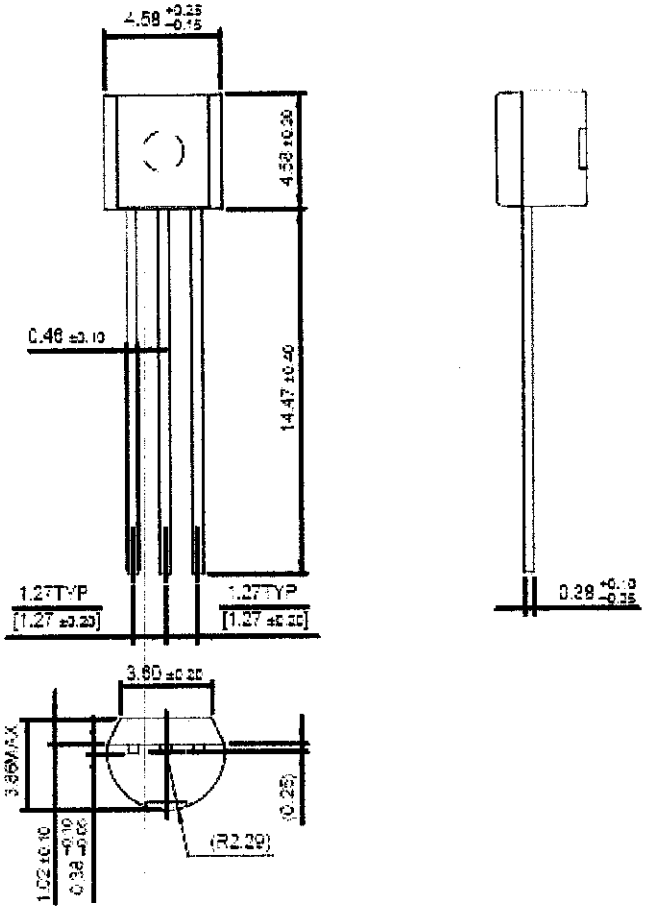
Symbol	Parameter	Test Condition	Min.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C=10μA, I_E=0	60		V
BV_{CEO}	Collector Emitter Breakdown Voltage	I_C=10mA, I_B=0	30		V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E=10μA, I_C=0	5		V
I_{CBO}	Collector Cut-off Current	V_{CB}=50V, I_E=0		0.01	μA
I_{EBO}	Emitter Cut-off Current	V_{EB}=3V, I_C=0		10	nA
h_{FE}	DC Current Gain	V_{CE}=10V, I_C=0.1mA V_{CE}=10V, *I_C=150mA	35 100	 300	
V_{CE}(sat)	* Collector-Emitter Saturation Voltage	I_C=500mA, I_B=50mA		1	V
V_{BE}(sat)	* Base-Emitter Saturation Voltage	I_C=500mA, I_B=50mA		2	V
f_T	Current Gain Bandwidth Product	V_{CE}=20V, I_C=20mA, f=100MHz	300		MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz		8	pF

* Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

Rev. A, November 2002

Package Dimensions

TO-92



Dimensions in Millimeters

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Bottomless™	FPS™	MICROCOUPLER™	PowerSaver™	SuperSOT™-3
CoolFET™	FRFET™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	GlobalOptoisolator™	MicroPak™	QFET®	SuperSOT™-8
DOME™	GTO™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	HiSeC™	MSX™	QT Optoelectronics™	TinyLogic®
E²CMOS™	I²C™	MSXPro™	Quiet Series™	TINYOPTO™
EnSigna™	i-Lo™	OCX™	RapidConfigure™	TruTranslation™
FACT™	ImpliedDisconnect™	OCXPro™	RapidConnect™	UHC™
FACT Quiet Series™		OPTOLOGIC®	µSerDes™	UltraFET®
Across the board. Around the world.™		OPTOPLANAR™	SILENT SWITCHER®	VCX™
The Power Franchise®		PACMAN™	SMART START™	
Programmable Active Droop™		POP™	SPM™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

APPENDIX E

APPENDIX E

MICROCONTROLLER

MICROCHIP

PIC16F87X

28/40-pin 8-Bit CMOS FLASH Microcontrollers

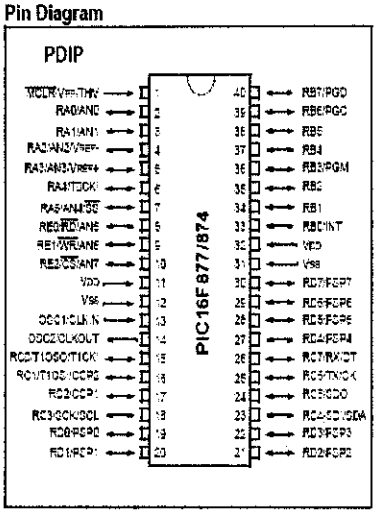
Devices Included in this Data Sheet:

- PIC16F873
- PIC16F874
- PIC16F876
- PIC16F877

Microcontroller Core Features:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of FLASH Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM)
  Up to 256 x 8 bytes of EEPROM data memory
- Pinout compatible to the PIC16C73B/74B/76/77
- Interrupt capability (up to 14 sources)
- Eight level deep hardware stack
- Direct, indirect and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and
  Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS FLASH/EEPROM technology
- Fully static design
- In-Circuit Serial Programming™ (ICSP) via two pins
- Single 5V In-Circuit Serial Programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.0V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial and Industrial temperature ranges
- Low-power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 20 µA typical @ 3V, 32 kHz
  - < 1 µA typical standby current

Pin Diagram



Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI™ (Master Mode) and I²C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

TABLE 1-1: PIC16F873 AND PIC16F876 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	9	I	ST/CMOS[3]	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	10	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP/THV	1	1	I/P	ST	Master clear (reset) input or programming voltage input or high voltage test mode control. This pin is an active low RESET to the device.
					PORTA is a bi-directional I/O port.
RA0/AN0	2	2	I/O	TTL	RA0 can also be analog input0.
RA1/AN1	3	3	I/O	TTL	RA1 can also be analog input1.
RA2/AN2/VREF-	4	4	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage.
RA3/AN3/VREF+	5	5	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage.
RA4/T0CKI	6	6	I/O	ST	RA4 can also be the clock input to the Timer0 module. Output is open drain type.
RA5/SS/AN4	7	7	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	21	I/O	TTL/ST[1]	RB0 can also be the external interrupt pin.
RB1	22	22	I/O	TTL	
RB2	23	23	I/O	TTL	
RB3/PGM	24	24	I/O	TTL	RB3 can also be the low voltage programming input.
RB4	25	25	I/O	TTL	Interrupt on change pin.
RB5	26	26	I/O	TTL	Interrupt on change pin.
RB6/PGC	27	27	I/O	TTL/ST[2]	Interrupt on change pin or In-Circuit Debugger pin. Serial programming clock.
RB7/PGD	28	28	I/O	TTL/ST[2]	Interrupt on change pin or In-Circuit Debugger pin. Serial programming data.
					PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	11	I/O	ST	RC0 can also be the Timer1 oscillator output or Timer1 clock input.
RC1/T1OSI/CCP2	12	12	I/O	ST	RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	13	13	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	14	14	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I²C modes.
RC4/SDI/SDA	15	15	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I²C mode).
RC5/SDO	16	16	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK	17	17	I/O	ST	RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	18	18	I/O	ST	RC7 can also be the USART Asynchronous Receive or Synchronous Data.
VSS	8, 19	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	20	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

TABLE 1-2: PIC16F874 AND PIC16F877 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP/THV	1	2	18	I/P	ST	Master clear (reset) input or programming voltage input or high voltage test mode control. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19	I/O	TTL	RA0 can also be analog input0.
RA1/AN1	3	4	20	I/O	TTL	RA1 can also be analog input1.
RA2/AN2/VREF-	4	5	21	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage.
RA3/AN3/VREF+	5	6	22	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage.
RA4/T0CKI	6	7	23	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/SS/AN4	7	8	24	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(1)	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3/PGM	36	39	11	I/O	TTL	RB3 can also be the low voltage programming input.
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6/PGC	39	43	16	I/O	TTL/ST(2)	Interrupt on change pin or In-Circuit Debugger pin. Serial programming clock.
RB7/PGD	40	44	17	I/O	TTL/ST(2)	Interrupt on change pin or In-Circuit Debugger pin. Serial programming data.
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	RC0 can also be the Timer1 oscillator output or a Timer1 clock input.
RC1/T1OSI/CCP2	16	18	35	I/O	ST	RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	17	19	36	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I²C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I²C mode).
RC5/SDO	24	26	43	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK	25	27	44	I/O	ST	RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	26	29	1	I/O	ST	RC7 can also be the USART Asynchronous Receive or Synchronous Data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
4: This buffer is a Schmitt Trigger input when configured in I²C mode, I²C levels when in mode and a CMOS input otherwise.

TABLE 1-2: PIC16F874 AND PIC16F877 PINOUT DESCRIPTION (CONTINUED)

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	MQFP Type	Buffer Type	Description
						PORTD is a bi-directional I/O port, or parallel slave port when interfacing to a microprocessor bus
RD0/PSP0	19	21	38	I/O	ST/TTL(3)	
RD1/PSP1	20	22	39	I/O	ST/TTL(3)	
RD2/PSP2	21	23	40	I/O	ST/TTL(3)	
RD3/PSP3	22	24	41	I/O	ST/TTL(3)	
RD4/PSP4	27	33	2	I/O	ST/TTL(3)	
RD5/PSP5	28	34	3	I/O	ST/TTL(3)	
RD6/PSP6	29	35	4	I/O	ST/TTL(3)	
RD7/PSP7	30	36	5	I/O	ST/TTL(3)	
						PORTE is a bi-directional I/O port
RE0/RD/AN5	8	9	25	I/O	ST/TTL(3)	RE0 can also be read control for the parallel slave port, or analog input.
RE1/WR/AN6	9	10	26	I/O	ST/TTL(3)	RE1 can also be write control for the parallel slave port, or analog input.
RE2/CS/AN7	10	11	27	I/O	ST/TTL(3)	RE2 can also be select control for the parallel slave port, or analog input.
VSS	12,31	13,34	6,29	P	—	Ground reference for logic and I/O pins
VDD	11,32	12,35	7,28	P	—	Positive supply for logic and I/O pins
NC	—	1,17,28, 40	12,13, 33,34		—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
4: This buffer is a Schmitt Trigger input when configured in I²C mode and is an open drain output when in I²C master mode.

2.0 MEMORY ORGANIZATION

There are three memory blocks in each of these PICmicro MCUs. The Program Memory and Data Memory have separate buses so that concurrent access can occur and is detailed in this section. The EEPROM data memory block is detailed in Section 4.0.

Additional information on device memory may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023).

2.1 Program Memory Organization

The PIC16F87X devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16F877/876 devices have 8K x 14 words of FLASH program memory and the PIC16F873/874 devices have 4K x 14. Accessing a location above the physically implemented address will cause a wrap-around.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PIC16F877/876 PROGRAM MEMORY MAP AND STACK

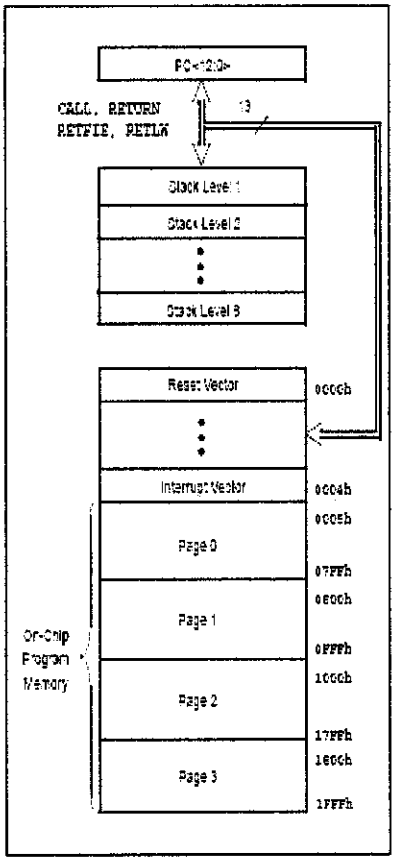
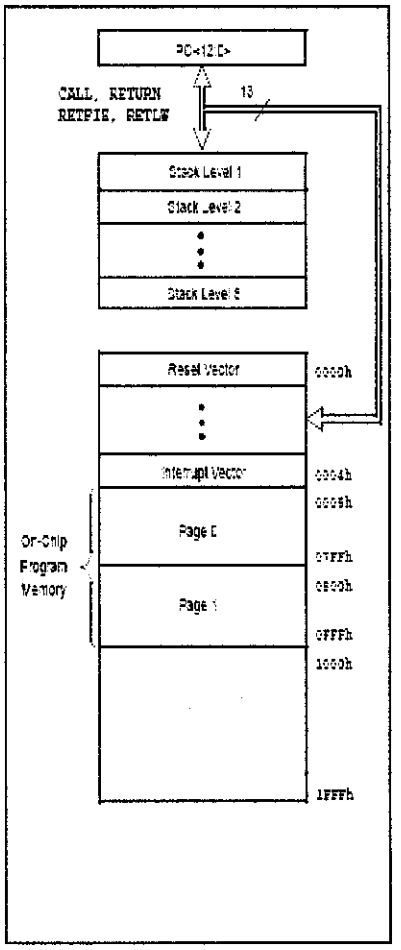


FIGURE 2-2: PIC16F874/873 PROGRAM MEMORY MAP AND STACK



2.2 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1(STATUS<6>) and RP0 (STATUS<5>) are the bank select bits.

RP1:RP0	Bank
00	0
01	1
10	2
11	3

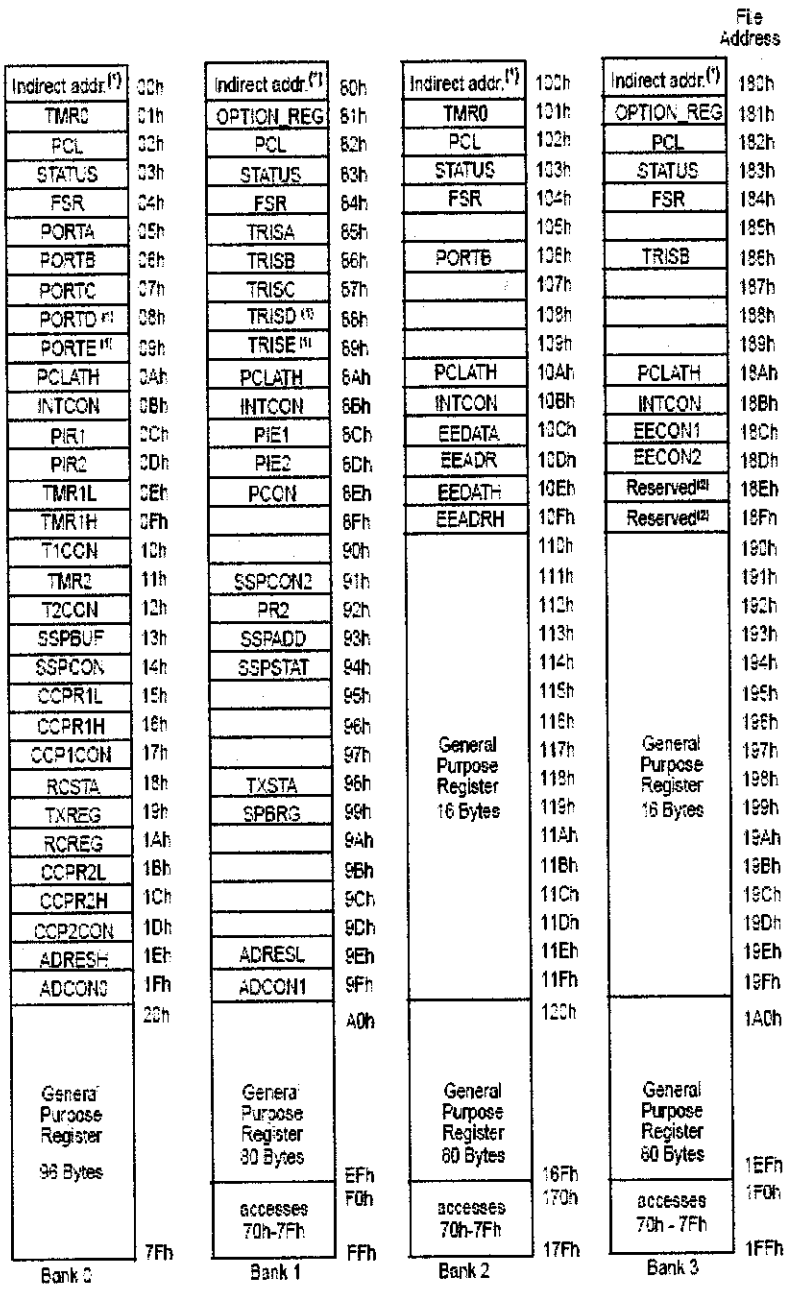
Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some "high use" Special Function Registers from one bank may be mirrored in another bank for code reduction and quicker access.

Note:	EEPROM Data Memory description can be found in Section 4.0 of this Data Sheet

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register FSR.

FIGURE 2-3: PIC16F877/876 REGISTER FILE MAP



Unimplemented data memory locations, read as '0'.

* Not a physical register.

Note 1: These registers are not implemented on 28-pin devices.

2: These registers are reserved, maintain these registers clear.

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1.

The Special Function Registers can be classified into two sets; core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral feature section.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 0											
00h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h(4)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(4)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h(4)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000	--0u 0000
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h(5)	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	uuuu uuuu
09h(5)	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
0Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(4)	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(3)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	(6)	—	EEIF	BCLIF	—	—	CCP2IF	-r-0 0--0	-r-0 0--0
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19h	TXREG	USART Transmit Data Register								0000 0000	0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000	0000 0000
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	—	ADON	0000 00-0	0000 00-0

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.

6: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 1											
80h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(4)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(4)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h(4)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
88h(5)	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h(5)	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111
8Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh(4)	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE(3)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	(6)	—	EEIE	BCLIE	—	—	CCP2IE	-r-0 0--0	-r-0 0--0
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	BOR	---- --qq	---- --uu
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
9Fh	ADCON1	ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0	0--- 0000	0--- 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Other (non power-up) resets include external reset through $\overline{MCLR}$ and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.

6: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 2											
100h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
101h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
102h(4)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
103h(4)	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx	000q quuu
104h(4)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
105h	—	Unimplemented								—	—
106h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
10Bh(4)	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
10Ch	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
10Dh	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
10Eh	EEDATH	—	—	EEPROM data register high byte						xxxx xxxx	uuuu uuuu
10Fh	EEADRH	—	—	—	EEPROM address register high byte					xxxx xxxx	uuuu uuuu
Bank 3											
180h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
182h(4)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
183h(4)	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx	000q quuu
184h(4)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
18Bh(4)	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
18Ch	EECON1	EEPGD	—	—	—	WRERR	WREN	WR	RD	x--- x000	x--- u000
18Dh	EECON2	EEPROM control register2 (not a physical register)								---- ----	---- ----
18Eh	—	Reserved maintain clear								0000 0000	0000 0000
18Fh	—	Reserved maintain clear								0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD, and TRISE are not physically implemented on the 28-pin devices, read as '0'.

6: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

3.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023).

3.1 PORTA and the TRISA Register

PORTA is a 6-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a hi-impedance mode). Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, the value is modified and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other PORTA pins have TTL input levels and full CMOS output drivers.

Other PORTA pins are multiplexed with analog inputs and analog VREF input. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

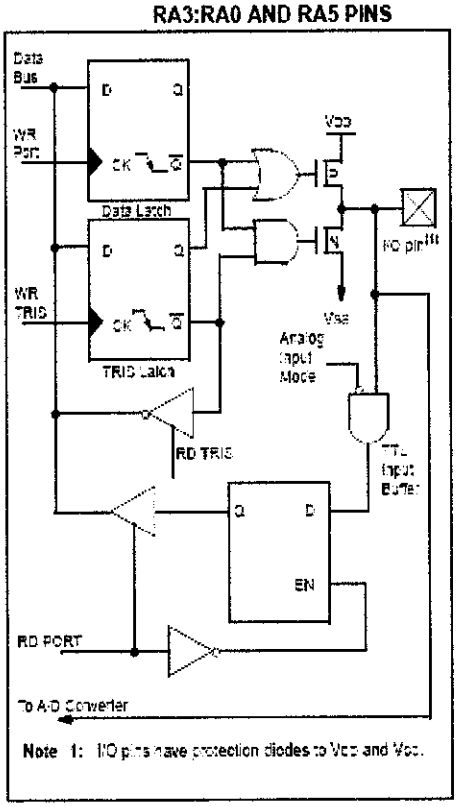
Note:	On a Power-on Reset, these pins are configured as analog inputs and read as '0'.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 3-1: INITIALIZING PORTA

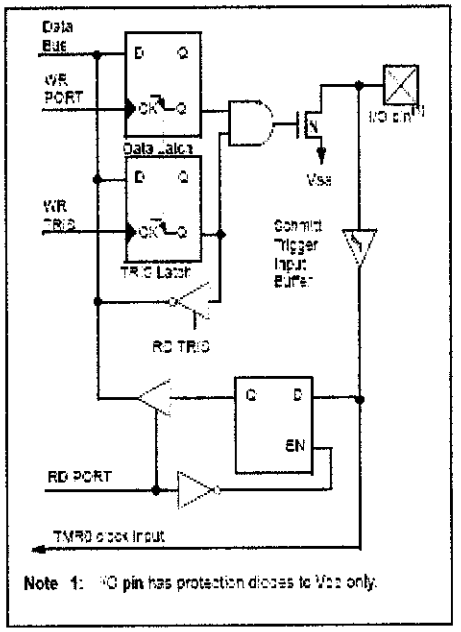
```
BCF     STATUS, RP0     ;
BCF     STATUS, RP1     ; Bank0
CLRF    PORTA           ; Initialize PORTA by
                        ; clearing output
                        ; data latches
BSF     STATUS, RP0     ; Select Bank 1
MOVLW   0x06            ; Configure all pins
MOVWF   ADCON1          ; as digital inputs
MOVLW   0xCF            ; Value used to
                        ; initialize data
                        ; direction
MOVWF   TRISA           ; Set RA<3:0> as inputs
                        ; RA<5:4> as outputs
                        ; TRISA<7:6> are always
                        ; read as '0'.
```

FIGURE 3-1: BLOCK DIAGRAM OF RA3:RA0 AND RA5 PINS



Note 1: I/O pins have protection diodes to Vdd and Vss.

FIGURE 3-2: BLOCK DIAGRAM OF RA4/T0CKI PIN



Note 1: I/O pin has protection diodes to Vss only.

TABLE 3-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input
RA1/AN1	bit1	TTL	Input/output or analog input
RA2/AN2	bit2	TTL	Input/output or analog input
RA3/AN3/VREF	bit3	TTL	Input/output or analog input or VREF
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0 Output is open drain type
RA5/SS/AN4	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
9Fh	ADCON1	ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0	--0- 0000	--0- 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note:	When using the SSP module in SPI slave mode and $\overline{SS}$ enabled, the A/D converter must be set to one of the following modes where PCFG3:PCFG0 = 0100, 0101, 011x, 1101, 1110, 1111.

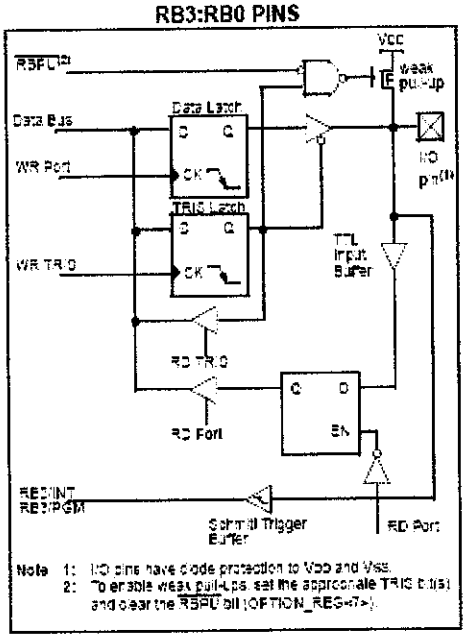
3.2 PORTB and the TRISB Register

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a hi-impedance mode). Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

Three pins of PORTB are multiplexed with the Low Voltage Programming function: RB3/PGM, RB6/PGC and RB7/PGD. The alternate functions of these pins are described in the Special Features Section.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit $\overline{\text{RBPU}}$ (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

FIGURE 3-3: BLOCK DIAGRAM OF RB3:RB0 PINS



Note 1: I/O pins have diode protection to VDD and VSS.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit (OPTION_REG<7>).

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

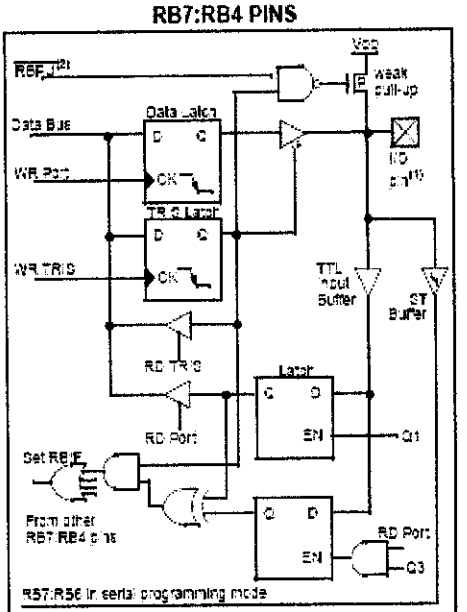
The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

This interrupt on mismatch feature, together with software configureable pull-ups on these four pins, allow easy interface to a keypad and make it possible for wake-up on key-depression. Refer to the Embedded Control Handbook, *"Implementing Wake-Up on Key Stroke"* (AN552).

RB0/INT is an external interrupt input pin and is configured using the INTEDG bit (OPTION_REG<6>).

RB0/INT is discussed in detail in Section 12.10.1.

FIGURE 3-4: BLOCK DIAGRAM OF RB7:RB4 PINS



Note 1: I/O pins have diode protection to VDD and VSS.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit (OPTION_REG<7>).

Note: When using Low Voltage ICSP Programming (LVP) and the pull-ups on PORTB are enabled, bit 3 in the TRISB register must be cleared to disable the pull-up on RB3 and ensure the proper operation of the device.

TABLE 3-3: PORTB FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM	bit3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6/PGC	bit6	TTL/ST(2)	Input/output pin (with interrupt on change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit7	TTL/ST(2)	Input/output pin (with interrupt on change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 3-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h, 181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

3.3 PORTC and the TRISC Register

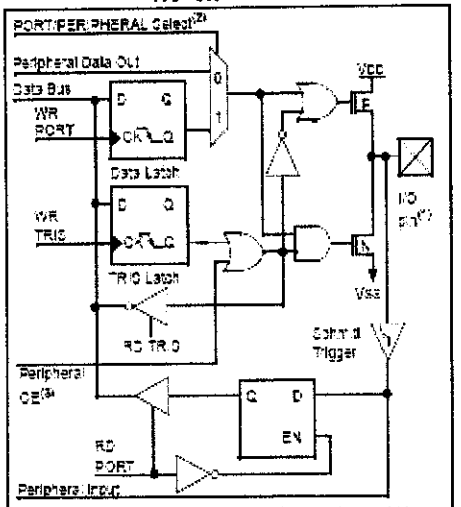
PORTC is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (=1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a hi-impedance mode). Clearing a TRISC bit (=0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin).

PORTC is multiplexed with several peripheral functions (Table 3-5). PORTC pins have Schmitt Trigger input buffers.

When the I^2C module is enabled, the PORTC (3:4) pins can be configured with normal I^2C levels or with SMBUS levels by using the CKE bit (SSPSTAT <6>).

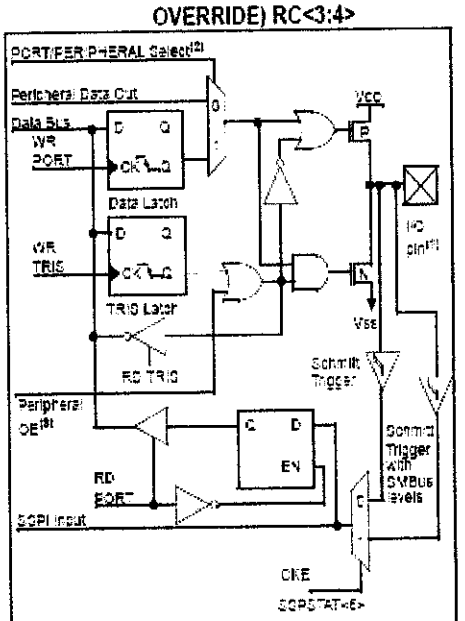
When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (**BSF, BCF, XORWF**) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

FIGURE 3-5: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE) RC<0:2> RC<5:7>



Note 1: I/O pins have diode protection to VDD and VSS.
2: Port/Peripheral select signal selects between port data and peripheral output.
3: Peripheral OE (output enable) is only activated if peripheral select is active.

FIGURE 3-6: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE) RC<3:4>



Note 1: I/O pins have diode protection to VDD and VSS.
2: Port/Peripheral select signal selects between port data and peripheral output.
3: Peripheral OE (output enable) is only activated if peripheral select is active.

TABLE 3-5: PORTC FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/ Compare2 output/PWM2 output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data output
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit or Synchronous Clock
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive or Synchronous Data

Legend: ST = Schmitt Trigger input

TABLE 3-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged.

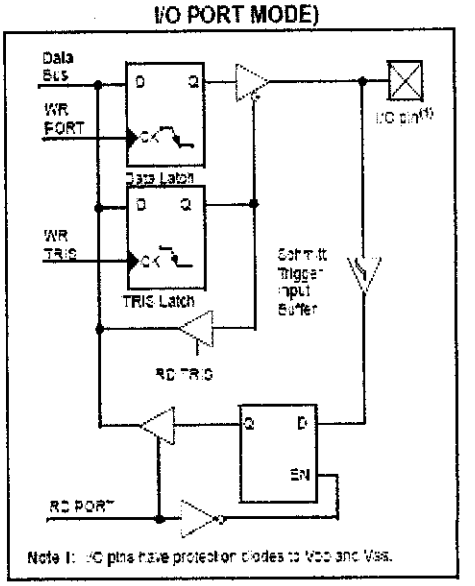
3.4 PORTD and TRISD Registers

This section is not applicable to the PIC16F873 or PIC16F876.

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

FIGURE 3-7: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 3-7: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL(1)	Input/output port pin or parallel slave port bit0
RD1/PSP1	bit1	ST/TTL(1)	Input/output port pin or parallel slave port bit1
RD2/PSP2	bit2	ST/TTL(1)	Input/output port pin or parallel slave port bit2
RD3/PSP3	bit3	ST/TTL(1)	Input/output port pin or parallel slave port bit3
RD4/PSP4	bit4	ST/TTL(1)	Input/output port pin or parallel slave port bit4
RD5/PSP5	bit5	ST/TTL(1)	Input/output port pin or parallel slave port bit5
RD6/PSP6	bit6	ST/TTL(1)	Input/output port pin or parallel slave port bit6
RD7/PSP7	bit7	ST/TTL(1)	Input/output port pin or parallel slave port bit7

Legend: ST = Schmitt Trigger input TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffer when in Parallel Slave Port Mode.

TABLE 3-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PORTD.

3.5 PORTE and TRISE Register

This section is not applicable to the PIC16F873 or PIC16F876.

PORTE has three pins, RE0/$\overline{RD}$/AN5, RE1/$\overline{WR}$/AN6 and RE2/$\overline{CS}$/AN7, which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers.

I/O PORTE becomes control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs). Ensure ADCON1 is configured for digital I/O. In this mode, the input buffers are TTL.

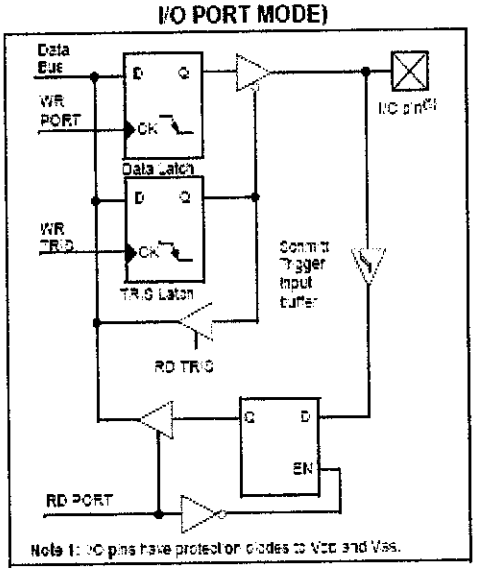
Register 3-1 shows the TRISE register, which also controls the parallel slave port operation.

PORTE pins are multiplexed with analog inputs. When selected as an analog input, these pins will read as '0's.

TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Note:	On a Power-on Reset, these pins are configured as analog inputs.

FIGURE 3-8: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)



Note 1: I/O pins have protection diodes to VDD and VSS.

REGISTER 3-1: TRISE REGISTER (ADDRESS 89h)

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
IBF	OBF	IBOV	PSPMODE	—	bit2	bit1	bit0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Parallel Slave Port Status/Control Bits

bit 7: **IBF:** Input Buffer Full Status bit
1 = A word has been received and is waiting to be read by the CPU
0 = No word has been received

bit 6: **OBF:** Output Buffer Full Status bit
1 = The output buffer still holds a previously written word
0 = The output buffer has been read

bit 5: **IBOV:** Input Buffer Overflow Detect bit (in microprocessor mode)
1 = A write occurred when a previously input word has not been read (must be cleared in software)
0 = No overflow occurred

bit 4: **PSPMODE:** Parallel Slave Port Mode Select bit
1 = Parallel slave port mode
0 = General purpose I/O mode

bit 3: **Unimplemented:** Read as '0'

PORTE Data Direction Bits

bit 2: **Bit2:** Direction Control bit for pin RE2/$\overline{CS}$/AN7
1 = Input
0 = Output

bit 1: **Bit1:** Direction Control bit for pin RE1/$\overline{WR}$/AN6
1 = Input
0 = Output

bit 0: **Bit0:** Direction Control bit for pin RE0/$\overline{RD}$/AN5
1 = Input
0 = Output

APPENDIX F

APPENDIX F

MICROCONTROLLER LANGUAGE

Microcontroller Language

```
#include <p16f877.inc>

                cblock  0x20    ;start the general purpose registers
                NumL
                NumH
                endc
;start the program
                ORG     0x0000
                GOTO    Initialise
                ORG     0x0004          ;set interrupt

Initialise
        clrf    PORTA
        clrf    PORTB
        clrf    PORTC
        BANKSEL         ADCON1                  ;disable A/D conversion on start
        movlw   0x06
        movwf   ADCON1                  ;initiate AD conversion
        BANKSEL         PORTA

setPorts bcf    STATUS, RP0     ;select bank 0
        call    Init_ADC0       ;initialise A/D conversion
        bsf     STATUS, RP0
        bcf     STATUS, RP1     ;select bank 1
        movlw   H'00'
        movwf   TRISC           ;set port C as output
        movlw   H'FF'           ;set port B as input from digital conversion
        bcf     STATUS, RP0     ;clear bank 0

Main
        btfsc   PORTB, 0
        call    temp
```

```
                goto    Main

Init_ADC0                               ;set for AN0
                movlw   b'01000001'     ;select port A as pin 0
                movwf   ADCON1                  ;set the ADCON1
                movlw   b'00000000'     ;enable A/D conversion
                movwf   ADCON1
                BANKSEL         ADCON0
                Return

Init_ADC1                               ;set for AN1
                movlw   b'01001001'     ;select port A as pin 1
                movwf   ADCON0                  ;set the ADCON1
                BANKSEL         ADCON1
                movlw   b'00000000'     ;enable A/D conversion
                movwf   ADCON1
                BANKSEL         ADCON0
                Return

Read_ADC        bsf     ADCON0, GO_DONE     ;initiate the A/D
                btfsc   ADCON0, GO_DONE
                goto    $ -1                ;wait for ADC to finish
                movf    ADRESH,W
                movwf   PORTC
                return

temp
                call    Init_ADC0
                call    Read_ADC
                return

                end
```