PERFORMANCE STUDY OF 1 BIT STATIC RAM BASED ON PROCESS TECHNOLOGIES

By

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DISSERTATION

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
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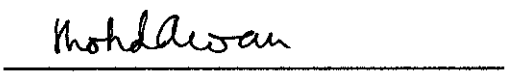
Approved:



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TRONOH, PERAK

MAY 2011

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Nadiah.

(Nadiah Binti Md Tumiran)

ABSTRACT

A basic memory cell of Static Random Access Memory (SRAM) topology consists of four transistors which act as a flip flop and two more transistors will act as pass transistor. In this study, experiment is done by varying the values of different variables that can affect the performance of basic memory cell. Among the variables are magnitudes of voltage supply, temperature, clock frequency and process technology to be used in fabrication of memory cell. These variables will have their own limit due to the configuration of circuit and properties transistor parameters in the memory cell. These values will determine the performance of the memory cell. The studies are carried out using various process technologies by simulation at schematic level. The results show that higher clock frequency will require higher value of supplied voltage. Lower supplied voltage will make SRAM failed to operate at high temperature. Different process technology will also influence the value for minimum supplied voltage used and temperature range that the SRAM circuit can operate properly. The process technology of hp14tb has the minimum voltage supply of 0.83 V at 5 MHz while ami16 has the widest effective range temperature from -229°C to 224°C at 100MHz and 1.3 V simulation.

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LIST OF ABBREVIATION AND NOMENCLATURE

ROM	Read Only Memory
RAM	Random Access Memory
SRAM	Static Random Access Memory
ENIAC	Electronic Numerical Integrator and Computer
LSI	Large Scale Integrated
TTL	Transistor-transistor Logic
ECL	Emitter-Coupled Logic
MOSFET	Metal Oxide Silicon Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
ZBT	Zero Bus Turnaround
syncBurst	synchronous-burst
DDR	Double Data Rate
I/O	Input/Output
NMOS	N-channel Metal Oxide Semiconductor
FinFET	Fin Field Effect Transistor
PMOS	P-channel Metal Oxide Semiconductor
R/W	Read/Write
W/L	Width/Length
CPU	Central Processing Unit
ALU	Arithmetic Logic Unit
6T	six transistor
DVFS	Dynamic Voltage and Frequency Scalling

CHAPTER 1

INTRODUCTION

1.1 Background of Study

In a digital computer, there is a portion inside it that stores information of binary words for later usage. This portion is called memory. Memory of a computer not only limited in storing program and data during program execution but memory also stored processed data. Memory can be divided into two categories which is magnetic core memory and semiconductor memory. These memories are the main memory of a digital computer. There are three main operations involved in dealing with memory. The first operation is addressing. Each location inside the memory can be accessed by addressing that particular cell using address decoder. After the cell memory is addressed, write and read operations can be done to the desired memory cell. Information is introduced into memory by write operation while information is acquired from memory by read operation [1].

1.1.1 Semiconductor Memories

The name of this memory comes from the binary cells that store bits in the matrix form are made of semiconductor material. Semiconductor memory is broadly categorized into Read Only Memory (ROM) and Random Access Memory (RAM). ROM is mainly used for storing control program while RAM is used as temporary storage for current data [1].

1.1.2 RAM

Basic unit for RAM is called binary cell which utilize the concept of a flip-flop. This binary cell stored either a 1 or 0 inside one unit as long as the power is available. RAM is also called as read write memory as the previously stored data can be erased and replaced with new data by writing process. This memory belongs to the volatile memory as binary cell becomes 0 regardless of the previous data that it holds once the power supply is off. Since the read operation in RAM does not change the stored data in the previous write operation, RAM is grouped under the non destructive memory [1].

1.1.3 SRAM

Static Random Access Memory (SRAM) is one type of RAM used in memory of a computer. This memory does not need to be refreshed all the time for the binary cell to hold its data. The disadvantages of this memory are that it is slow in speed and require large semiconductor area. Moreover, this memory will consume a significant amount of power. All these criteria make it not favorable to be used in very large size memories [1].

1.1.4 SRAM History

In the early computer memory system of the year 1945, mercury and nickel wire delay lines was used as memory in the Electronic Numerical Integrator and Computer (ENIAC) that was made by thousands of vacuum tubes. Later in the year 1952, core memory was invented. It was made of a small ring of ferrite which is a ferromagnetic ceramic material that could be magnetized in two different directions that can be translated as 0's or 1's. This core will hold one bit of information either a 1's or 0's depends on the magnetic charge direction when it is magnetized [2].

The first development was made by Intel Corporation in the year of 1969 with the intention to replace the traditional computer core memory systems. The new product was made based upon low-cost standardized circuits in high volume that incorporates Large Scale Integrated (LSI) technology. The first product from Intel was a 64-bit bipolar high-speed RAM chip that was called as the 3130 Shottky model. The second product from the company was a 256-bit Static RAM memory chip, model 1101 [3].

1.1.5 Types of SRAM

There are many type of SRAM that can be categorized based on many categories. If categorized based on transistor type, SRAM have two types which is bipolar junction transistor that is used in Transistor-transistor Logic (TTL) and Emitter-Coupled Logic (ECL) whereby it is fast in speed but consumed a lot of power. While Metal Oxide Silicon Field Effect Transistor (MOSFET) type that is used in Complementary Metal Oxide Semiconductor (CMOS) is low on power and commonly used today.

There are two types of function for SRAM which is asynchronous whereby it is independent of clock frequency so that data in and data out are controlled by address transition. The second type is synchronous whereby all timings are initiated by the clock edges so that address, data in and other control signals are dependent with the clock signals [2]. SRAM can also be categorized base on its feature. There are many features available currently for SRAM. Among them is ZBT (Zero Bus Turnaround), syncBurst (synchronous-burst), DDR (Double Data Rate), Quad Data Rate, Pipelined and Late-Write SRAM [4].

The turnaround for ZBT SRAM or the number of clock cycles it takes to change from write to read access to the SRAM and vice versa is zero. The syncBurst SRAM features synchronous burst write access to the SRAM in order to increase the write operation of SRAM. DDR SRAM is a synchronous, single read/write port with double data rate of I/O (Input/Output).

In Quad Data Rate SRAM, it is a synchronous with separate read and write ports and a quadruple data rate I/O. Pipelined SRAM is also called as register to register mode SRAM whereby a register is added in between memory and output. In a Late-Write SRAM, input data only needed at the end of the cycle [4]. The commonly used SRAM today is of MOSFET type that can be further classified which is N-channel Metal Oxide Semiconductor (NMOS), CMOS and Fin Field Effect Transistor (FinFET).

1.1.5.1 NMOS SRAM

NMOS SRAM binary cell is designed with two inverters whereby both inputs and outputs are cross-coupled with each other to form a basic flip-flop circuit. The cross-coupled transistors are of enhancement mode NMOS transistor. The load devices used in this type of memory cell can either be two depletion-mode transistors or two polysilicon resistors. Load device that use high-valued resistors has improved the memory design in terms of less power dissipation and a compact, high density memory. The biggest disadvantage for this design is that the memory device will be larger in size that makes it not profitable to be fabricated [5].

There are two NMOS transmission gate transistor that act as a pass transistor in which they are connected to the memory cell with the complementary bit lines. Read and write operation can be accessed to the memory cell by the use of pass transistor. When the word line signal is low, pass transistors are cut off and memory cell is isolated to the bit lines. In this standby condition, the stored data inside the memory remain as long as power is supplied to the cell. When word line signal is high, pass transistors are bias and memory cell is connected to bit lines. Thus, data can be read or write into the memory cell [5].

1.1.5.2 CMOS SRAM

In CMOS SRAM binary cell design, the load device consists of two p-channel Metal Oxide Semiconductor (PMOS) transistors. The same design of cross-coupled inverter in NMOS SRAM is used in this memory cell to make a simple flip-flop. Moreover, the same concept of pass transistor also used in this design. The advantages for using CMOS technology are low static power dissipation, superior noise immunity, wide operating temperature range, sharp transfer characteristics and wide voltage supply tolerance [6].

CMOS technology is essentially using a lower power than NMOS due to the conducting paths between power and ground does not arise during either one of logic state. Furthermore, current is drawn only during switching time since the p- channel and n- channel devices will both turn on at small amount of time due to the both channels are in series configuration. Hence, this memory uses less power in the standby mode since the contributors are only surface, junction and channel leakage currents.

1.1.5.3 FinFET SRAM

The gate-length scaling can be further scaled down to 10-nm [7], [8] by using the thin-body transistor structure of FinFET technology. Moreover, this technology can enhance the SRAM performance through independent gating. This technology also allows lightly doped channel, insignificant depletion charge and capacitance which resulted in a memory with a steep sub-threshold slope and parasitic device with lower capacitance [9]. The schematic of SRAM by using FinFET is basically the same with CMOS technology with verification of a conventional double-gated design and the parameters values during the simulation process such as the channel doping. Hence, the basic concepts of a flip-flop and pass transistor are also applied to this memory cell.

1.2 Problem Statement

Static RAM is important in a computer as it hold the operating system information which contributes to the speed of the computer itself. There are many factors that can affect the performance of SRAM which are process technology, supplied voltage, temperature, access period time and configuration of memory cell. The performance of SRAM can be studied by investigating the dependence of 1-bit SRAM before continuing for the larger capacity. Schematics and simulation for this 1-bit memory cell will be done by using process technologies available in the Cadence software in UTP.

1.3 Objectives

The objective for this project is to analyze the performance of 1-bit SRAM basic memory cell based on several different states or conditions that will be manipulated with the selected parameters and also based on several process technologies available in the market. All schematics and simulations are done by using Cadence software. The study includes the limitations of process technology, clock frequency, supplied voltage and temperature that affect the read and write-ability (data stability), function and density of memory cell.

1.4 Scope of Study

The scope of this project includes the drawing for a schematic of 1-bit Static RAM basic memory cell consisting six transistors. Later, simulation for process of Read/Write (R/W) from and to the unit cell will be done by verifying the input and output signal of binary data (0/1). Next, the memory cell is simulated based on several conditions which is the magnitude of supplied voltage, temperature and clock frequency will be changed in order to analyze the memory performance. A detailed discussion for the memories performance will be done later on.

For the optimization in terms of Width/Length (*W/L*) of the transistor, few experiments will be conducted by using optimization tools in the Cadence software. All simulations will be done by using the same manipulator parameters as before to study the memory cell performance. Further discussion will be done in analyzing the performance of memory cell based on several process technologies. This will complete the analysis for the performance of SRAM based on different state or condition and several process technologies.

CHAPTER 2

LITERATURE REVIEW

2.1 Digital Computer

The memory unit is a device in digital computer which stored program and data of binary words. There are three groups of memory components in the computer system which is main memory, secondary memory and internal processor memory. These memories are group according to their characteristic. The main memory or primary memory can be accessed directly by Central Processing Unit (CPU). This memory stored program and data during the computer operation. The total capacity for this memory varies from few kilo-bytes to several mega-bytes depending on the computing system. The secondary or auxiliary memory stored program and large data files that are not required by the CPU constantly. Hence, this memory is bigger in capacity but with slower speed than main memory. The internal processor memory is the inner-most memory of the computer. The speed for this memory is higher compared to the other two memories as this memory will be combined together with the Arithmetic Logic Unit (ALU) and control unit and then integrated into single chip. This CPU is expensive and also limits the capacity of the memory to be built inside [6].

2.2 Types of Semiconductor Memories

There are different types of semiconductor memories available nowadays which can be categorized into two main categories. Figure 1 shows the classification of memories in a digital computer.

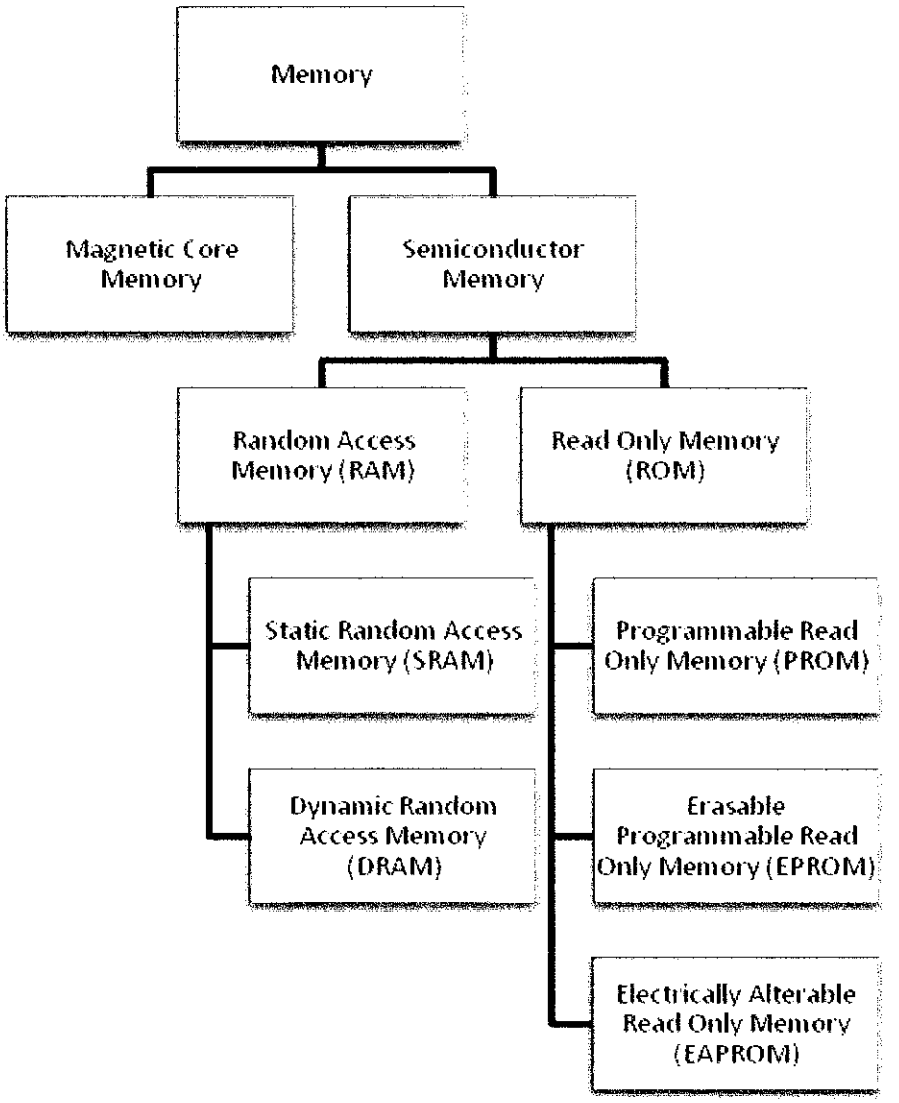

Figure 1 : Classification of memories in a digital computer [1]

2.3 SRAM Memory Cells

Static RAM is a basic bistable flip-flop circuit that can retain its memory with only a dc current or voltage applied to the binary cell. SRAM is large in size as one cell consists of six transistors in a cell. In brief, the invention of a memory cell comprises of two transistors act as cross-coupled drive transistors, another two transistors act as floating-gate load devices and two transistors act as word-select pass transistors. Nevertheless, this memory does not require additional complexity of refresh cycle and refresh circuitry thus making it faster in terms of speed. The binary cell of SRAM has been evolving rapidly throughout the years as technology is growing day by day.

As memory is made from logic gates through MOSFET thus, the density of memory must be scaled in order to keep track with scaling trend of MOSFETs [10]. The commonly used structure for a memory cell comprises of six NMOS enhancement mode transistors [11]. The cell size must be reduced and circuit should be functioning properly in a low voltage mode.

2.4 SRAM Cell Operation

There are three main operations in a basic memory cell which is read, write and standby mode. In a standby mode, the circuit is idle whereby the word line is not accessed thus separating memory cell from bit lines by the pass transistor. The cross-coupled inverters will continue reinforce each other without any interference from outside of the basic cell [11].

In this basic memory cell, six transistors (6T) is used as shown in Figure 2 and the schematic for complete circuit that is used in the simulation process can be referred in the Appendix III.

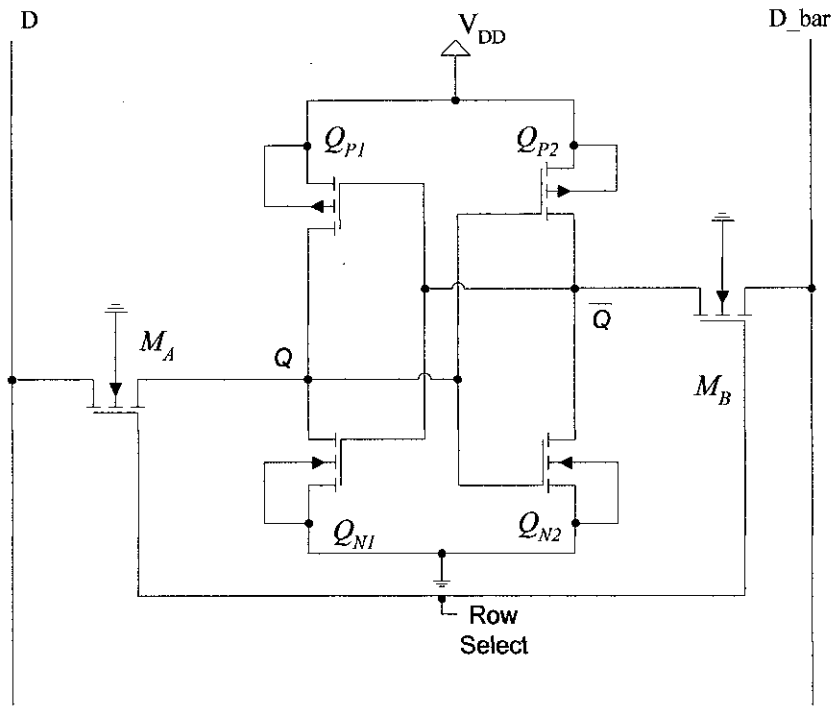

Figure 2 : 6T Cell Basic Memory Topology [11]

In this circuit, the output of the cross-coupled inverters will be in two static conditions which is 0's or 1's for one bit stored information. When $\bar{Q}$ is in low voltage or logic 0, transistor Q_{P1} is on while Q_{N1} is cut off so that Q is in high voltage or logic 1. This lead to Q_{P2} to cut off while Q_{N2} is on thus make certain that $\bar{Q}$ in logic 0. When Q is in logic 0, transistor Q_{P2} is on while Q_{N2} is cut off so that $\bar{Q}$ is logic 1. This in turn make Q_{P1} to cut off while Q_{N1} is on thus make sure that $\bar{Q}$ in logic 1. The pass transistors which are M_A and M_B will then connect the basic memory to the data lines so that the stored data at both Q and $\bar{Q}$ is accessible to the read circuit [5].

The supplied voltage to the SRAM must be stable and not to fluctuate beyond ±10% of the main supplied (V_{DD}). SRAM uses low voltage supply and draw little power.

2.5 Pull-up Circuit

A basic memory cell that uses CMOS technology can be further improved by adding elements for greater performance result. Pull-up circuit consists of two PMOS transistor that are located at the complementary data bit lines as shown in Figure 3.

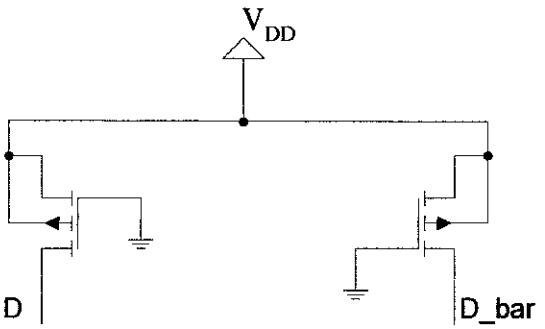

Figure 3 : Pull-up Circuit [5]

These additional features are added to improve the diffusion structure in order to enhance the immunity of SRAM against the electrostatic discharge [5].

2.6 Write Circuits

The write circuit has two inputs which is data that will be written into cell memory and write enable signal. This circuit is a multiplexer gate made from CMOS application to give high or low voltage at node bit line so that state '0' or '1' can be passed to node Q and $\bar{Q}$. Figure 4 and Figure 5 show the write circuit for input D and D_bar, respectively.

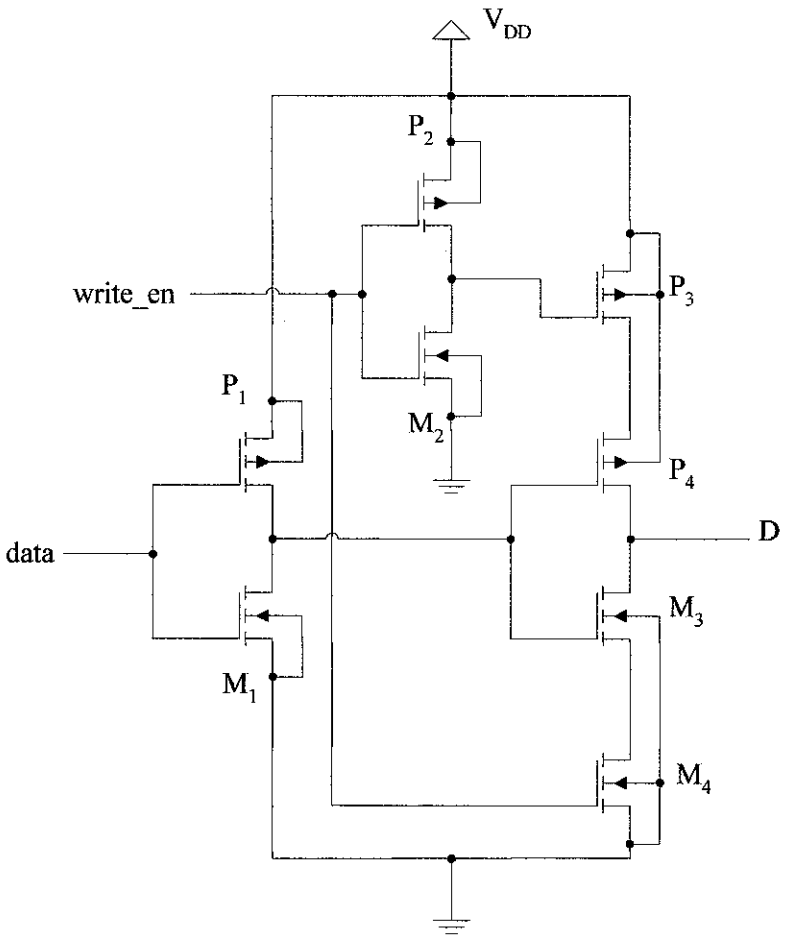

Figure 4 : Write Circuit for Input D

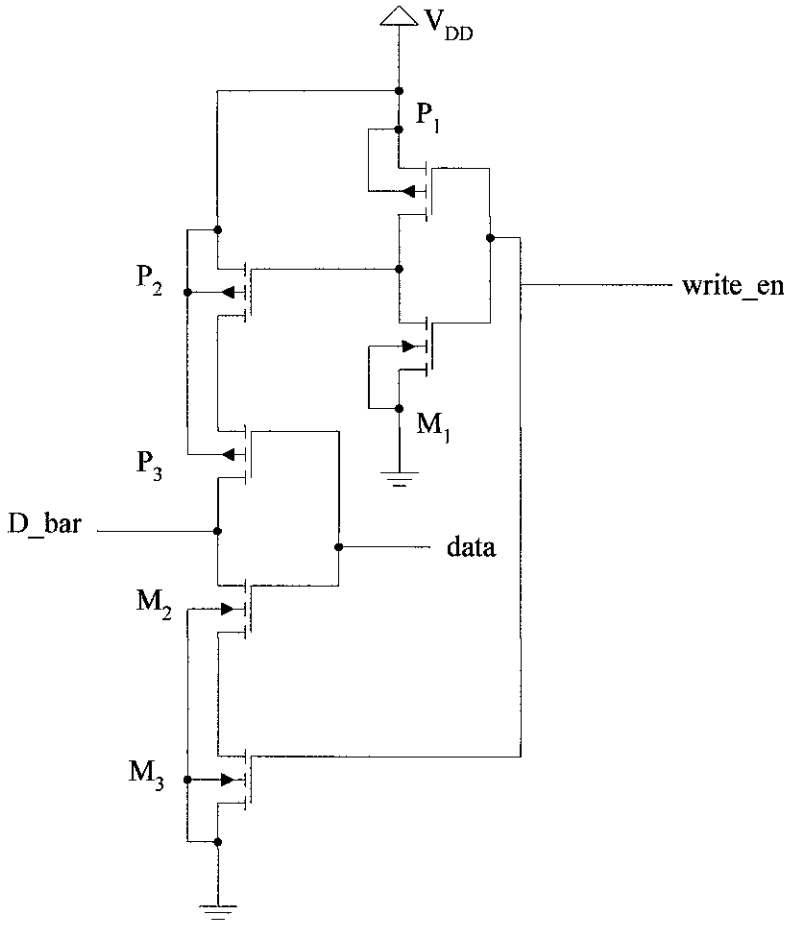

Figure 5 : Write Circuit for Input D_bar

2.7 Read Circuit

Figure 6 shows the read circuit that uses CMOS transistors. The read circuit used in this project is a semi-latch sense amplifier which is the improved version of voltage sense amplifier [12]. This circuit utilizes the concept of cross-coupled sense amplifier whereby the inputs are connected to the data bit lines through another pass transistor that is activated by the read signal. When sense_en signal is low, both data bit lines will get pass through flip-flop output circuit and output will follow D-bit state.

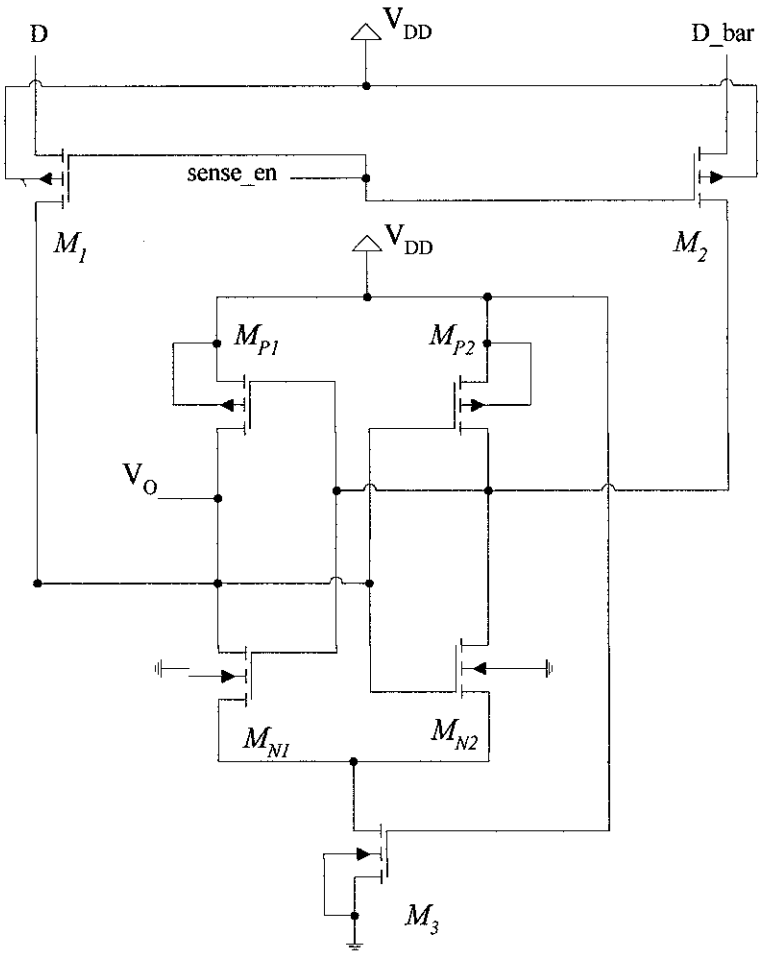

Figure 6 : Read Circuit Using Semi-latch Sense Amplifier

2.8 SRAM Circuit

The SRAM circuit is a combination between all circuits mention previously. It consists of four main parts which are pull-up circuit, basic memory cell, read and write circuit. The data bit line which is D and D_bar as in Figure 2 is connected to a pull-up circuit at the top part and to read circuit at the bottom part. The write circuit is a mux circuit that have two inputs which are data signal and write enable signal. The output of write circuit is connected to data bit line which is the D and D_bar line. The output of the SRAM circuit is taken from the output of the read circuit which is a semi-latch sense amplifier. Figure 7 shows the SRAM circuit used for simulation in this work.

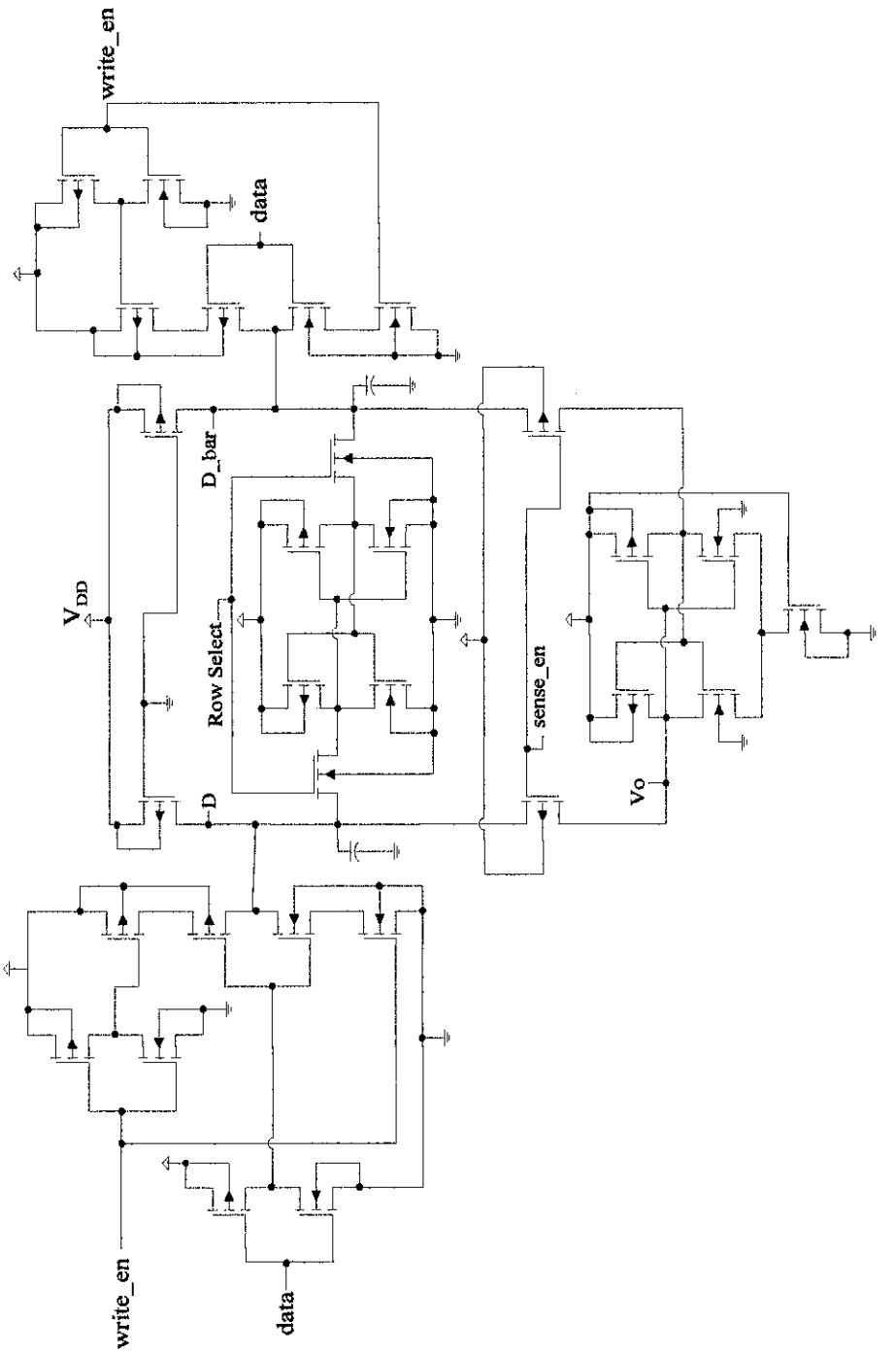

Figure 7 : SRAM Circuit

CHAPTER 3

METHODOLOGY

3.1 Procedure Identification

The schedule for this project is divided into two parts. Each part is set to be completed in one semester of study. The Gantt Chart can be seen at Appendix I for the first part and also at Appendix II for the second part. The project is carried out according to the process flow as shown in Figure 8. It is started with defining problems or issues related to SRAM performance. These problems are associated with parameters that will limit the performance of SRAM. After defining the parameters that affect SRAM stability and performance, research is conducted in collecting data needed for this project. Literature review and background study of SRAM were done in this phase so that this project is up to date with current issues of SRAM. Then, 1-bit basic memory cell circuit is designed by using Cadence software. The schematic comprises of one cell of SRAM with precharge, read and write circuit. When the design of SRAM is satisfied without errors, then simulation is carried out in the analog environment of Cadence software. Simulation is done by varying the magnitude of supplied voltage, V_{DD}, temperature and clock frequency, f_{CLK} signal. This procedure is later repeated by using different types of process technology that is available in Cadence software. If the simulation is not satisfactory, then more research will be done in updating the design of SRAM cell. All simulations are carried out after modification or correction was made at the schematic diagram. All the results that have been gathered during the simulation process will be analysed, compared and interpreted.

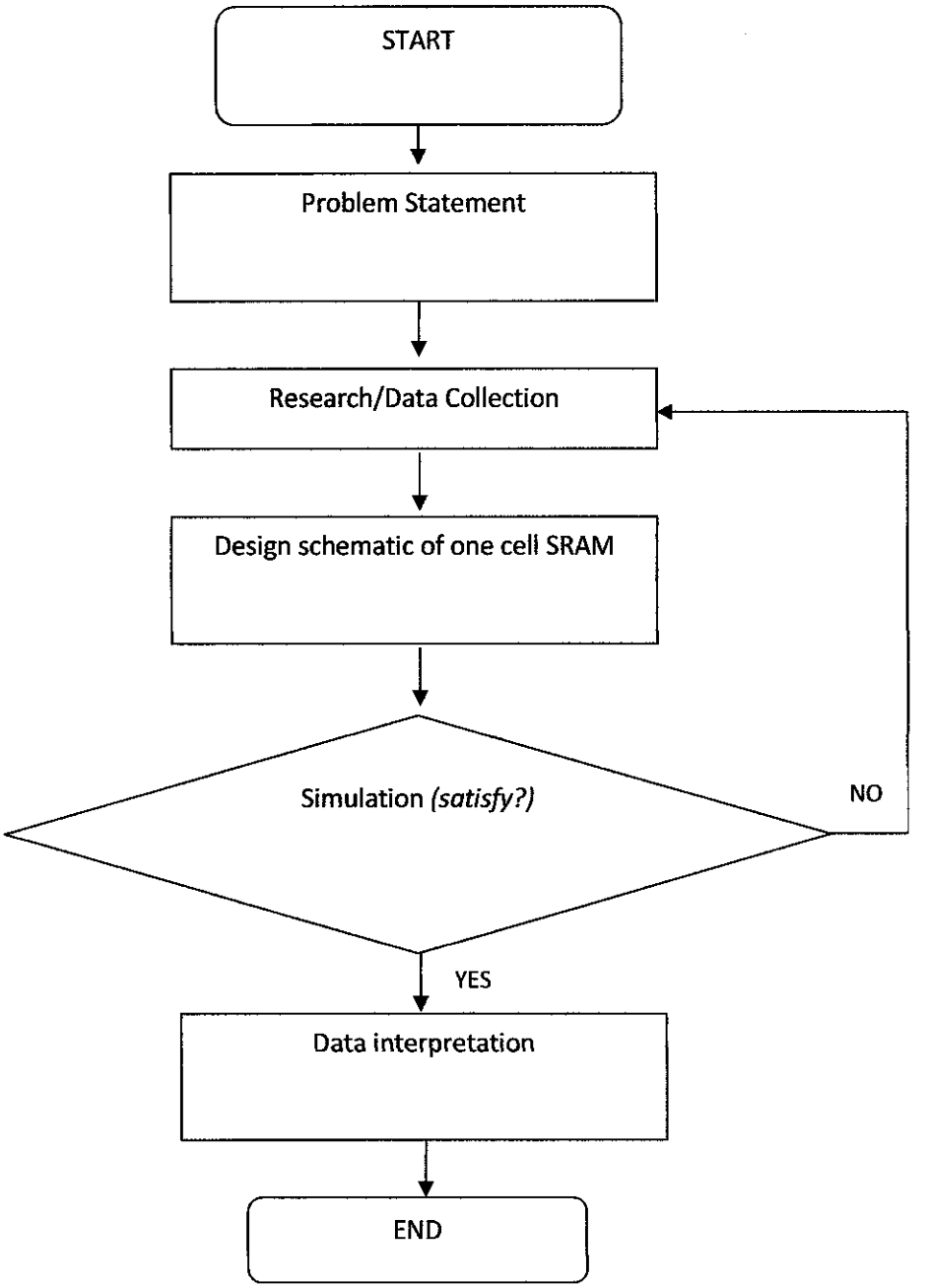

Figure 8 : Flow Diagram for Project Work

3.2 Tools and Equipment Used

The memory cell block is built by using six transistors whereby four of them is used as cross-coupled inverter that act as basic flip-flop and two more transistors will act as a pass transistor. The schematic of this memory cell will be simulated by various state or condition in analysing the performance of the memory cell.

All the parameters such as the magnitude of V_{DD}, temperature and clock frequency, f_{CLK} signal will be changed in order to verify the memory cell performance. The first design of memory cell is done by using ami16 technology. Optimization is carried out after the memory cell was designed. This will give some changes in the value of the transistor's width. Later, the memory cell is designed by using another process technology with different value of transistor channel length.

This circuit of analog type is quite complicated to be analysed and simulated, thus require different software to be used. One of the software used in microelectronic design is Cadence software as this software support all stages of IC design and verification

3.2.1 Cadence Software

This software is also compatible with different fabrication technologies used today. Cadence Composer Schematic Editor provides the schematic view while Cadence Affirma supports the simulation environment. Then, circuit layout can be created by using Virtuoso Layout Editor, while Diva software in Cadence will provide all the verification in layout design [13].

There are several process technologies available to be used with Cadence software which is ami06, ami16, tsmc35 and hp14tb. The number for each process name represents value of minimum channel length of transistor that can be used. Table 1 shows transistor's minimum length and width for different processes.

Table 1 : Minimum Length and Width of Transistor for Each Process Technology

Process Technology	Minimum Length of Transistor	Minimum Width of Transistor
ami06	0.6 μm	1.5 μm
ami16	1.6 μm	4.0 μm
tsmc35	0.4 μm	0.6 μm
hp14tb	0.6 μm	0.9 μm

CHAPTER 4

RESULT AND DISCUSSION

4.1 Clock Frequency and Voltage Supply Effect

In this study, the memory cell of SRAM is an asynchronous type which means that the cell performance is independent of clock signal. All operation of reading and writing can only be performed when the cell is being access by address decoder whereby memory cell is activated using column and row decoder. For the first part of this dissertation, simulation is done by using ami16 process at room temperature of 27°C. The SRAM circuit can be referred in Appendix III. Output circuit as shown previously in Figure 6 is only enabled when read signal is complimentary to write signal as cell memory cannot have write and read operation at the same time. There are two write circuit used as shown in Figure 4 and Figure 5 earlier to give the data bit lines to the memory cell. Both of these circuits have two inputs which are data and write signal. Therefore, two settings for input signals were used in this simulation as listed in Table 2. The edit properties box for these input signals can be referred in Appendix IV and Appendix V.

Table 2 : Setting for Input Signal

	Time Rise	Time Fall	Pulse Width	Pulse Period
t_1 (read/write signal)	1 ns	1 ns	$\frac{2}{2 \times f_{CLK}}$	$\frac{2}{f_{CLK}}$
t_2 (data signal)	1 ns	1 ns	$\frac{2}{f_{CLK}}$	$\frac{4}{f_{CLK}}$

As can be seen in Table 2, the pulse width and period for each input signal is in equation form. The value for both pulse width and period of each signal can be varied by changing the parameter of f_{CLK} (clock frequency) used in the simulation. Figure 9 and 10 shows the waveform for both input signal whereby the top waveform is t_1 (read/write signal) and the bottom waveform is t_2 (data signal). It can be seen that if the value for f_{CLK} is higher, the pulse width and period for input signal is shorter.

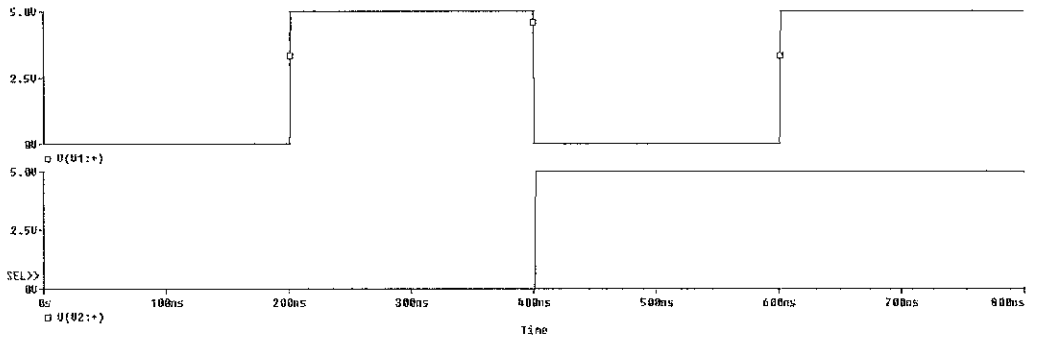

Figure 9 : Waveform of Input Signals for f_{CLK} = 5 MHz

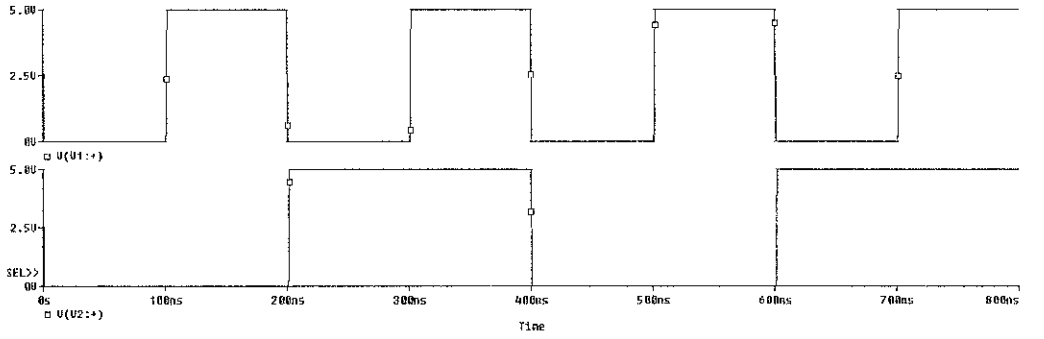

Figure 10 : Waveform of Input Signals for f_{CLK} = 10 MHz

The clock frequency is varied from low to high frequency to give longer and shorter pulse width of input signal to the circuit. The value of voltage supply is also varied throughout the simulation in order to find the limit value for voltage supply before memory cell start malfunction. For the first simulation, the clock frequency is set to 5 MHz. The simulation is started using a voltage supply of 5 V and the voltage is decreased by a step size of 0.1 V. The voltage limit is found by analyzing waveform produced at output circuit.

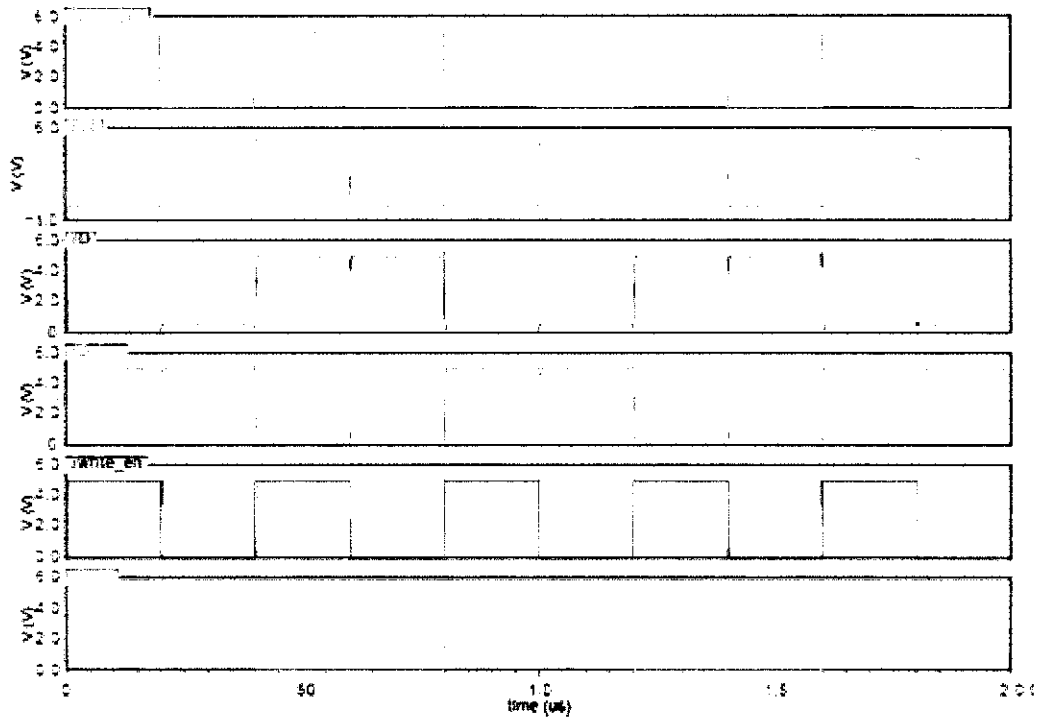

Figure 11 : Simulation for V_{DD} = 5 V with f_{CLK} = 5 MHz

Figure 11 shows the six timing diagrams as a result of simulation with voltage supply of 5 V. The first timing diagram, starting from the top most is sense enable signal (sense_en) while the second timing diagram is output signal (Vo) and the third timing diagram is data bit line of D_bar and D followed by write enable signal (write_en) and the last timing diagram is data signal. In this simulation, the SRAM circuit works as expected when it is supplied with maximum voltage of 5 V.

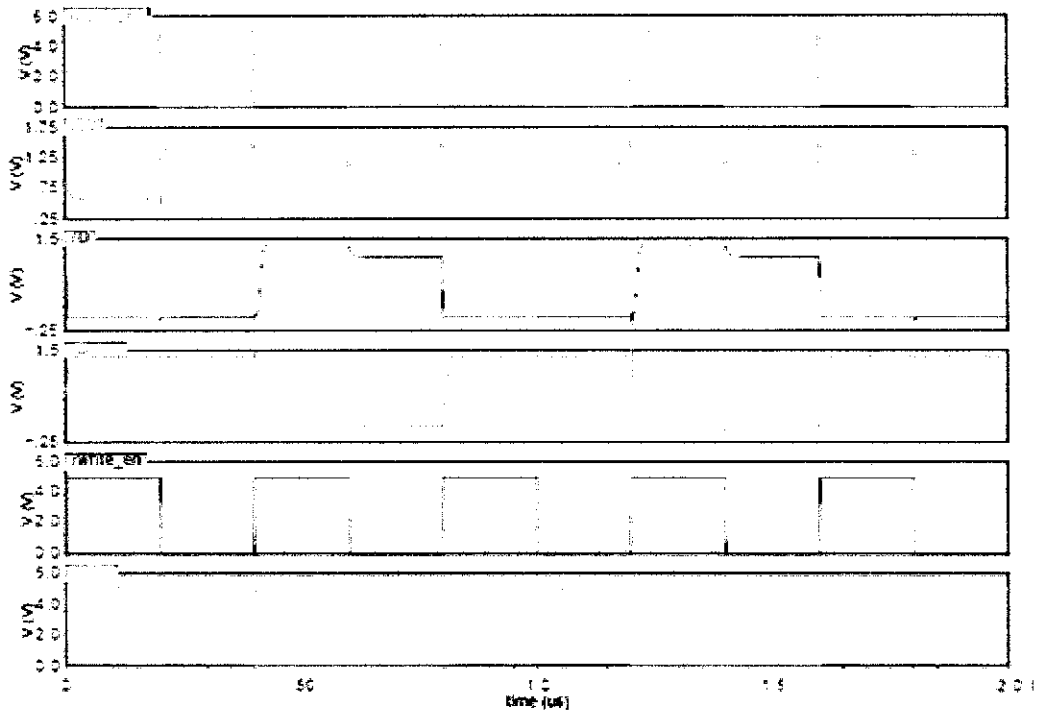

Figure 12 : Simulation for V_{DD} = 1.4 V with f_{CLK} = 5 MHz

Figure 12 shows the result of simulation using a V_{DD} = 1.4 V. The timing diagram of the six signal is sense enable signal, output signal, data bit line, write enable signal, and data signal respectively. In this simulation, the output signal is distorted and both state 0 and state 1 cannot be differentiated clearly between them. The NMOS transistor speed is too slow which resulted in failure to the read circuit which uses a sense amplifier concept. Therefore, for clock frequency of 5 MHz, the minimum voltage can be supplied to SRAM circuit is 1.5 V.

Another simulation is also done regarding the clock frequency and voltage supply effect but with different setup for the input signals as different values of clock frequency was used. Exactly the same as previous simulation, the schematic is simulated by using ami16 process technology at room temperature of 27°C. For this simulation, the clock frequency is set to 10 MHz. Simulation is start at 5 V and reduced by step size of 0.1 V until the limit for voltage supply is reached.

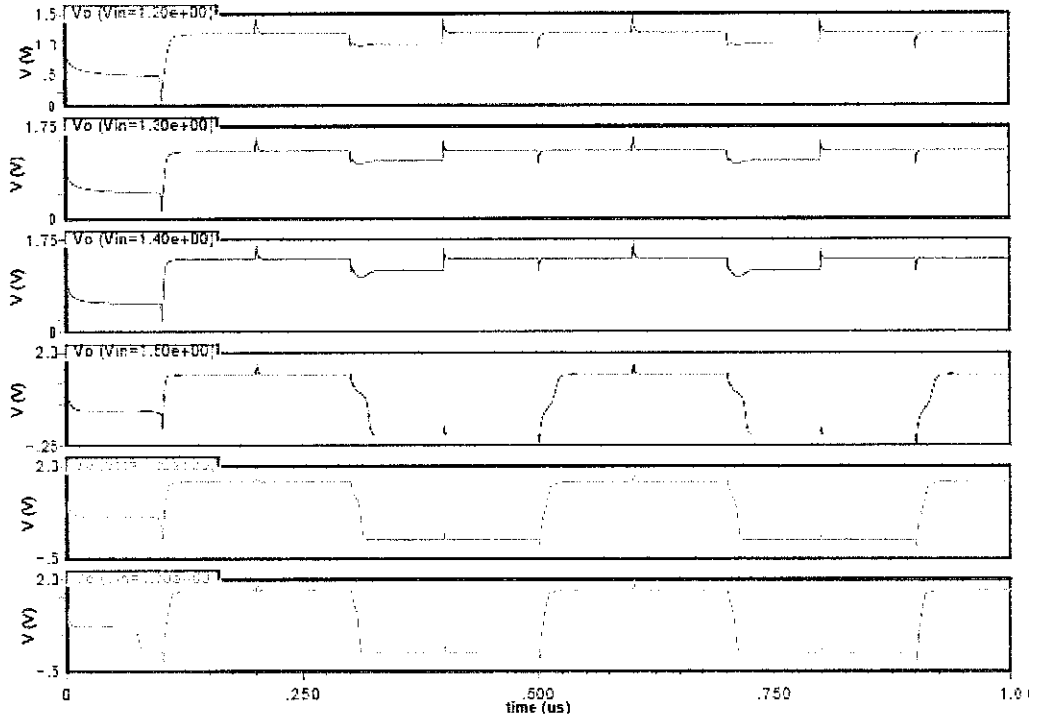

Figure 13 : Simulation for Output Signal with Clock Frequency of 10 MHz

Figure 13 shows the six timing diagrams of output signal, Vo as a result of simulation with different voltage supply starting from 1.2 V until 1.7 V. It can be seen that the output signal begins to disoriented from the third timing diagram that shows output signal (Vo) with voltage supply of 1.4 V. For the disoriented output signal, both state 1 and state 0 cannot be distinguished clearly. Therefore, for clock frequency setting of 10 MHz, the minimum supplied voltage is 1.5 V. Table 3 shows the result of simulation with different clock frequency setting with the respective supplied voltage limit.

Table 3 : Simulation Result with Different Clock Frequency Setting

Clock Frequency, MHz	5	10	20	100	200	300
Supplied Voltage Limit, V	1.5	1.5	1.5	1.8	2.4	3.1

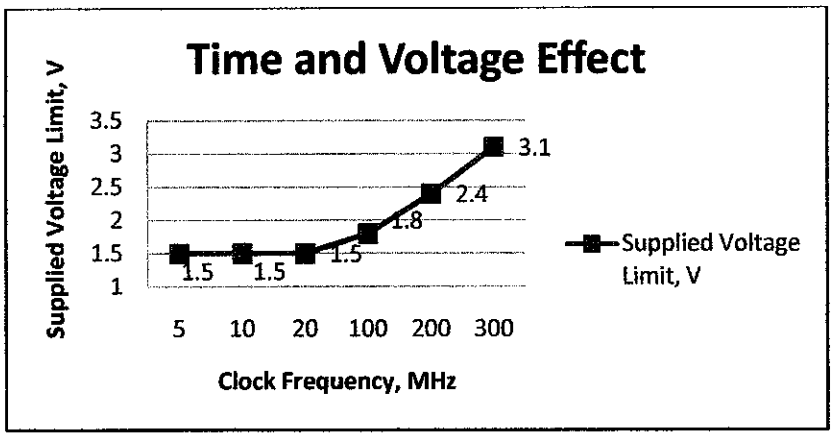

Figure 14 : Simulation Using ami16 Process Technology for Clock Frequency and Voltage Supply Effect

Figure 14 summarizes the clock frequency and voltage supply effect simulation using ami16 process. As the clock frequency is reduced, the supplied voltage limit also reduced. This is because the total gate charge needs longer time to be charged when circuit is using lower voltage supply. As shown in Figure 15, total gate charge consists of parasitic capacitances internal to the device. Moreover, Miller effect capacitance from drain to gate also needs to be taken into consideration. Gate charge is very important specification as the switching of MOSFET depends on the necessary amount of charge at the gate device.

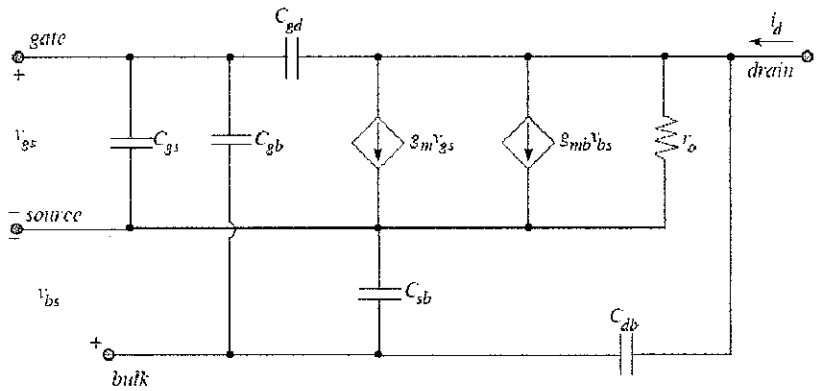

Figure 15 : MOSFET Small Signal Model [14]

Furthermore, when supplied voltage is reduced, the clock frequency or speed also reduced as shown in Eq. (1) below which comes from the sub-micron CMOS design [15]:

$$f_{max} \propto \frac{V-V_t}{V} \quad (1)$$

In the Eq. (1) above, f_{max} is the maximum clock frequency in circuit operation and V is the supplied voltage and V_t is the threshold voltage. In Dynamic Voltage and Frequency Scaling (DVFS) system, the controller will select the lowest voltage supply suitable for the desired clock frequency that is sufficient in completing the workload on schedule without overheating circuit. Hence, this work provides information needed for DVFS [16].

4.2 Temperature Effect

In the temperature effect study, the memory cell performance is independent of clock signal as all operation towards cell can only be performed when the cell is being accessed by address decoder using column and row intersection. All simulations are done by using ami16 process. There are two manipulator parameters considered which are clock frequency and supplied voltage. In the first simulation, the clock frequency is set to 20 MHz. The voltage supply is set at 5 V.

The temperature is varied throughout the simulation in order to find the effective range of temperature before the circuit fails to operate. Figure 16 shows the result of simulation for temperature at -229°C which consists of four timing diagram (sense enable, output signal, bit line signal, write and data signal). It can be seen that the output signal is a smooth waveform with a clear distinguishable state 1 and state 0.

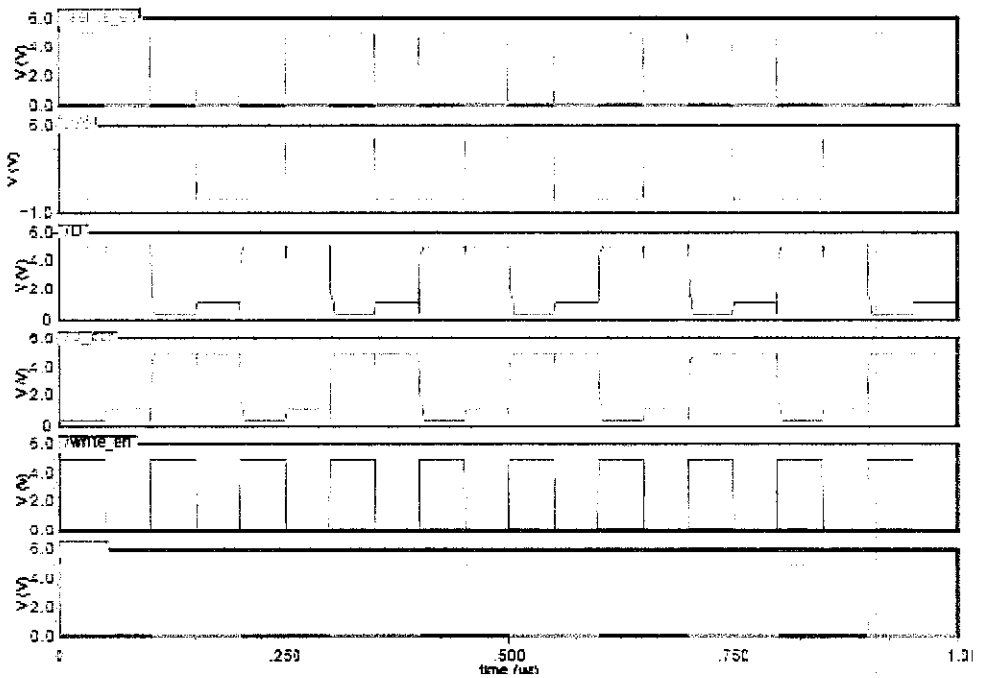

Figure 16 : Simulation for Temperature of -229°C with V_{DD} 5 V and f_{CLK} = 20 MHz

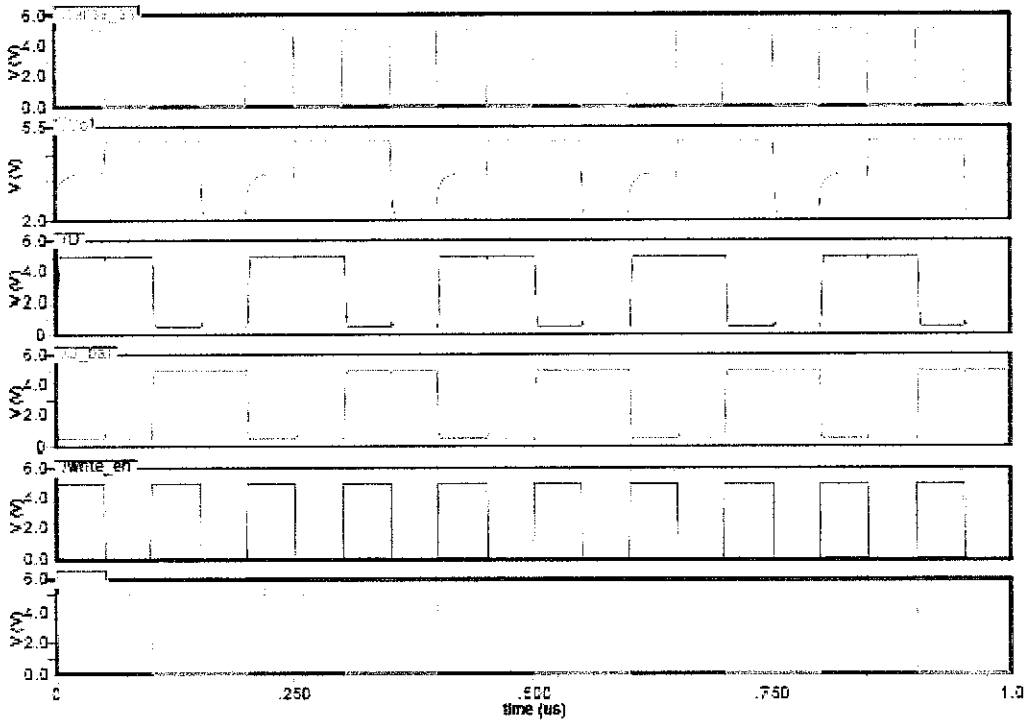

Figure 17 : Simulation for Temperature of 291°C with V_{DD} 5 V and f_{CLK} = 20 MHz

Figure 17 shows the six timing diagrams obtained from the simulation at temperature set to 291°C which are the sense enable, output signal, bit line signal, write and data signal respectively. As shown in Figure 16, the circuit output is not at the right state of the input data. Hence, the highest possible temperature that this circuit can withstand is at 290°C. If the circuit to operate at temperature more than 290°C, then the SRAM will not be able to perform properly.

The simulation is carried out again using the same clock frequency but the supplied voltage is set to 1.5 V. The temperature is varied throughout the simulation in order to find the limit for surrounding temperature before memory cell fail to operate. The simulation temperature is set to -250°C and step size is increased by 1°C. The simulation results are given in Appendix VI and Appendix VII.

Table 4 shows that voltage supply does influence the effective range temperature for memory cell to function properly. It can be seen that for clock frequency of 20 MHz, the circuit can only withstand temperature up to 243°C when the circuit is supplied with 1.5 V. This is the minimum voltage for the circuit to operate properly. However, when circuit is supplied with 5 V, the range of operating temperature becomes wider by 47 degree.

Table 4 : Effective Range Temperature for Different Supplied Voltage with Clock Frequency of 20 MHz

Supplied Voltage, V	Effective Range Temperature, °C
5	-229 to 290
1.5	-250 to 243

Another simulation is carried out to observe this temperature effect case when the input signal of both data and read signal are changed to shorter pulse width signal. In this simulation, the clock frequency is set to 100 MHz. The voltage supply is set to 5 V and later at minimum voltage supply of 1.8 V. The temperature is varied throughout the simulation in order to find the limit for surrounding temperature before the circuit fails to operate. All results obtained in the simulations are given in Appendix VIII to Appendix XI. Table 5 shows the summarized of the results obtained in the simulation.

Table 5 : Effective Range Temperature for Different Supplied Voltage with Clock Frequency of 100MHz

Supplied Voltage, V	Effective Range Temperature, °C
5	-229 to 290
1.8	-250 to 57

Table 6 shows the difference in clock frequency setting and voltage supply will influence the effective range temperature for circuit. In can be concluded that the lower the supplied voltage, the effective range of temperature become smaller. It means that the circuit cannot tolerate high temperature environment for its operation. This is because device characteristic of MOSFET is affected by temperature variations thus circuit performance will vary for different temperature that the circuit is exposed to [17]. The fluctuation of temperature in a circuit will also change the device parameters. The parameters are threshold voltage, carrier mobility and saturation velocity [18].

As temperature is increased, the gate overdrive will also increase while the carrier mobility will decreased. The relation of this temperature and carrier mobility can be approximated as in Eq. (2) [16]

$$\mu(T) = \mu(T_r)\left(\frac{T}{T_r}\right)^{-k_\mu} \tag{2}$$

whereby T is the value of absolute temperature, T_r is the value of room temperature and k_μ is the value for fitting parameter which is usually about 1.5. Moreover, saturation voltage is inversely proportional to temperature. Hence, as temperature is increase, saturation voltage will decrease. With the increasing of temperature, threshold voltage magnitude will decrease almost in linear relationship and the approximation is shown in Eq. (3) [16].

$$V_t(T) = V_t(T_r) - k_{vt}(T - T_r) \tag{3}$$

whereby the value for k_{vt} is around 1-2 mV/K. All these decreasing values will in turn reduce the speed of memory cell alongside the drain current.

Table 6 : Effective Range Temperature for Different Supplied Voltage Using ami16 Process

Clock Frequency	Voltage Supply, V	Effective Range Temperature, °C
20MHz	5	-229 to 290
	1.5	-250 to 243
100MHz	5	-229 to 290
	1.8	-250 to 57

4.3 Process Technology Effect

There are several types of different process technologies available to be used with Cadence software. For example, there are process technology called ami06, ami16, tsmc35 and hp14tb. Different process technologies will have different minimum width and length for transistor. In the process technology effect case, all simulations are done by using several process technologies for temperature, clock frequency and voltage supply effects. All simulation results for clock frequency and voltage supply effect based on several process technologies are given in Appendix XII to Appendix XVII. Table 7 shows minimum supplied voltage with different clock frequency setting for four different process technologies.

Table 7 : Minimum Supplied Voltage with Different Clock Frequency Setting for Different Process Technologies

Clock Frequency	Process Technology			
	ami06	ami16	tsmc35	hp14tb
5 MHz	1.0 V	1.5 V	1.25 V	0.83 V
10 MHz	1.0 V	1.5 V	1.25 V	0.86 V
20 MHz	1.0 V	1.5 V	1.25 V	0.91 V
100 MHz	1.3 V	1.8 V	1.25 V	1.11 V
200 MHz	1.4 V	2.4 V	1.30 V	1.31 V
300 MHz	1.6 V	3.1 V	1.43 V	1.47 V

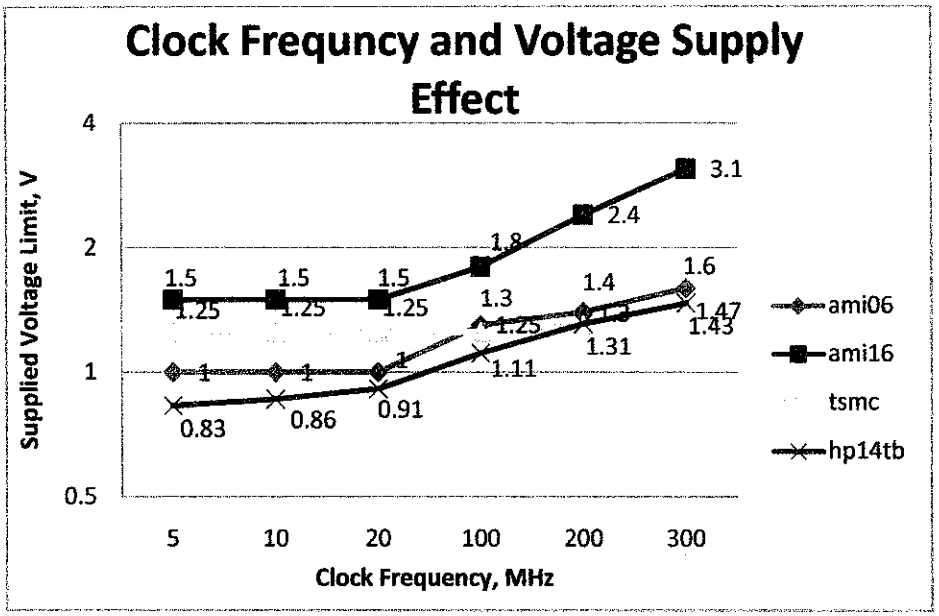

Figure 18 : Simulation using Different Process Technologies for Clock Frequency and Voltage Supply Effect

Figure 18 shows the result of simulations that were carried out using different process technologies. For all seven types of clock frequency setting used, all output voltage decrease when supplied voltage is reduced. Moreover, the results for the clock frequency and voltage supply effect for all process technologies have similar pattern whereby if lower clock frequency is used, the value of the voltage supply limitation to the circuit will be lowered. This is because of the equations in the sub-micron CMOS design whereby a decline in voltage will resulted in a decrease of frequency [15]. Note that, different process technology will have different supply voltage limit. This is because the threshold voltage, carrier mobility and channel length are different in every process. The list of the device parameters are shown in the Table 8.

Table 8 : Device Parameter Value in Different Process Technology

		ami06	ami16	tsmc35	hp14tb
NMOS	Threshold Voltage, *Vt*	0.7086 V	0.5815607 V	0.4964448 V	0.6558651 V
	Carrier Mobility, μ	533.6953445 $cm^2/V.s$	640.0382895 $cm^2/V.s$	444.9381976 $cm^2/V.s$	445.0609817 $cm^2/V.s$
	Channel length	1.7E17 cm	7.5E16 cm	1.7E17 cm	1.7E17 cm
PMOS	Threshold Voltage, *Vt*	- 0.9179952 V	- 0.8058627 V	-0.6636594 V	-0.8131136 V
	Carrier Mobility, μ	202.4540953 $cm^2/V.s$	268.4532224 $cm^2/V.s$	151.3305606 $cm^2/V.s$	168.0565267 $cm^2/V.s$
	Channel length	1.7E17 cm	2.4E16 cm	1.7E17 cm	1.7E17 cm

The circuit is also simulated for the temperature effect by using different process technologies. All simulation results for temperature effect based on several process technologies are given in Appendix XVIII to Appendix XXXIII. Table 9 shows the different setting of clock frequency gives different range of effective temperature that is also influenced by the supplied voltage and process technology used to the circuit. This happened due to the device parameters are different for each process technology. As shown in Table 8, the carrier mobility in ami06 process is higher compared to tsmc35 process which makes the circuit with process technology ami06 has a wider effective range of temperature. As temperature is increased, the gate overdrive voltage will increase while carrier mobility will decrease. Thus, the speed of circuit is slower.

Table 9 : Effective Range Temperature for Different Supplied Voltage by using Different Process Technologies

	Clock Frequency	Voltage Supply, V	Effective Range Temperature, °C
ami16	20MHz	5	-229 to 290
		1.5	-250 to 243
	100MHz	5	-229 to 290
		1.8	-250 to 57
ami06	20MHz	5	-250 to 294
		1.00	-198 to 197
	100MHz	5	-250 to 294
		1.30	--250 to 224
tsmc35	20MHz	5	-250 to 305
		1.25	-240 to 170
	100MHz	5	-250 to 305
		1.25	-230 to 121
hp14tb	20MHz	5	-250 to 270
		0.91	-117 to 58
	100MHz	5	-250 to 265
		1.11	-250 to 35

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

In conclusion, the output voltage will drop whenever the supplied voltage into the memory cell is reduced. For lower frequency of input signal, the minimum supplied voltage before the circuit begins to malfunction is lower compared to higher frequency of input signal. This is due to the parasitic capacitances of the transistor itself needs time for the charging and discharging processes when data is written into the memory cell. With the same clock frequency setting, as voltage supply is reduced, effective range temperature also reduced. This is because as voltage is reduced, the gate overdrive will increase while carrier mobility will decrease. When temperature is increased, this in turn lowers the write/read process of memory cell. Different process technologies have different values for device parameters. The performance of cell memory is affected when the voltage supply, temperature and clock frequency are changed. Different process technology will have different supply voltage limit. This is because the threshold voltage, carrier mobility, channel length and width of transistor are different in every process. As temperature is increased, the circuit becomes more unstable due to using different types of process technology.

5.2 Recommendations

For this project, it is recommended to further study on performance of memory cell with different topologies to enhance cell performance. It is also recommended that this project is taken to the next step which is the layout circuit. Simulation can also be done by using nano technology as comparison to the latest technology.

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APPENDIX I

Gantt Chart FYP I

Agenda\week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	20
Title Selection - Performance Study Based on Process Technologies of 1Bit Static RAM																
Meeting with Supervisor																
Research on SRAM																
Learn Cadence Software																
Simulate Schematic of Basic Memory Cell																
Preparing Preliminary Report																
Preliminary Report Submission																
Simulate Schematic Based on Several Conditions – voltage supply, temperature and clock frequency (using ami16)																
Analyse Simulation Schematic Based on Several Conditions - voltage supply, temperature and clock frequency (using ami16)																
Preparing Progress Report																
Progress Report Submission																
Seminar																
Simulate Schematic Based on Several Conditions - voltage supply, temperature and clock frequency but with the use of different process technology (ami06)																

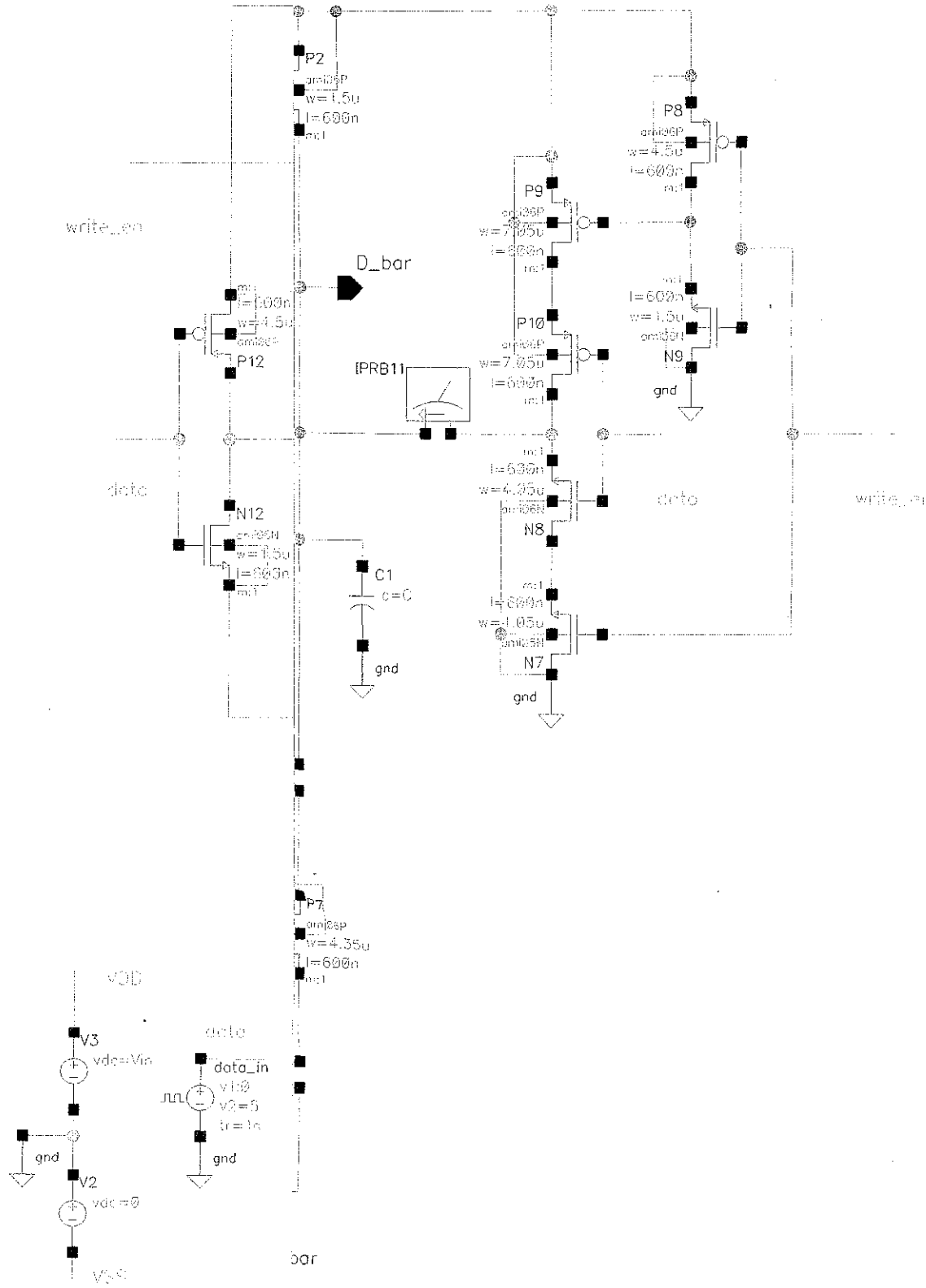
Analyse Simulation Schematic Based on Several Conditions - voltage supply, temperature and clock frequency but with the use of different process technology (ami06)																
Preparing Draft Report																
Draft Report Submission																
Compare Simulation 2 Different Process – ami16 and ami06																
Preparing Interim Report																
Interim Report Submission																
Oral Presentation																

APPENDIX II

Gantt Chart FYP II

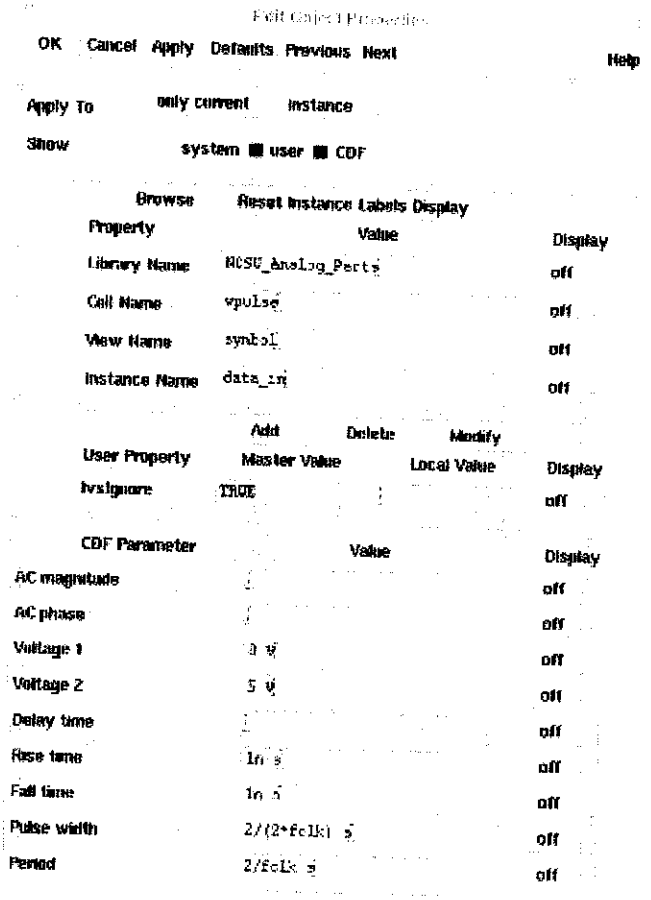
Agenda\week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	17
Optimize SRAM circuit																
Simulate Schematic Based on Several Conditions - voltage supply, temperature and clock frequency (using ami06 and ami16)																
Analyse Simulation Schematic Based on Several Conditions - voltage supply, temperature and clock frequency (using ami06 and ami16)																
Preparing Progress Report																
Progress Report Submission																
Simulate Schematic Based on Several Conditions - voltage supply, temperature and clock frequency (using tsmc35 and hp14tb)																
Analyse Simulation Schematic Based on Several Conditions - voltage supply, temperature and clock frequency (using tsmc35 and hp14tb)																
Compare Simulation 4 Different Process – ami06, ami16, tsmc35 and hp14tb																
Preparing Draft Report																
Draft Report Submission																
Preparing Final Report and Technical Paper																
Final Report (Soft Cover) and Technical Paper Submission																
Oral Presentation																
Final Report (Hard Cover) Submission																

Schematic for F



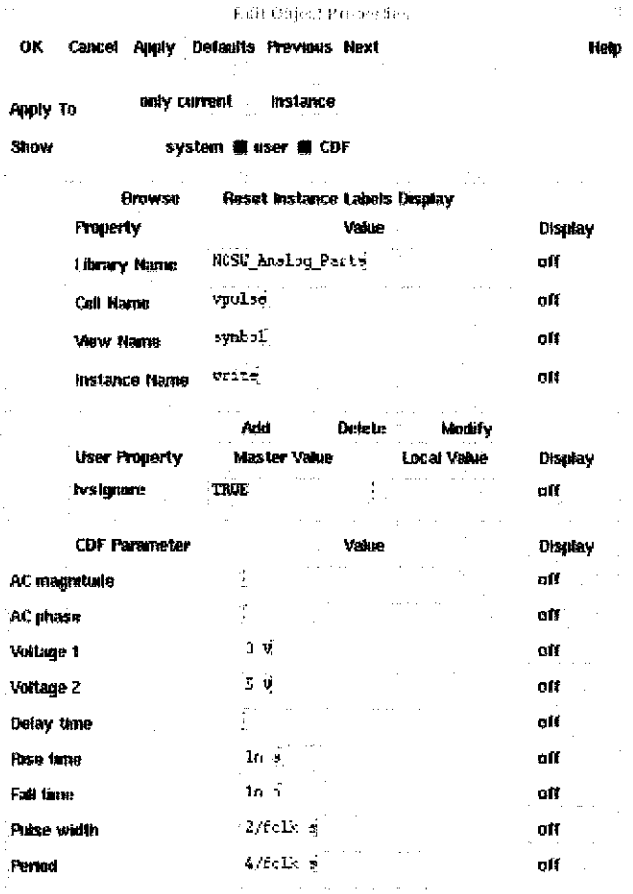
APPENDIX IV

Read/Write Signal Properties



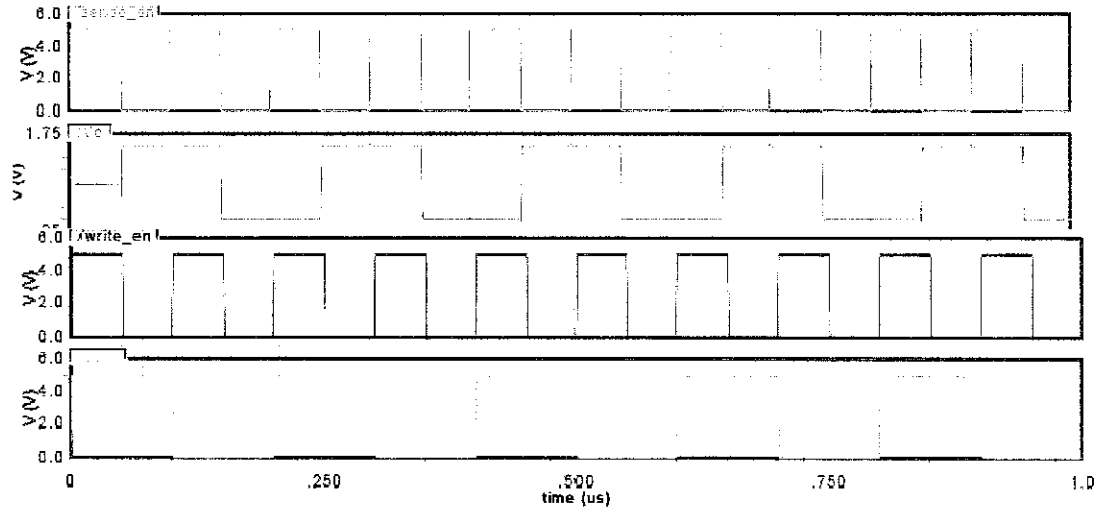
APPENDIX V

Data Signal Properties



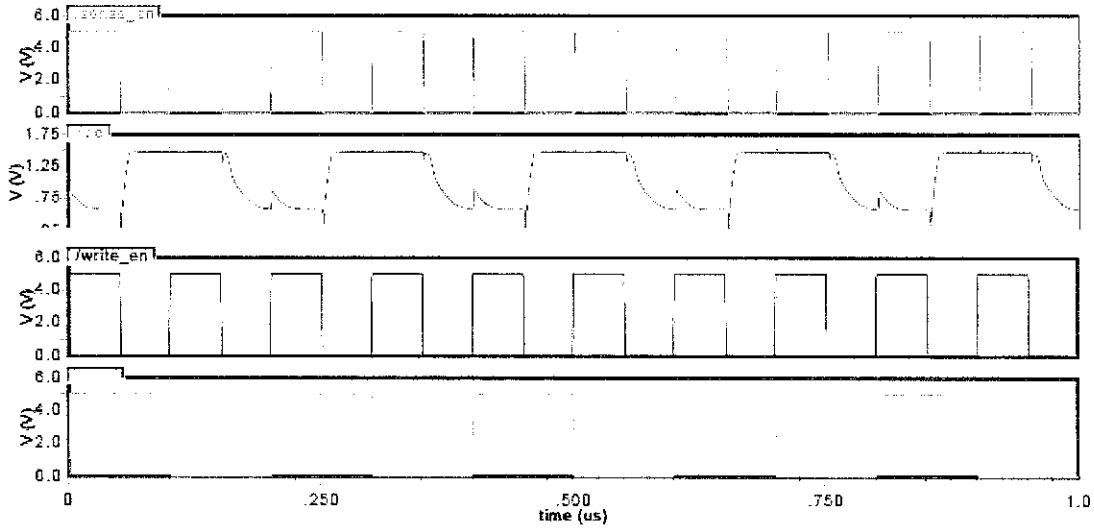
APPENDIX VI

Simulation for Temperature of -250°C with V_{DD} = 1.5 V and f_{CLK} = 20 MHz by Using ami16 Process



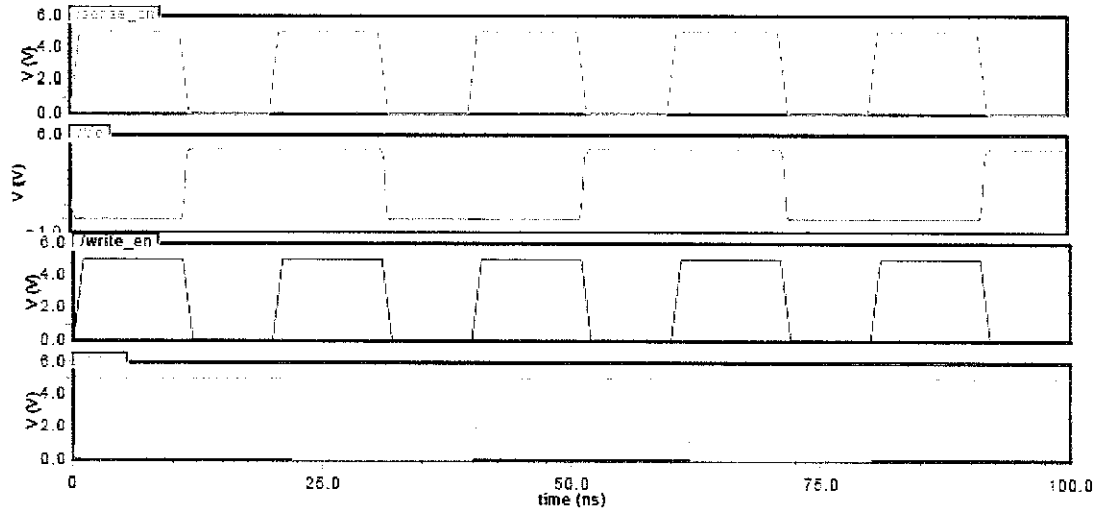
APPENDIX VII

Simulation for Temperature of 243°C with V_{DD} = 1.5 V and f_{CLK} = 20 MHz by Using ami16 Process



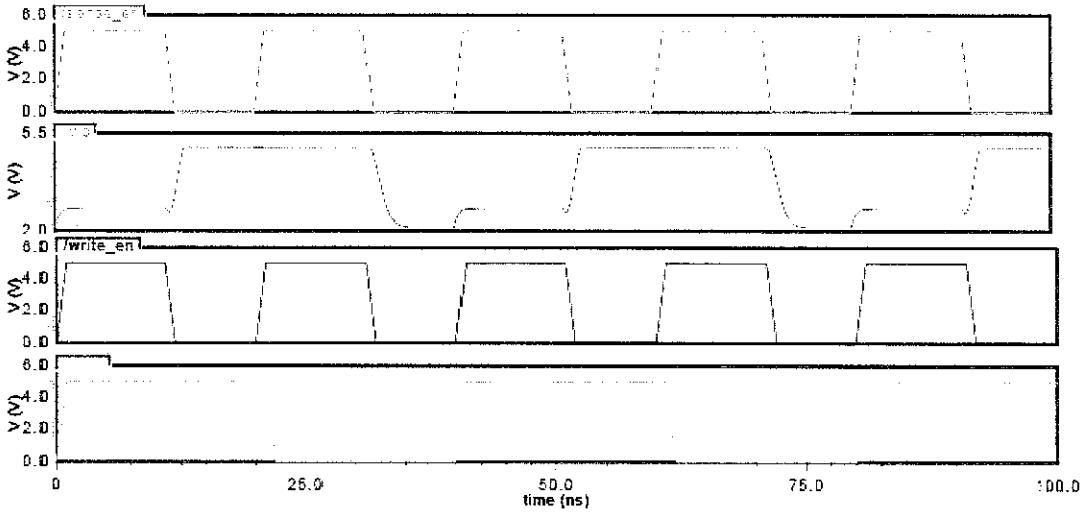
APPENDIX VIII

Simulation for Temperature of -229°C with V_{DD} = 5 V and f_{CLK} = 100 MHz by Using ami16 Process



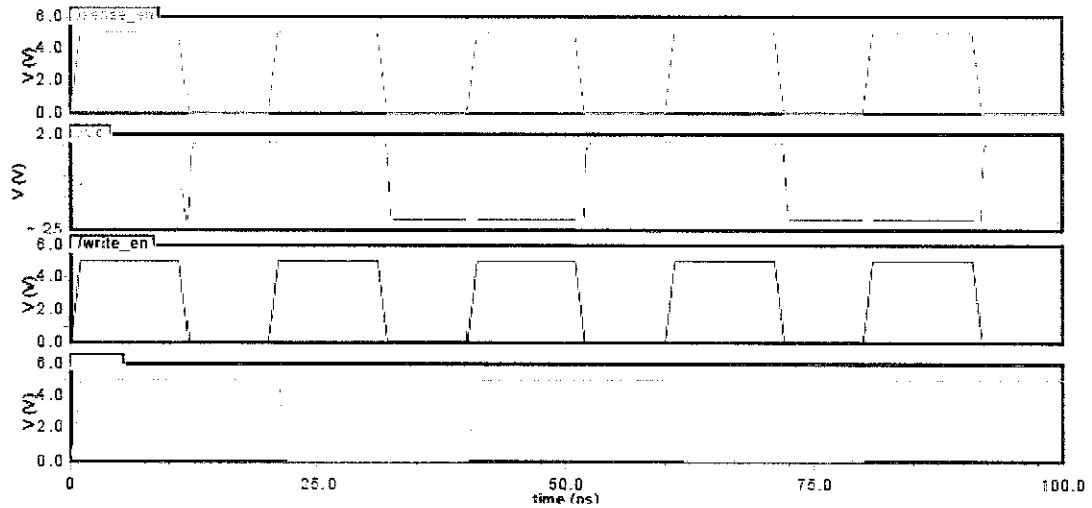
APPENDIX IX

Simulation for Temperature of 290°C with V_{DD} = 5 V and f_{CLK} = 100 MHz by Using ami16 Process



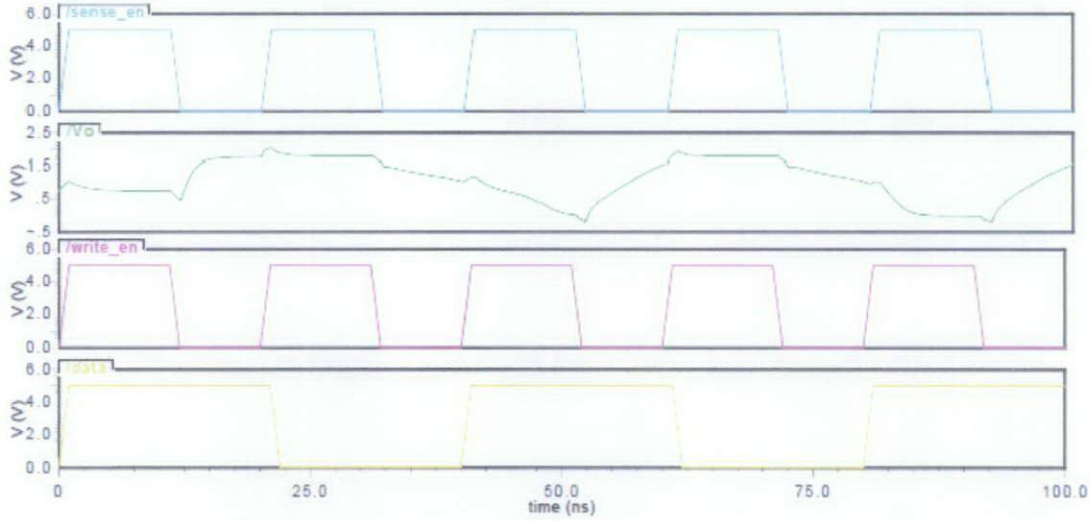
APPENDIX X

Simulation for Temperature of -250°C with V_{DD} = 1.8 V and f_{CLK} = 100 MHz by Using ami16 Process



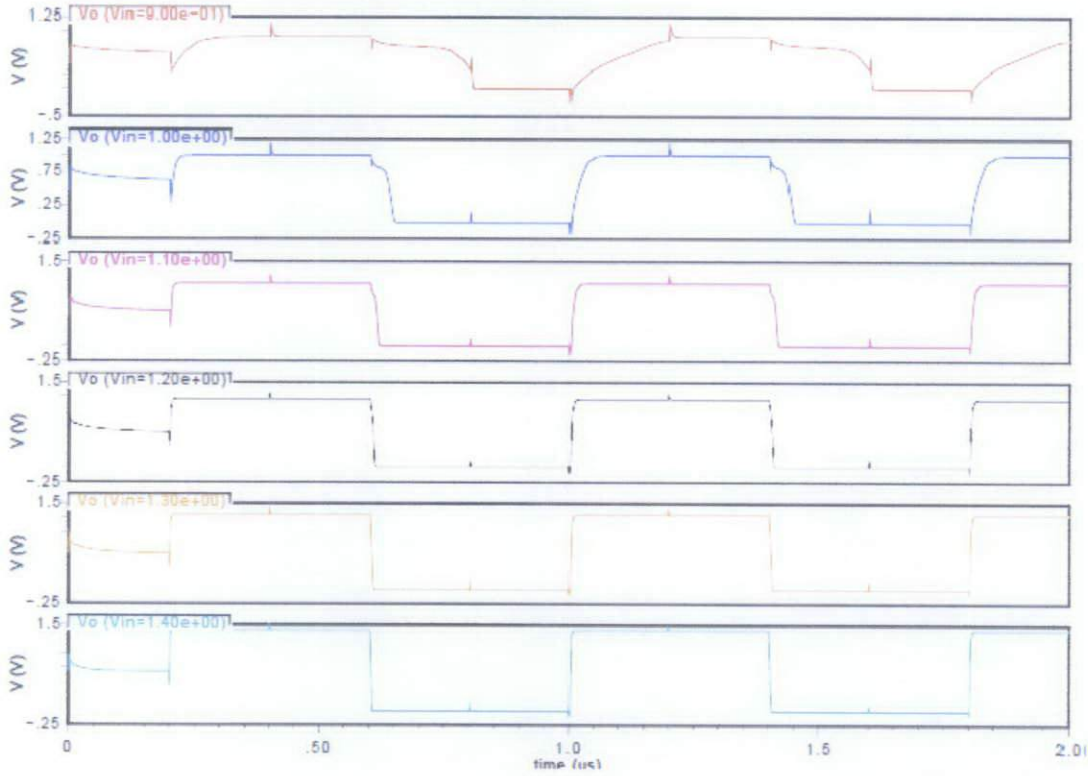
APPENDIX XI

Simulation for Temperature of 57°C with V_{DD} = 1.8 V and f_{CLK} = 100 MHz by Using ami16 Process



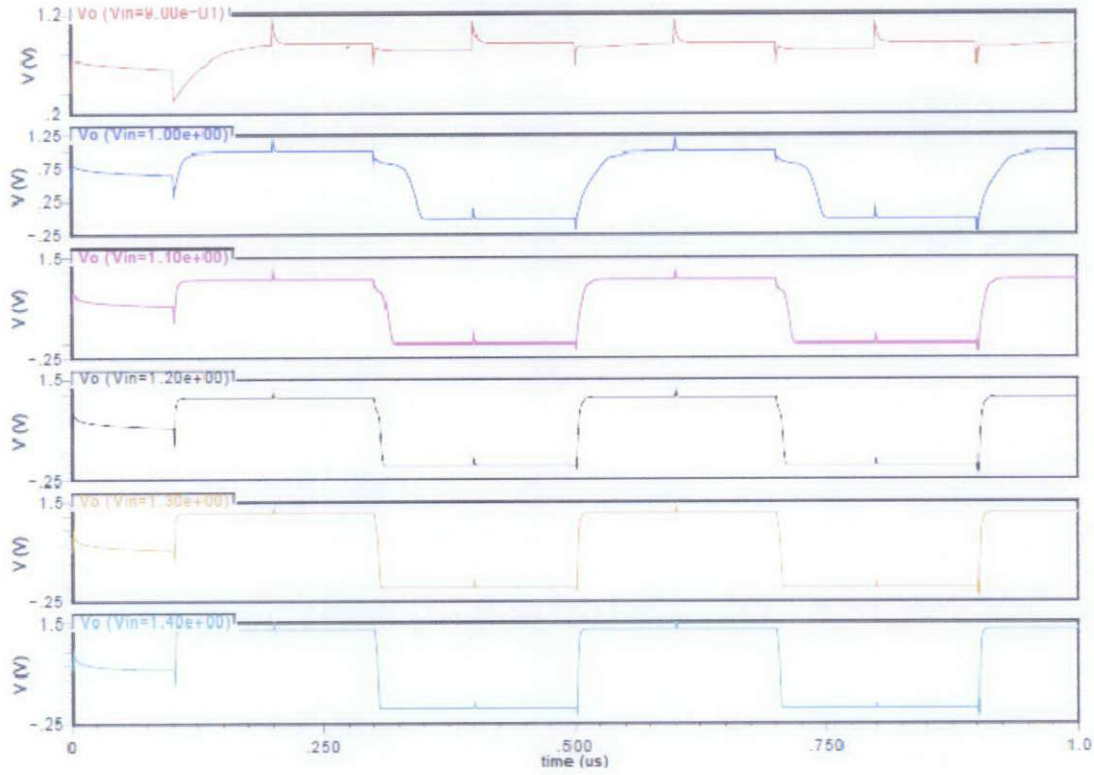
APPENDIX XII

Simulation for Temperature of 27°C with f_{CLK} = 5 MHz by Using ami06 Process



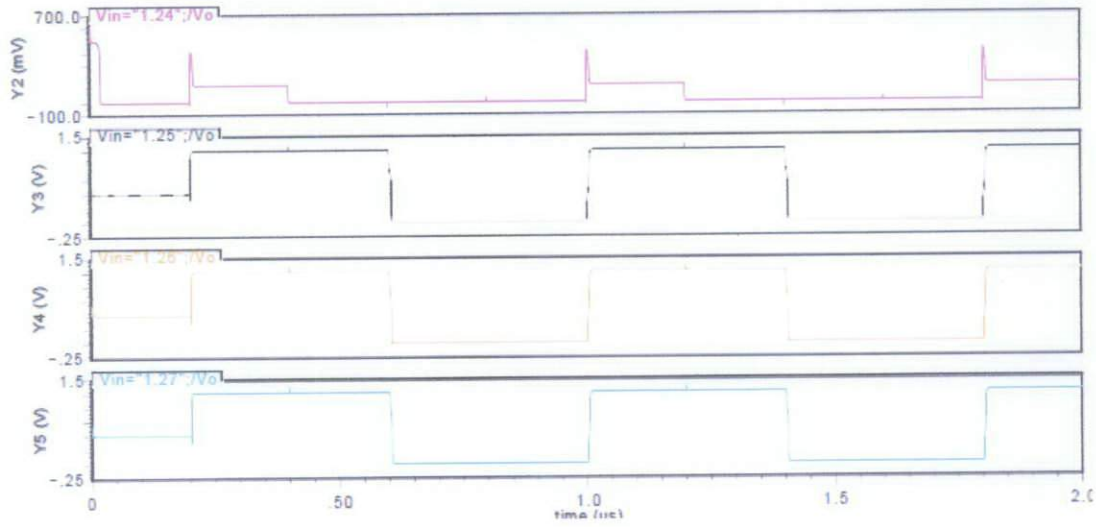
APPENDIX XIII

Simulation for Temperature of 27°C with f_{CLK} = 10 MHz by Using ami06 Process



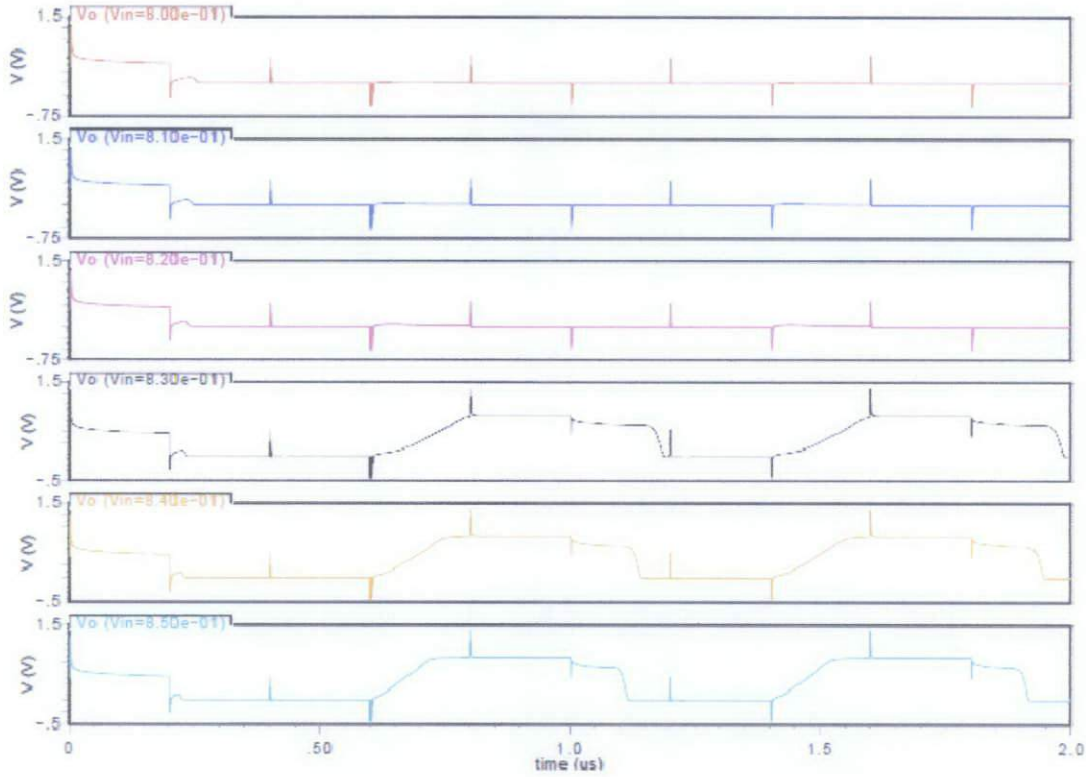
APPENDIX XIV

Simulation for Temperature of 27°C with f_{CLK} = 5 MHz by Using tsmc35 Process



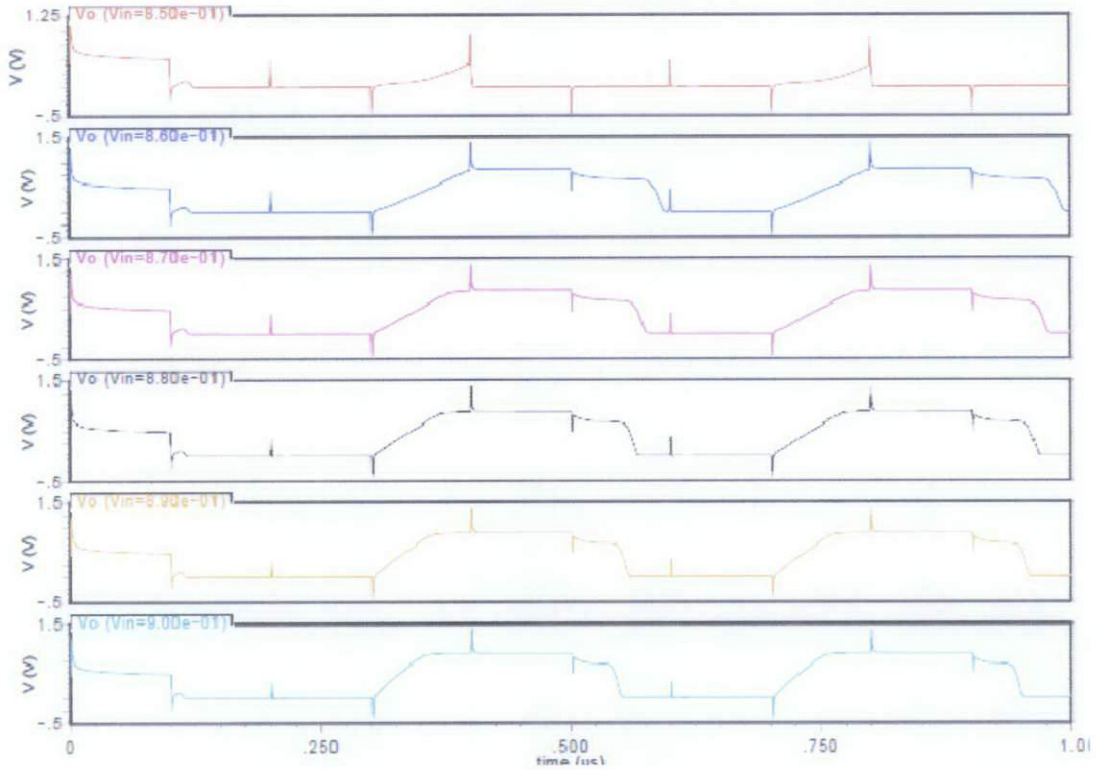
APPENDIX XVI

Simulation for Temperature of 27°C with f_{CLK} = 5 MHz by Using hp14tb Process



APPENDIX XVII

Simulation for Temperature of 27°C with f_{CLK} = 10 MHz by Using hp14tb Process



APPENDIX XVIII

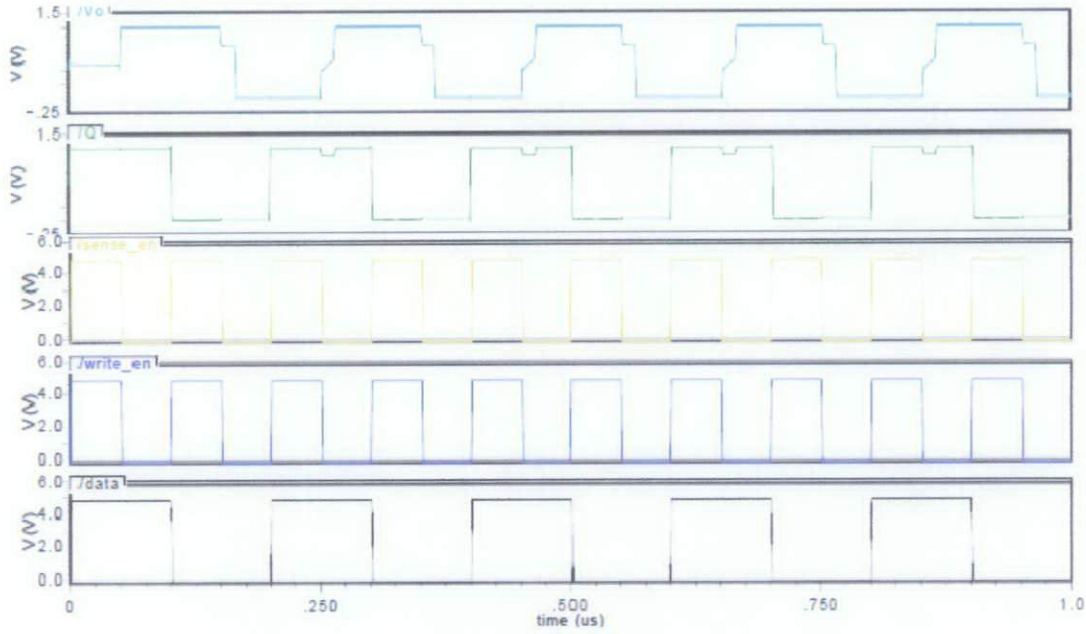
Simulation for Temperature of -250°C with V_{DD} = 5 V and f_{CLK} = 20 MHz by Using tsmc35 Process

APPENDIX XIX

Simulation for Temperature of 305°C with V_{DD} = 5 V and f_{CLK} = 20 MHz by Using tsmc35 Process

APPENDIX XX

Simulation for Temperature of -240°C with V_{DD} = 1.25 V and f_{CLK} = 20 MHz by Using tsmc35 Process

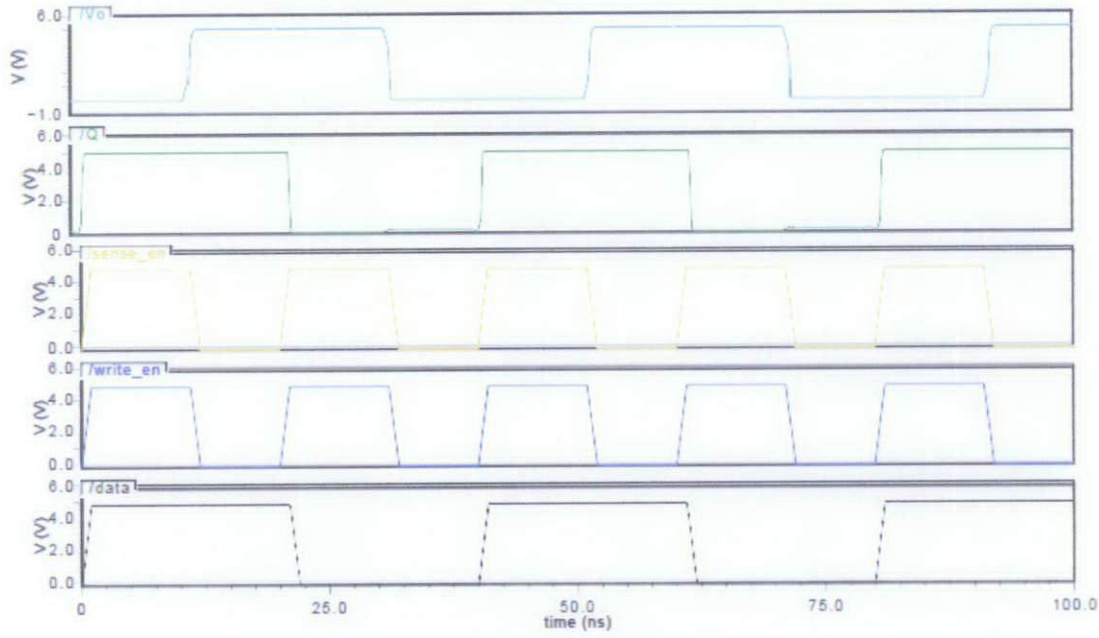


APPENDIX XXI

Simulation for Temperature of 170°C with V_{DD} = 1.25 V and f_{CLK} = 20 MHz by Using tsmc35 Process

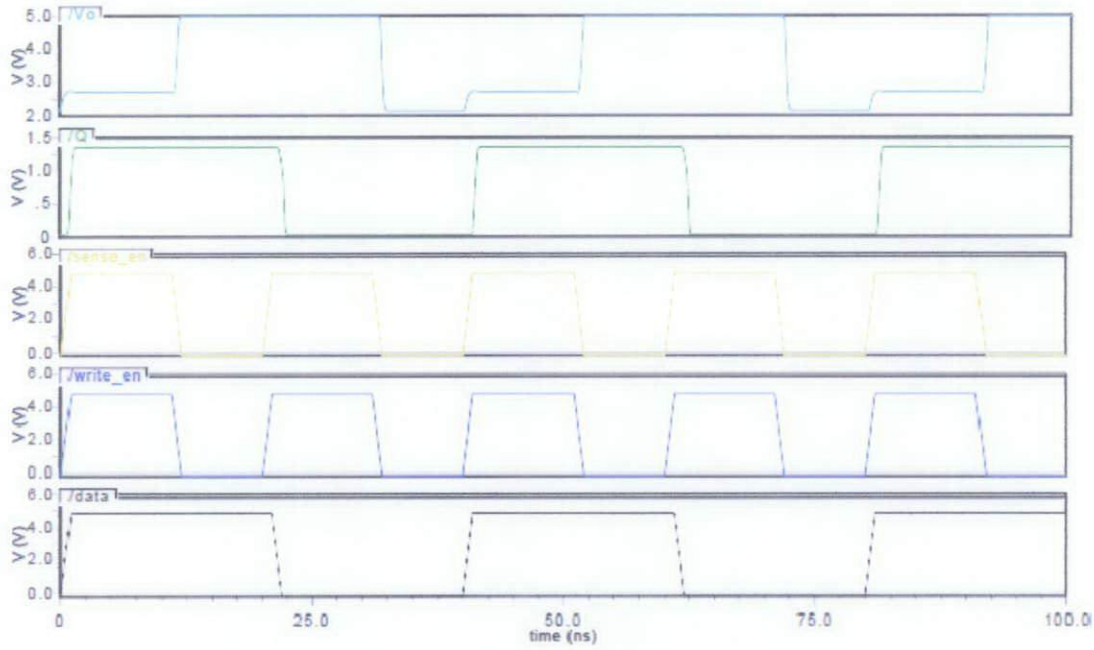
APPENDIX XXII

Simulation for Temperature of -250°C with V_{DD} = 5 V and f_{CLK} = 100 MHz by Using tsmc35 Process



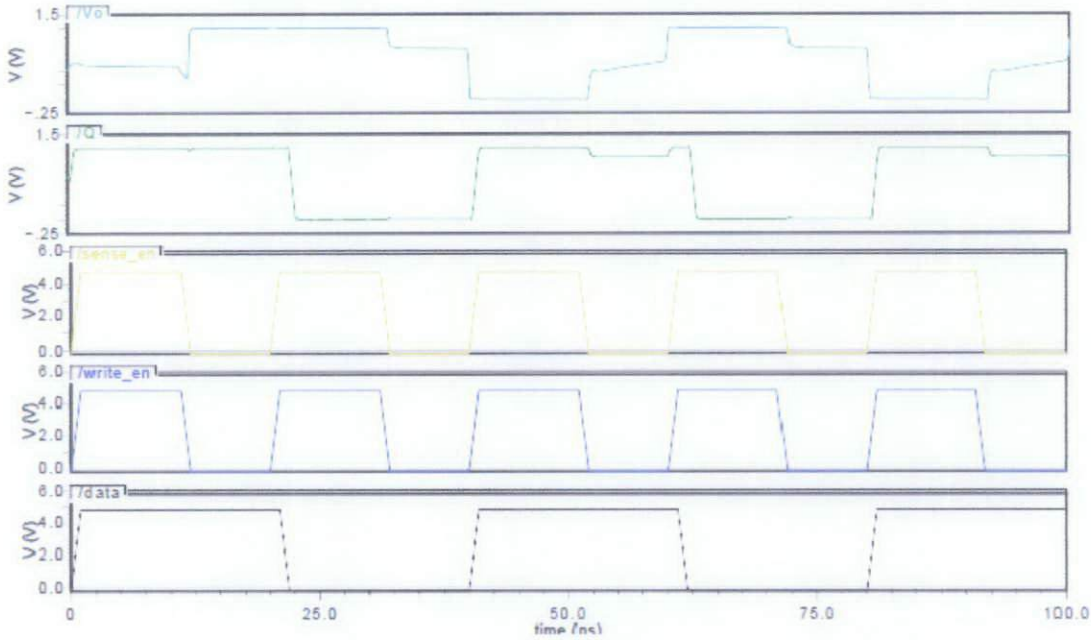
APPENDIX XXIII

Simulation for Temperature of 305°C with V_{DD} = 5 V and f_{CLK} = 100 MHz by Using tsmc35 Process



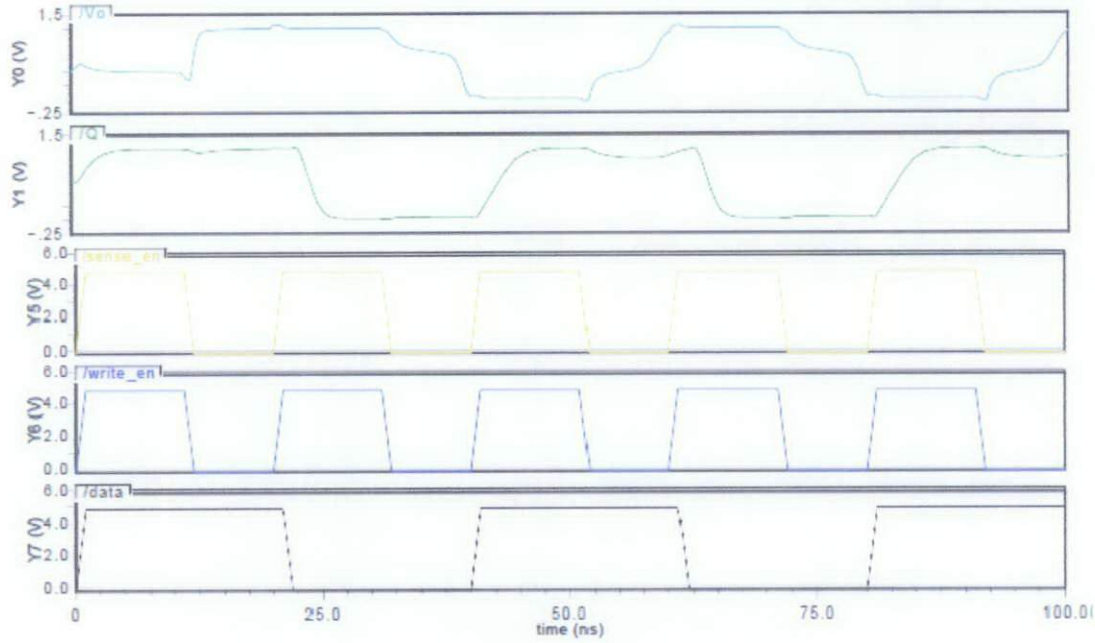
APPENDIX XXIV

Simulation for Temperature of -230°C with V_{DD} = 1.25 V and f_{CLK} = 100 MHz by Using tsmc35 Process



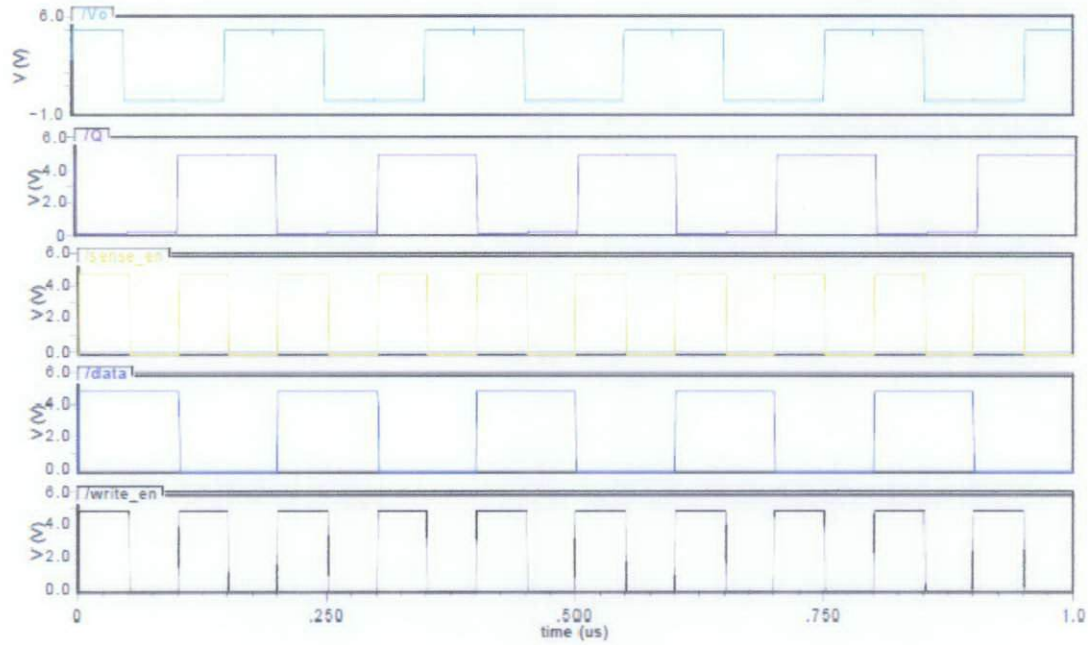
APPENDIX XXV

Simulation for Temperature of 121°C with V_{DD} = 1.25 V and f_{CLK} = 100 MHz by Using tsmc35 Process



APPENDIX XXVI

Simulation for Temperature of -250°C with V_{DD} = 5 V and f_{CLK} = 20 MHz by Using hp14tb Process

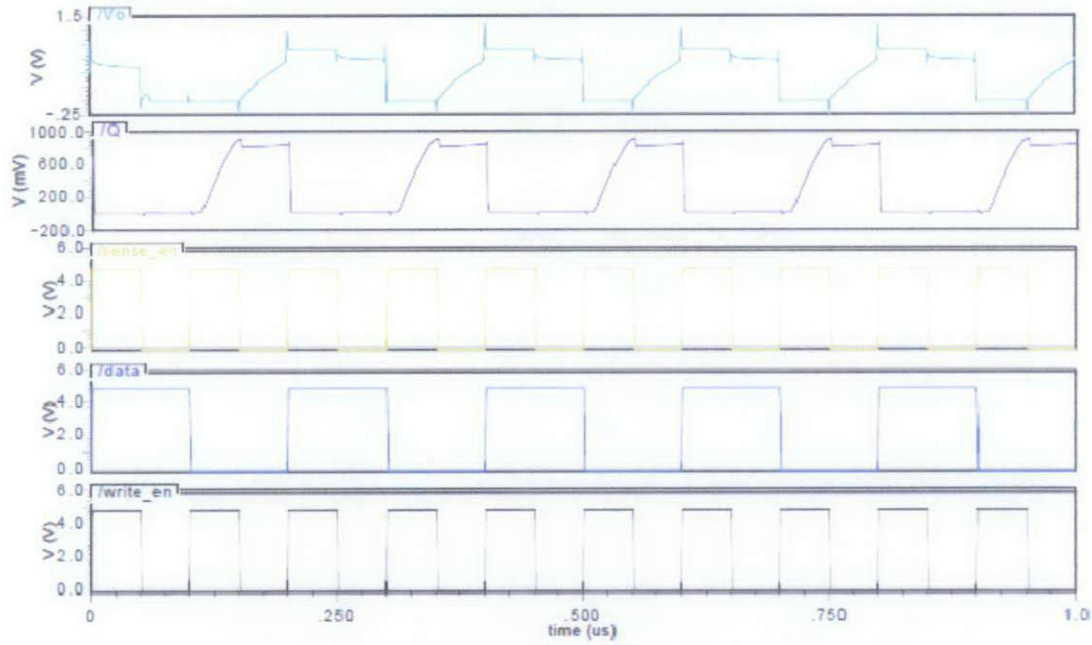


APPENDIX XXVII

Simulation for Temperature of 270°C with V_{DD} = 5 V and f_{CLK} = 20 MHz by Using hp14tb Process

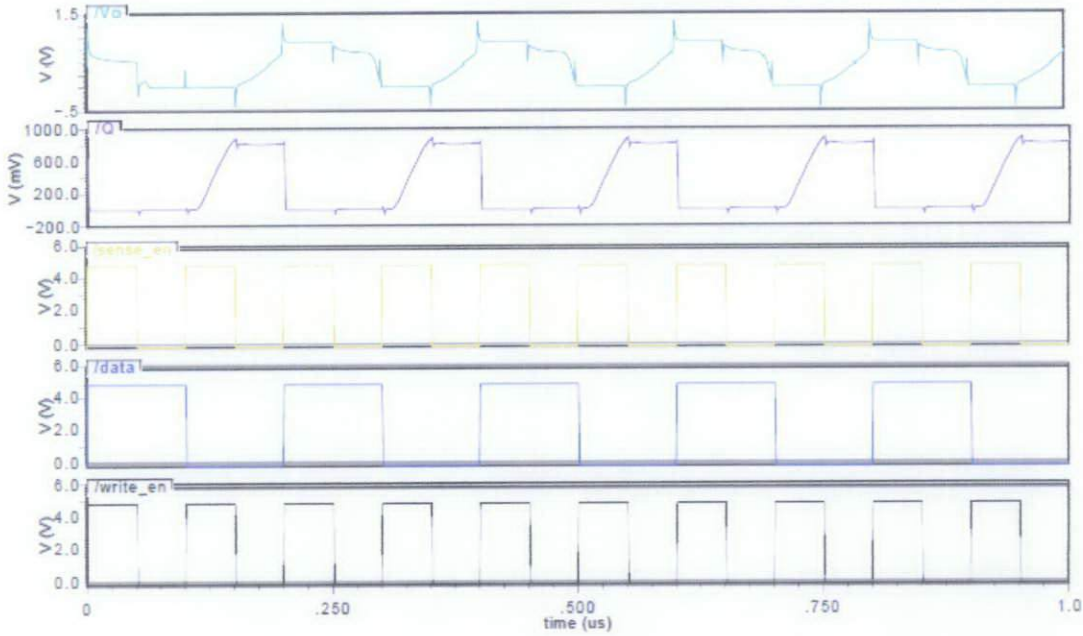
APPENDIX XXVIII

Simulation for Temperature of -117°C with V_{DD} = 0.91 V and f_{CLK} = 20 MHz by Using hp14tb Process



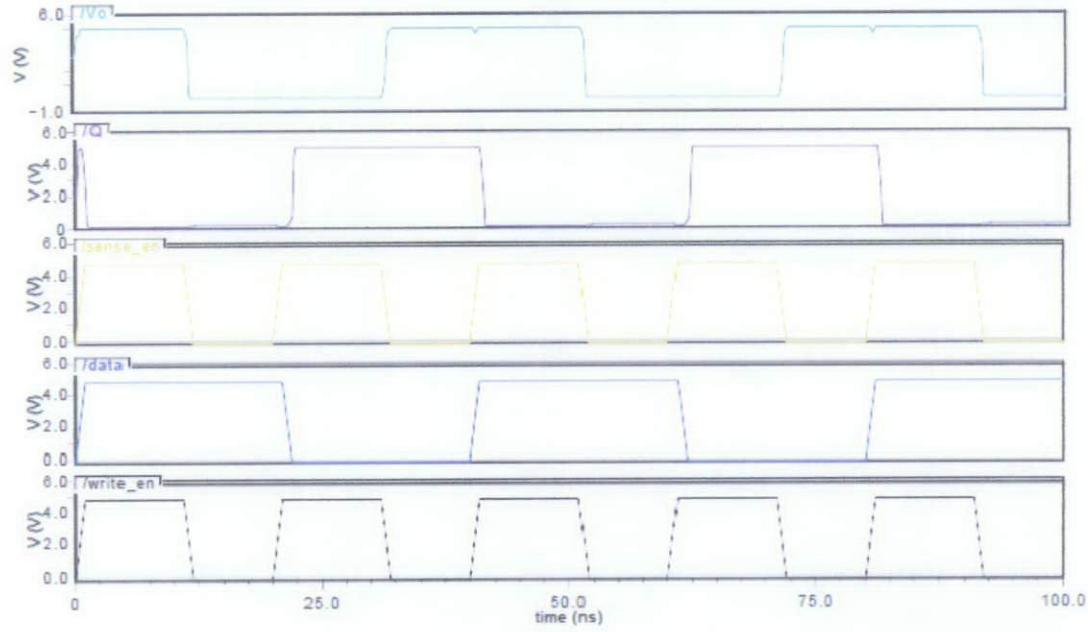
APPENDIX XXIX

Simulation for Temperature of 58°C with V_{DD} = 0.91 V and f_{CLK} = 20 MHz by Using hp14tb Process



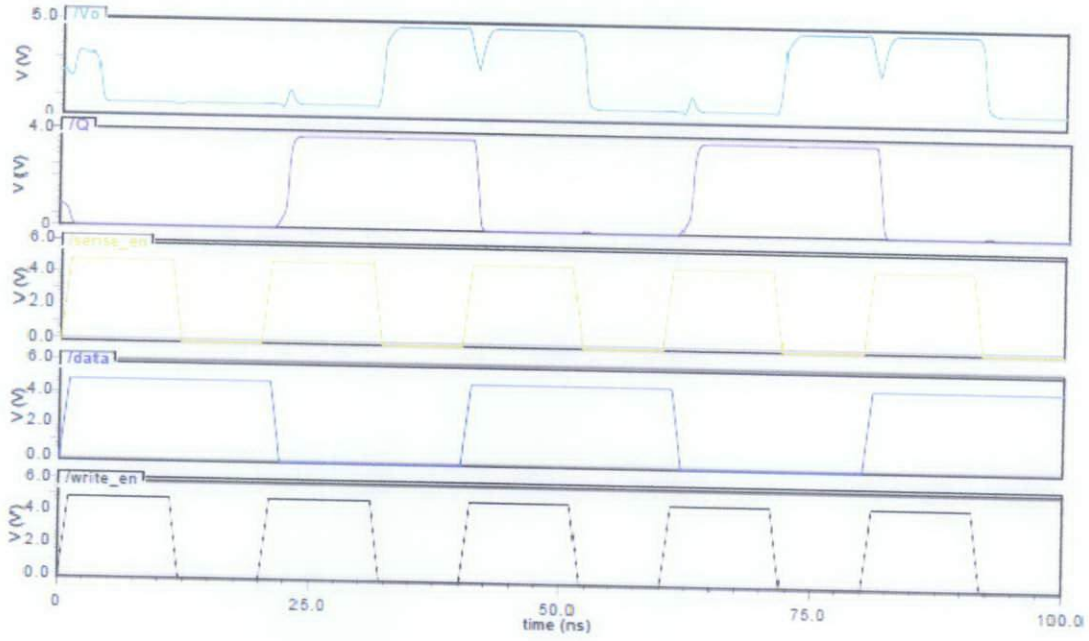
APPENDIX XXX

Simulation for Temperature of -250°C with V_{DD} = 5 V and f_{CLK} = 100 MHz by Using hp14tb Process



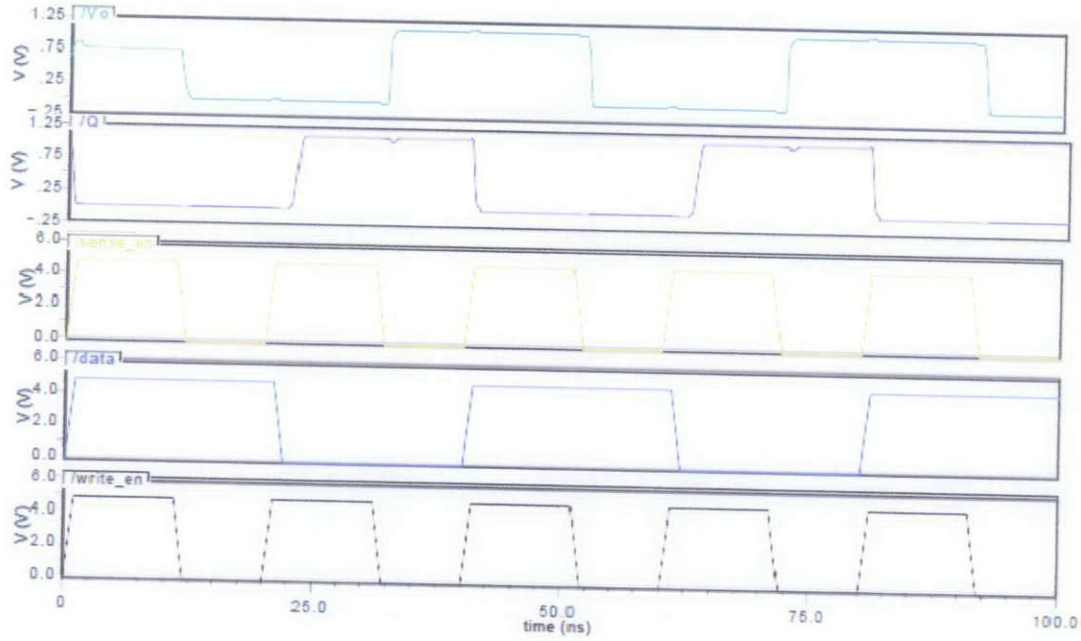
APPENDIX XXXI

Simulation for Temperature of 265°C with V_{DD} = 5 V and f_{CLK} = 100 MHz by Using hp14tb Process



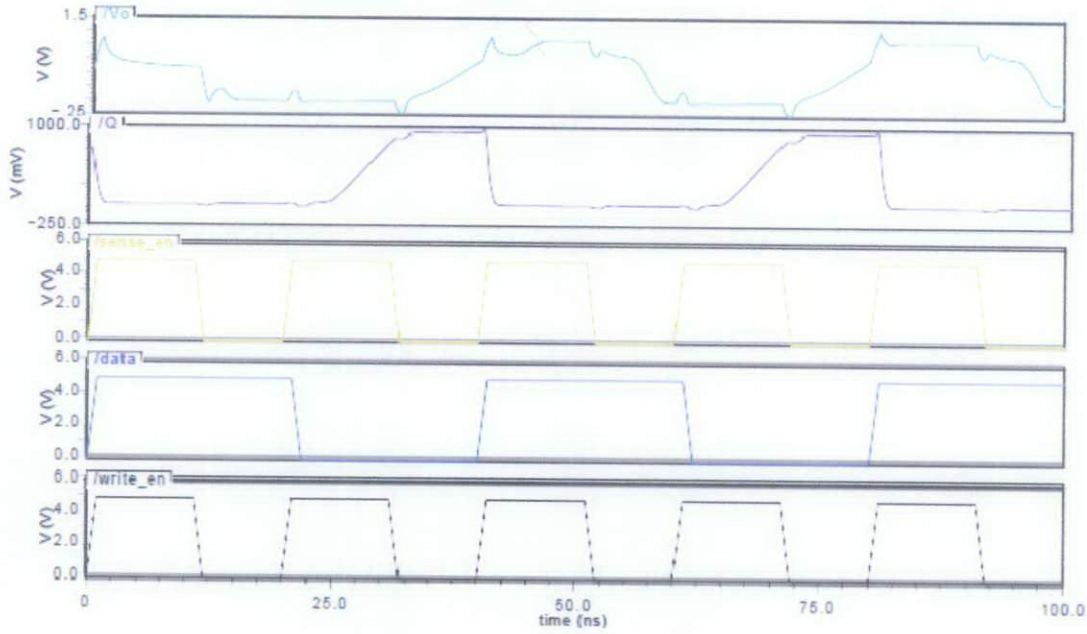
APPENDIX XXXII

Simulation for Temperature of -250°C with V_{DD} = 1.11 V and f_{CLK} = 100 MHz by Using hp14tb Process



APPENDIX XXXIII

Simulation for Temperature of 35°C with V_{DD} = 1.11 V and f_{CLK} = 100 MHz by Using hp14tb Process



APPENDIX XXXIII

Simulation for Temperature of 35°C with V_{DD} = 1.11 V and f_{CLK} = 100 MHz by Using hp14tb Process