THE IMPACT OF LOW DUTY CYCLES IN HIGH FREQUENCY GATE DRIVER

By

ATIQAH BINTI AB. RAHIM

FINAL REPORT

Submitted to the Electrical & Electronics Engineering Programme

in Partial Fulfilment of the Requirements

for the Degree

Bachelor of Engineering (Hons)

(Electrical & Electronics Engineering)

Universiti Teknologi PETRONAS

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CERTIFICATION OF APPROVAL

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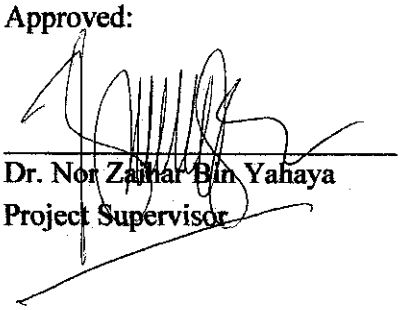
Approved:



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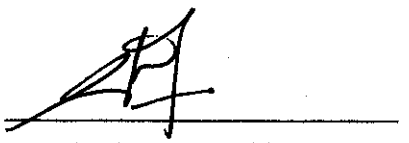
January 2011

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



Atiqah Binti Ab. Rahim

ABSTRACT

This study is about the impact of low duty cycle in high frequency gate driver. Duty cycle is important for power electronic device to make it work efficiently. Thus, the objective for this project is to design the lowest duty cycle as possible in order to observe the impact on gate driver and converter. The different value of duty cycle will be applied to two different types of gate drivers which are conventional gate driver and resonant gate driver. By applying pulse width modulation (PWM) to gate driver switches, it will be determined the duty cycle of the gate driver. The PWM is fed directly to both switches on drive circuit to activate the power MOSFET. Thus, by changing the PWM value, it will affect the duty cycle of the gate driver and resultant power MOSFET, *M3*. Therefore, the different output voltage, output current and operation mode of buck converter can be determined from the duty cycle at *M3*. Thus, the lowest duty cycle can be obtained with respect to the buck converter's performance. Some basic calculations and relationship between duty ratios to the converter will be explored in this work. However, the dead time application needs to be considered to avoid cross conduction for gate driver circuit to improve the efficiency of the driver. The findings show the lowest duty cycle of high frequency CGD is 16 % whilst 15 % for RGD.

ACKNOWLEDGEMENT

In the name of Allah, the Most Gracious, the Most Merciful. I give a lot of thanks and praise to God for His guidance and blessings throughout the semester to accomplish this Final Year project.

My deepest gratitude and admiration goes to my Supervisor, Dr. Nor Zaihar Bin Yahaya for being supportive and willing to share outstanding knowledge and expertise upon the project completion. Under his continuous supervision, the project is able to complete within the schedule.

Besides, I would like to take this opportunity to express my deepest appreciation to my fellow colleagues and family members for continuously lend me a shoulder and helpful hands upon the completion of this project. Hopefully, this project would be beneficial for my future undertaking and career development.

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ABBREVIATIONS AND NOMENCLATURES

t_{on} : ON time state (sec)

t_{off} : OFF time state (sec)

D : Duty Cycle (%)

T : Period (sec)

$M1$: High side switch

$M2$: Low side switch

$M3$: Resultant Power MOSFET

PWM : Pulse width modulation

$V1$: Gate Driver Voltage Source (V)

R_g : Gate resistor (Ω)

V_{out} : Output Voltage (V)

V_{in} : Input Voltage (V)

D : Diode

C : Capacitor (F)

L : Inductor (H)

iLr : Inductor current (A)

Lr : Resonant Inductor (H)

td : Time Delay (sec)

tr : Rise time (sec)

tf : Fall Time (sec)

iL_{max} : Maximum Inductor Current (A)

iL_{min} : Minimum Inductor Current (A)

I_{max} : Maximum Current (A)

I_{min} : Minimum Current (A)

fs : Switching frequency (Hz)

t_{rec} : Recovery time (sec)

ΔV : Ripple Voltage (V)

CHAPTER 1

INTRODUCTION

1.1 Research Rationale

The ultimate goal for this work is to design the low duty cycle for high frequency gate driver and to observe the impact by having the low duty cycle. The first task is to design the suitable gate drivers which are conventional and resonant gate driver at high frequency, 1 MHz. The resonant gate driver is designed to improve the performance of conventional gate driver for high frequency.

Then, the different in duty cycles will be applied to both drivers in order to get the lowest duty cycle can be operated. Once the lowest duty cycle is determined, the gate driver's performance and converter will be analyzed at high frequency.

However, there are issues related to high frequency applications in MHz range especially the significant gate driving losses, where in the high-current applications, it requires large die size active switches, often MOSFETs. At higher switching frequency, the increasing gate driving loss may often offset the advantages gained by the lower conduction losses with a large die size MOSFETs [1].

The second task is the implementation of the pulse width modulation to the gate driver. Hence, it needs to be designed correctly in designing the duty cycle for the gate driver. The changes of pulse width modulation will change the duty cycle of the gate driver.

1.2 Problem Statements

The different value of duty cycle on gate driver will affect the resultant power MOSFET and also to the power converter. Pulse width modulation needs to be designed appropriately at the gate driver's switches without any cross conduction. It is because, the incorrect signal will be fed to the power converter and may affect the performance of the converter.

It is impossible to have too low duty cycle for high frequency gate driver that it might introduce problems in operating system of gate driver. The low duty cycle from the driver will be applied to the buck converter where the maximum duty cycle is 50 %. Thus, some research and different duty cycle values will be tested to simulate the conventional gate driver and resonant gate driver.

1.3 Objectives

There are few objectives to be achieved in this project:

i. To understand and simulate the Conventional Gate Driver (CGD) at high frequency.
ii. To understand the function of duty ratio in totem-pole CGD.
iii. To apply the buck converter as an application to the driver.
iv. To apply Resonant Gate Driver (RGD) instead of (CGD) with same value of duty cycle.
v. To analyzed the performance of CGD and RGD after simulation.

1.4 Scope of Study

There are two types of gate drivers used in these projects: conventional and resonant gate driver. This study will focus on the different value of duty cycle applied to the gate driver in order to obtain the lowest duty cycle.

The 1 MHz of switching frequency is used in this work and the application circuit is a buck converter. Then, the circuit will be simulated using Pspice software and the other settings will be discussed in details in Chapter 3.

The graph and analysis for both drivers and buck converter's performance are based on Pspice simulation. Thus, by having this study, the limitation of duty cycle to the gate driver will be determined to make gate driver operate properly.

CHAPTER 2

LITERATURE REVIEW

2.1 Duty Cycle

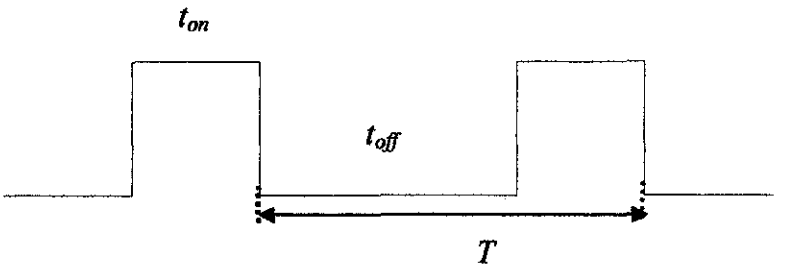

Figure 1: Duty Cycle Pulse

The duty ratio, D or duty cycle is defined as the percentage of t_{on} state in one complete switching cycle. It is also known as a fraction of time that a system is in an active state. Similarly, duty cycle is the proportion of time at which a component, device, or system can operate. It can be represented as in Eq. (1):

$$D=\frac{t_{on}}{T} \tag{1}$$

where T is the period of the overall system as shown in Figure 1. In this high frequency of 1 MHz, the period is 1 μs while t_{on} will be represented as active state. Some probability can be obtained by using Eq. (1) with the constant value of period, T which is;

i. The duty cycle is high if t_{on} is at long duration.

ii. The duty cycle is low if t_{on} is at short duration.

In this work, the probability (ii) will be used to observe the impact to the gate driver with the application of buck converter. The t_{on} will be designed as short as possible to obtain low duty cycle. Any smaller changes of duty cycle will affect the gate driver's operation, converter's application and pulse width modulation.

2.1.1 Effects on Gate Driver

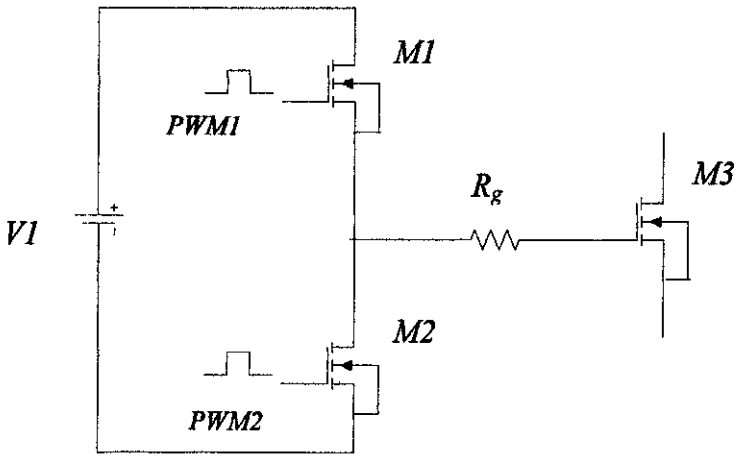

Figure 2: Conventional Gate Driver (CGD)

Figure 2 shows the configuration of CGD. The duty cycle is applied to the *PWM1* and *PWM2* of the gate driver. It is also a signal to turn on the *M1* and *M2* switches. The signal is an alternating pulse and the details of pulse width modulation will be discussed in section 2.3. In [2], the pulse width of *M1* is smaller than *M2* in low duty cycle application. Whereas, the pulse width of *M1* will increase as the duty cycle of the gate driver increases.

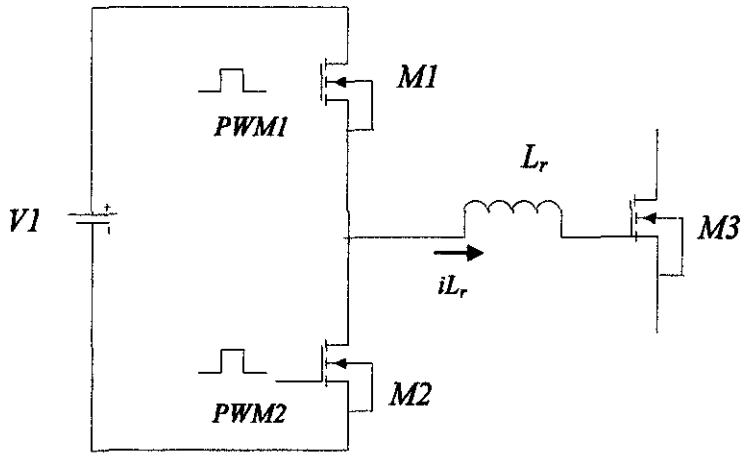

Figure 3: Resonant Gate Driver (RGD)

Figure 3 shows the RGD implementation. The duty ratio will determine the length of conduction time of power MOSFET, *M1* that provides sufficient t_{on} for iL_r to completely charge and discharge. Otherwise, this eventually results in oscillation during t_{off} and hence generates power loss [3].

With the significant impact of duty cycle for RGD implementation, the iL_r can be determined even shorter or longer duration when duty cycle is applied. Hence the power dissipation in RGD is easy to calculate [3, 4].

When the various duty cycles applied to the both drivers, this may affect the performance of the resultant Power MOSFET, *M3*. Any changes in duty cycles will change the resultant power MOSFET. In addition, the pattern of resultant power MOSFET is similar to pattern of *M1* pulses.

2.1.2 Effects on Buck Converter

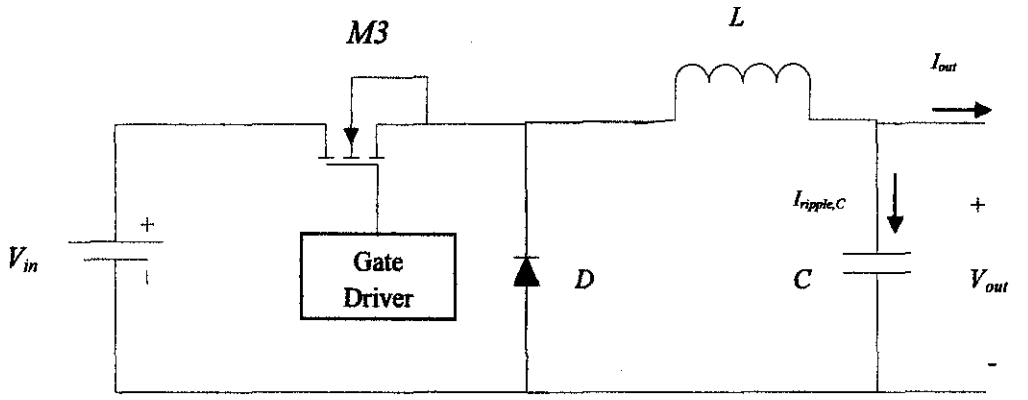

Figure 4: Buck Converter Application

Buck converter as shown in Figure 4 is activated by the gate driver. The duty cycle from the gate driver is applied to the resultant power MOSFET, *M3* and gives a new duty cycle to buck converter. That means, the duty cycle of the converter is based on the resultant of power MOSFET, *M3*. Thus, by having a different duty cycle at gate driver, it will change the duty cycle of *M3* and consequently affect buck converter's output parameters values.

For different duty cycle in *M3*, the *L* and *C* will also be changed accordingly. The maximum limit for duty cycle in application of buck converter is 50 %. When the duty cycle is 50 %, the worst case $I_{ripple,C}$ at capacitor will occur which is about one half of the I_{out} [5].

The buck converter can operate around 10 % as low duty cycle that convert 7 V to 12 V down to 2 V [6]. However, this application is only apply for 300 kHz switching frequency.

2.1.3 *Effects on V_{out} and I_{out}*

$$V_{out}=(D)(V_{in}) \quad (2)$$

From Eq. (2) above, the duty cycle will affect the output voltage. This equation can be implemented by using buck converter as shown in Figure 4. Having a constant value of V_{in}, the V_{out} can be varied depending on the duty cycle applied to the gate driver. In this case;

i. V_{out} is high when D is high.
ii. V_{out} is low when D is low.

Based on Eq. (2), the gate driver can operate even at lower duty cycle. However, this is not true since the C and L components values need to be considered as long as it is an acceptable value. This is because, it can affect the performance of the buck converter and also the iL_r for RGD implementation.

Besides, by changing the duty cycle, it will change the value of I_{out} based on Eq. (3) below;

$$I_{out}=\frac{I_{in}}{D} \quad (3)$$

Hence, further studies in low duty cycle will be focused in order to know how low duty cycle can reach. Therefore, the gate driver can operate properly after some issues are considered as summarized in Table 1.

Table 1: Summary Issues Related to Duty Cycle

Description of Duty Cycle	Issues	Advantages
Gate Driver switches [2]	The pulse width of *M1* is smaller than the pulse width of *M2* in low duty cycle application.	Easily determined the low duty cycle designed.
Resonant Gate Driver [3]	Provide sufficient t_{on} for iL_r to completely charge and discharge. Otherwise, this eventually results in oscillation during t_{off} and hence generates power loss.	To allow iL_r flow without disruptions.
Application of Buck Converter - $I_{ripple,C}$ [5]	The worst case $I_{ripple,C}$ is about one half of the I_{out} for 50 % duty cycle.	-
- V_{out} =2 V - V_{in} = 7 V to 24 V [6]	Only apply for 300 kHz switching frequency.	10 % performance of duty cycle

2.2 Gate Driver

Gate driver is the body of switching circuit which activates the t_{on} and t_{off} of transistor. It includes either half bridge or a full bridge configuration of the gate drive signals. The gate driver circuit has to be operated efficiently with low power loss in order to produce a high performance system.

The switching for the gate driver can be activated using either bipolar transistor or power MOSFET. The bipolar transistor uses current driven while the power MOSFET is a voltage driven with its insulated gates. With the basic knowledge of the principles of driving the gates of these devices will allow the designer to speed up or slow down the switching speeds according to the requirements of the application [7].

Gate driver circuit is crucial for accurate turn on and turn off of the transistor. Besides, by having a high frequency, this can cause gate driving loss, lower efficiency and excessive power loss due to power challenge in turning on and turning off the power MOSFET. For most converters, the gate energy losses become a concern at switching frequencies beyond 1 MHz.

There are several types of gate driver used in order to drive the power converter. Here, the two types of gate drivers will be discussed in this project are conventional gate driver and resonant gate driver.

2.2.1 Conventional Gate Driver (CGD)

The conventional gate driver shown in Figure 2 has been developed and has a same configuration of half bridge structure known as totem-pole driver. A bipolar totem-pole is a pair of driving switches, *M1* and *M2*. Besides, it includes an equivalent driving resistor R_g between driving switches and power MOSFET, *M3*.

When *PWM1* is generated to *M1*, it will turn on the *M1* while *M2* will be turned off. The signal's behavior at *M1* is due to the gate driver voltage source, *V1*. In order to know the pulses are correct, the node voltage will be measured. The procedure on how to measure the node voltage is discussed in section 3.5.1.

However, the conventional gate driver has a lot of problem due to switching losses, gate driving losses related to the main power MOSFET gate charge especially at high frequency operation which is the gate driving loss is approximately two-third of the total gate drive loss [8].

2.2.2 Resonant Gate Driver (RGD)

Resonant gate driver is designed to improve the performance of conventional gate driver in order to reduce gate driving losses caused by high switching frequency operation [9]. It consists of inductor, L_r instead of resistance between power MOSFET and totem pole driver. The resonant gate driver technique is utilizing L-C resonance to charge and discharge the MOSFET gate capacitance [10].

The operation of the RGD is similar to CGD but, this driver has a charging and discharging gate capacitance of MOSFET through inductor L_r. The energy losses are dissipated when input gate capacitance charges and discharges during the switching stage. Hence, some of the dissipated energy must be recovered. The sufficient duration signal must be applied to the switch of gate driver to make the L_r charge and discharge properly.

However the new resonant driver has been introduced by using two half bridge circuits [10, 11]. The energy for new resonant gate driver in this article is recovered during both charging and discharging transitions.

In designing the gate drive circuit, it has to make sure that the input energy is sufficient to the gate of the power MOSFET in order to make it conduct successfully. Hence, the parameters that need to be considered are: voltage applied to the gate driver,VI switching frequency for the switch, time delay, duty ratio, D, and the size of resonant inductor, L_r.

There are some probabilities when choosing the size of the resonant inductor as stated in article [12] which are;

i. If L_r is higher, it will increase the charging and discharging time of iL_r and causes the lower speed.
ii. If L_r is lower, the transient response will be reduced and this causes the high speed.

2.3 Pulse Width Modulation (PWM)

Nowadays, power converter's switching frequency is being pushed to high frequency up to MHz range with fast transient response by using PWM.

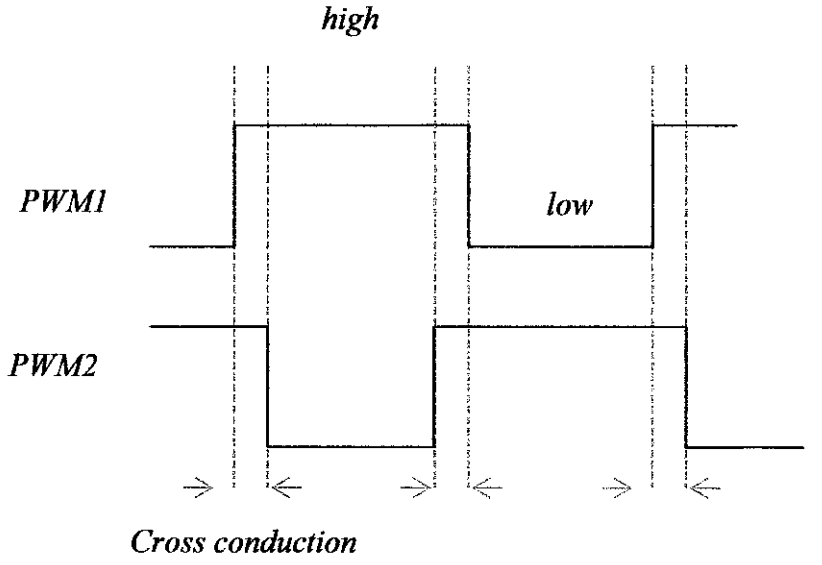

Figure 5: Cross Conduction Waveform

PWM shown in Figure 5 is widely used in digital to analog conversion by using *'high'* and *'low'* signal levels of digital pulses to create some analog values. The h*igh* side is known as t_{on} while *low* side is t_{off}. However, PWM needs to be designed correctly to avoid cross conduction as shown in Figure 5 which is an overlapping between t_{on} and t_{off}.

The duty cycle of a square wave is modulated to encode a specific analog signal level. The t_{on} is the time during which the DC supply is applied to the load, and the t_{off} is the times during which that supply is switched off. Given a sufficient pulse width, any analog value can be encoded with PWM [13].

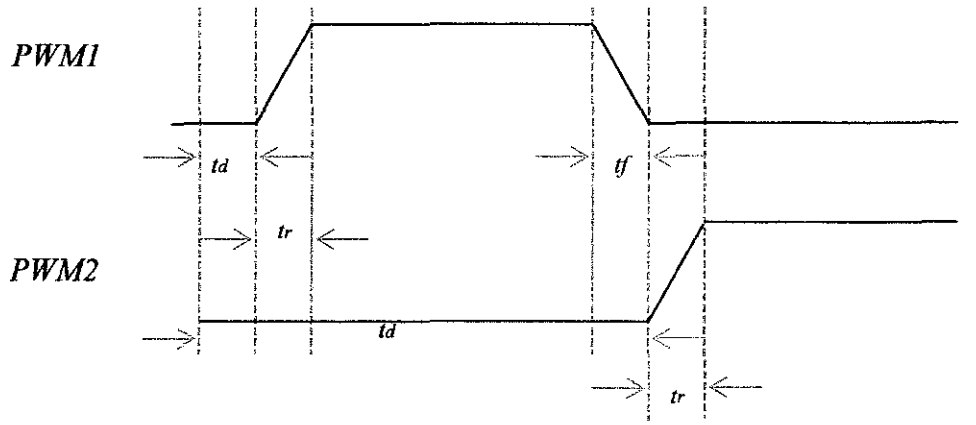

Figure 6: PWM Design

In order to avoid any cross conduction between two pulses, the time delay, *td*, rise time, *tr* and fall time, *tf* will take into consideration in designing the PWM as shown in Figure 6. Time delay is very important to prevent short circuit which occurs when both signals are at *low* state.

Since the PWM is fed to the *M1* and *M2* switches, it also represents the duty cycles generated to the driver. So, by varying the PWM at the gate driver, it will vary the duty cycle as well.

From PWM, it can adjust the duty ratio to produce voltage in the range of 10 % to 100 % of the maximum supplied voltage, depending on the PWM resolution. The PWM resolution is defined as the maximum number of pulses that can be packed into a PWM period. Meanwhile, the PWM period is an arbitrarily time period in which PWM takes place [14].

2.4 Body Diode Conduction

Body diode conduction occurs at the node voltage between totem pole of driver, *M1* and *M2*. Body diode conduction is due to internal diode of the power MOSFET called parasitic diode. When *M1* and *M2* switches are turned off, this parasitic diode is forward biased due to diode continuity approaching -0.7 V and exists at the falling edge of the switch-node [15].

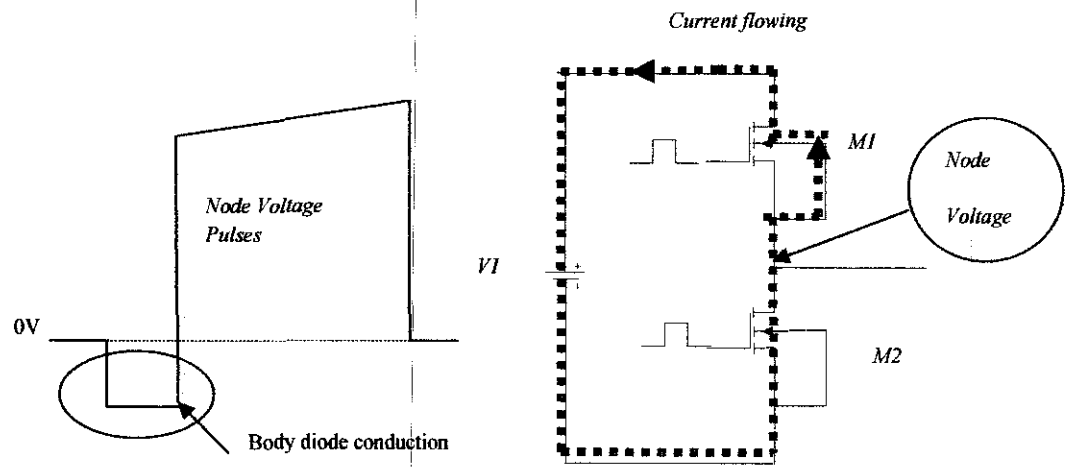

Figure 7: Body Diode Conduction

Figure 7 shows the gate driver and body diode conduction at the node voltage pulses. It shows that the body diode conduction occurs at *M1* when the switch *M2* is turned off due to current flowing through the driver as shown in Figure 7. However, the current in the body diode *M1* needs to be removed before *M1* turns on. This is because, if the body diode conduction in the circle occurs, it might result in conduction loss. Smaller body diode conduction will have smaller conduction loss. Hence, it is important to have a sufficient time delay, *td* to reduce this loss [3, 16].

2.5 Buck Converter

In this work, the buck converter is used as an application for the gate driver. This converter is a common Dc-Dc converter topology in power management applications. It can convert a voltage source into a lower regulated voltage. For example, within a computer system, voltage needs to be stepped down and a lower voltage needs to be maintained.

There are five standard elements or components for buck regulator shown in Figure 4 which are;

i. Power MOSFET, *M3*
ii. Diode, *D*
iii. Capacitor, *C*
iv. Inductor, *L*
v. Resistor, *R*

The resultant power MOSFET, *M3* of the gate driver is acting as the switch of buck converter. Hence, the duty cycle of the buck converter depends on this switch.

Therefore, the values for the component of *L, C* and *R* have to be changed for different values of duty cycle. The methods and calculation to obtain the component values will be discussed in Chapter 3.

2.5.1 Operation Mode of Buck Converter

The buck converter operates in continuous conduction mode (CCM). This is because, CCM is the best choice for optimum performance and it allows maximum output power to be obtained from a given input voltage and switch current rating [17].

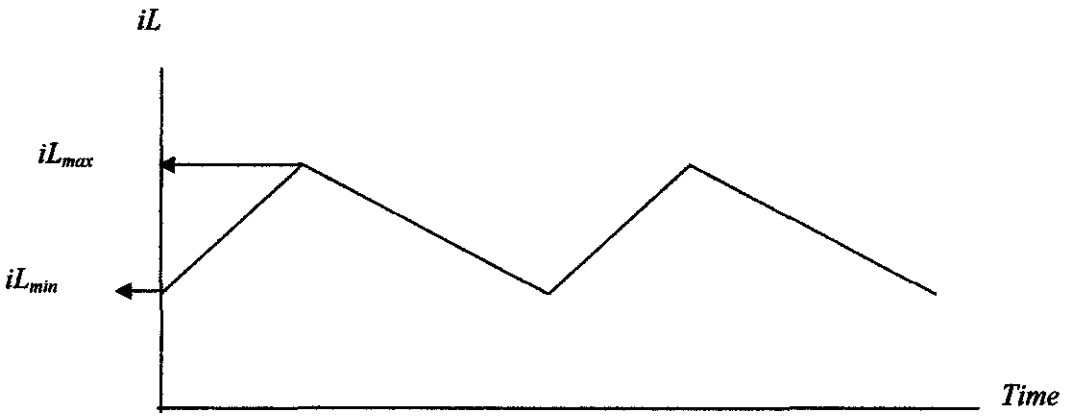

Figure 8: Continuous Conduction Mode

The graph for CCM is shown as Figure 8 above. CCM means, the current in the energy transfer inductor never goes to zero between switching cycles.

In order to avoid the discontinuous conduction mode (DCM), it is important to choose the value for inductor, L that obtained from calculation which will be discussed in section 3.4. The equation is used to determine the critical value for inductor. Hence, the inductor value should be greater than the critical inductor value for CCM operation. It is because, the critical value of inductor is the minimum limit to allow the converter operating in DCM.

CHAPTER 3
METHODOLOGY

3.1 Project Planning

The project planning of the project is shown in the flow chart at Figure 7 below;

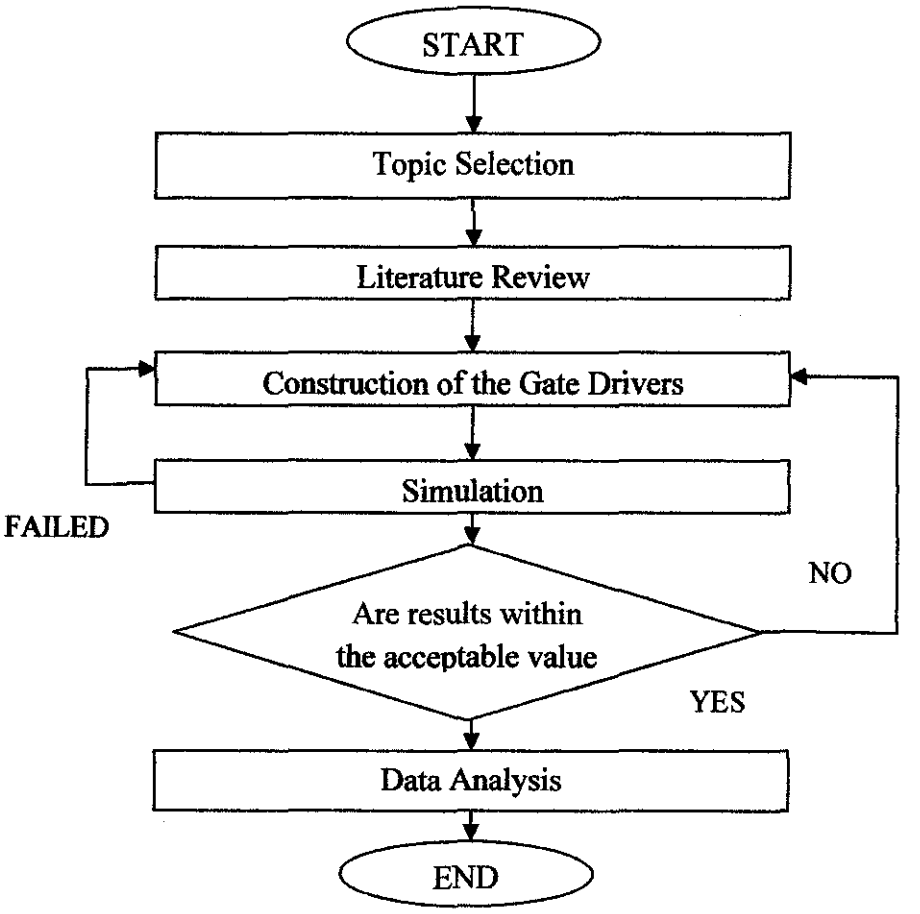

Figure 9: Flow Chart for the Project Planning

From the flow chart shown in Figure 9, the project planning must be completed within the schedule based on the Gantt chart (Appendix A). After selecting of the topic entitled "The Impact of Low Duty Cycle in High Frequency Gate Driver", the literature review is the most important part to be covered. Many research papers are gathered to understand the basic concept related to duty cycle of the high frequency gate driver.

Next, the gate drive consisting of conventional gate driver (CGD) and resonant gate driver (RGD) are constructed as shown in Figure 2 and Figure 3. The selection of components for both gate drivers is important in order to simulate the circuit.

The software used to simulate the both drivers is Pspice. If the simulation fails, the components need to be selected again with different values. If the simulation passes, the buck converter will be used as application to the gate driver. Then, the different values of duty cycle are applied to the drivers. If the simulation results are wrong, all component values for converter need to be changed.

The analyses in the impact of duty cycle to the gate driver will be discussed in details in Chapter 4. Here, the simulation results will be displayed between both drivers. Thus, the lowest duty cycle *M1* of the driver can be determined.

3.2 Project Activities

3.2.1 Construction of the PWM

The construction of PWM is the most important part before designing high frequency gate driver. Besides, the correct PWM generation must be used to avoid the cross conduction as shown in Figure 5. The value for PWM's setting in the Pspice with 1 MHz is listed in the Table 2 below.

Table 2: PWM's Setting for *M1*=23.5 %

Component	Value
PWM1	V1=0V, V2=5V, *td*=5ns, *tr*=5ns, *tf*=5ns, PW= 235ns, PER=1000ns
PWM2	V1=0V, V2=5V, *td*=255ns, *tr*=5ns, *tf*=5ns, PW= 735ns, PER=1000ns

Table 2 shows the PWM's setting for high frequency gate driver using Pspice software. In this case, the total period for the PWM at 1 MHz is 1000 ns. By applying 5 ns for each *td, tr* and *tf* this will give 15 ns to the dead time as shown in Eq. (4):

$$\text{Dead Time} = td + tf + tr \tag{4}$$

At first, the 23.5 % duty cycle at *M1* of the gate driver is obtained. Thus, 235 ns need to be fed at *PWM1*. Meanwhile, the pulse width for *PWM2* will be 735 ns. It is important to check the PWM pulse before constructing the driver. So, the result of the pulses will be shown in section 4.1.1.

However, the PWM's setting is not a constant value since the different value of duty cycle needs to be applied. Any changes in duty cycle at *M1* switch will change the PWM's setting with respect to same dead time value. In this work, the variations of duty cycle at M1 are from 20 % to 14 %. Therefore, in section 4.1.1, the pulse width at *PWM1* and *PWM2* at different duty cycle tested in the simulation will be shown.

3.3 CGD's Construction

There are two different types of gate drivers constructed; CGD and RGD. The totem-pole which consists of *M1* and *M2* is the basic circuit for driver including power MOSFET, *M3*.

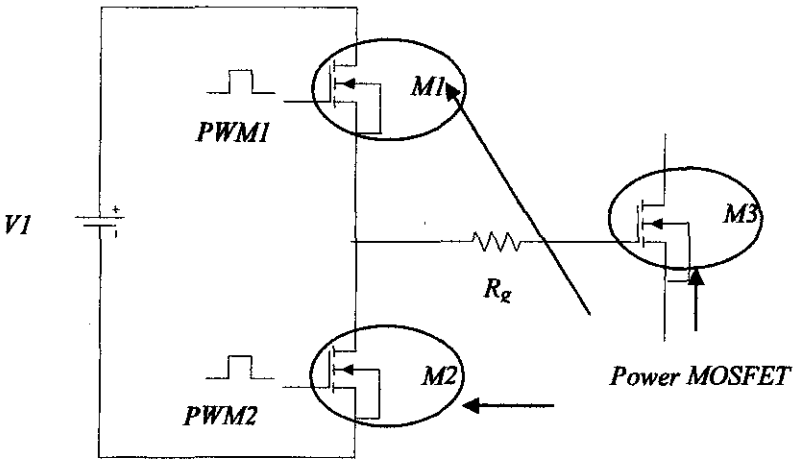

Figure 10: CGD's Construction

Based on Figure 10, it shows the CGD's construction. The *M1, M2* and *M3* are the power MOSFET used as switching devices for driver. The power MOSFET chosen must be suitable for the high switching frequency at 1 MHz. Therefore, IRFP250 has been chosen for all of them. It is based on the MOSFET characteristic for the high switching frequency.

Due to the IRFP250 datasheet (APPENDIX B), this power MOSFET is suitable for the high current and high speed switching which provides 33 A and 200 V. The *V1* as shown in Figure 10 is set to be 12 V. It is also the power supply to the resultant power MOSFET, *M3*.

Table 3: CGD's Components

Components	**Value**	**Type**
Power MOSFET	33 A/ 200 V	IRFP250
R_g	0.085 Ω	-

For CGD construction, the R_g value is 0.085 Ω as shown in Table 3. Based on the data sheet provided at APPENDIX B, the suitable R_g value is less than 0.085 Ω. Thus, in this project, the maximum value of R_g has been selected for the driver operation.

3.4 RGD's Construction

The only different construction between CGD and RGD is the gate resistor, R_g at CGD instead of resonant inductor, *Lr* at RGD.

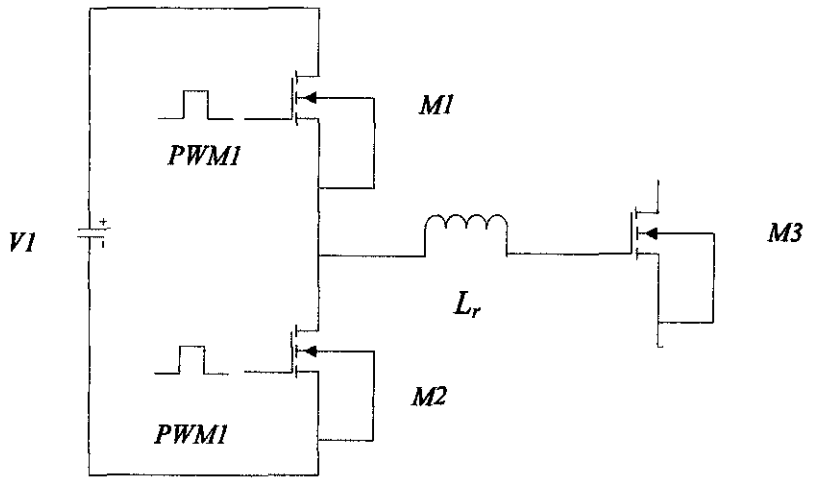

Figure 11: RGD's Construction

The RGD's construction shown in Figure 11 consists of L_r between the switching parts *M1, M2* and *M3*. It uses the same type of power MOSFET as CGD which is IRFP250. The suitable value for L_r needs to be chosen in order to make it charge and discharge completely within the pulse width given. This is because, the current through the inductor is varying with time. The relationship between inductor and current can be shown in Eq. (5);

$$V_L = L \frac{di_L}{dt} \tag{5}$$

Table 4: RGD's Components

Components	Value	Type
Power MOSFET	33 A/ 200 V	IRFP250
L_r	23 nH	-

Table 4 shows the components for designing the RGD. The L_r value for the RGD is 23 nH which is the maximum inductor value in this simulation. The value for L_r has been tested from 1 nH, 5 nH, 10 nH until the oscillation starts occur inside the pulse width given. Hence, the suitable value for L_r is an important in order to make iL_r to charge and discharge within the pulse width.

There are many types of analyses based on gate driver simulation for different duty cycles applied to *M1*. For examples, node voltage output, resultant power MOSFET, *M3* and body diode conduction time. The methods used to find these data will be discussed in section 3.3.1, 3.3.2 and 3.3.3, respectively.

3.5 Other's Part Measurement

3.5.1 Node Voltage Output

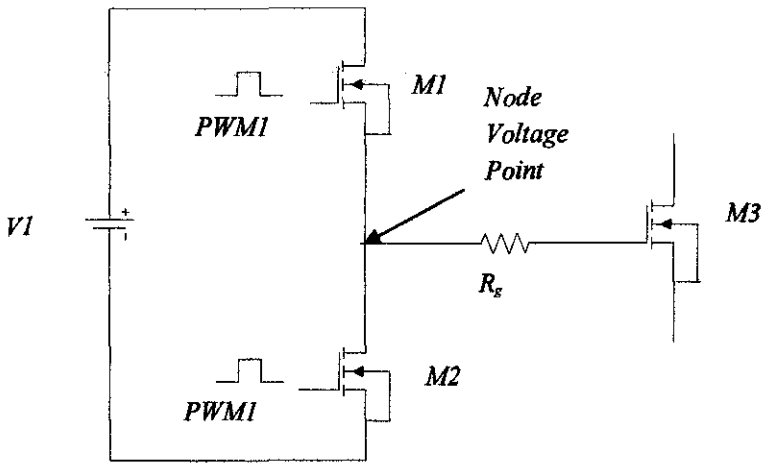

Figure 12: Node Voltage Point at Gate Driver

The node voltage is measured between *M1* and *M2* as shown in Figure 12 above. The voltage pin from the Psipce is placed exactly to the point after the design circuit is completed.

The node voltage is measured at 23.5 % of duty cycle at *M1* for CGD and RGD. The graph for node voltage output should have 12 V for the maximum voltage as set to the *V1*. The node voltage graph will be shown in section 4.1.2.1 for CGD and section 4.1.3.1 for RGD. As the duty cycles of the gate driver at *M1* changes, the node voltage will be measured to check the signal of the driver.

Next, the node voltage's result will be analyzed in detail in terms of the body diode conduction between the switches as in section 4.1.2.2 and 4.1.3.2. Then, the body diode conduction for different value of duty cycles with RGD will also be discussed in detail in the same section.

3.5.2 Resultant power MOSFET, M3

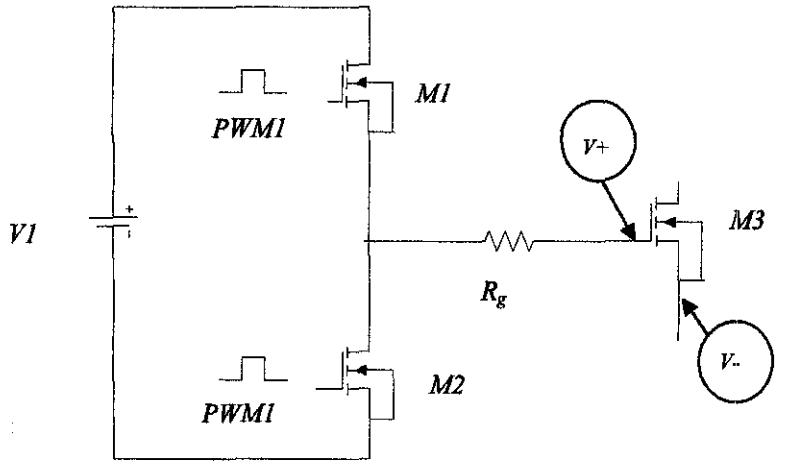

Figure 13: $V_{gs,\ M3}$ Point

The differential voltage marker is placed at the gate to source of power MOSFET, *M3* as shown in Figure 13. It is also known as $V_{gs,\ M3}$. The circuit is simulated to observe the pulses of the resultant power MOSFET, *M3* after 23.5 % of duty cycle at *M1* is applied.

Next, the resultant power MOSFET, *M3* for RGD will also be measured at the same point. Besides, the same graph will be analyzed for different value of duty cycle for both drivers. The results will be discussed in details in section 4.1.2.3 for CGD configuration and section 4.1.3.4 for RGD configuration.

The changes of duty cycle at gate driver, *M1* will affect the duty cycle at the *M3*. Besides, the resultant power MOSFET will give the duty cycle for buck converter's application. Therefore, the construction of the buck converter will be based on the duty cycle at *M3*.

3.6 Buck Converter's Application

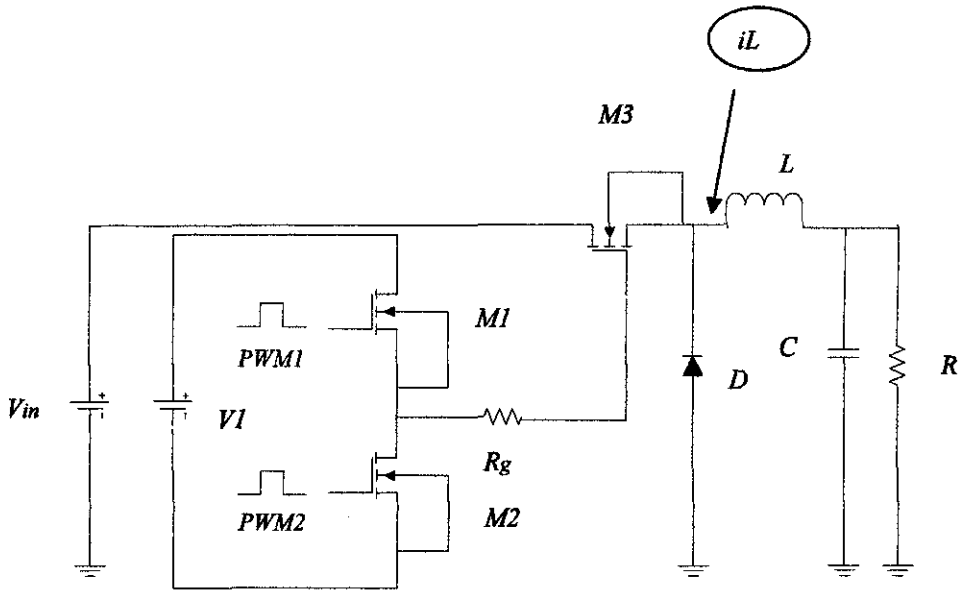

Figure 14: Gate Driver with Buck Converter's Application

After the gate driver is constructed, the buck converter will be fed to the resultant power MOSFET, *M3* as shown in Figure 14. There are five types of important components to construct buck converter which are *L, D, C, R* and *M3*. The value for all the components can be obtained based on the duty cycle at *M3*.

This duty cycle at *M3* can be obtained from the duty cycle of the gate driver, *M1*. In the beginning, the duty cycle of a gate driver is 23.5 %. Then, the different duty cycles are applied to the gate driver which is 20 % until 15 % eventually to observe the effect to the resultant power MOSFET.

Few parameters of buck converter's components are constant in order to make the calculation easier. Table 5 below shows the constant value of buck converter's component with MOSFET and diode type.

Table 5: Buck Converter's Components

Components	Value	Types
Vin	12 V	-
Power MOSFET	33 A/ 200 V	IRFP250
Resistor, *R*	3.5 Ω	-
Diode, D	-	1N6392

From the resultant power MOSFET, the buck converter's performance can be obtained such as the *iL* operation mode, output voltage and current. Hence, the parameters consisting *L* and *C* need to be chosen correctly.

Thus the parameters for the buck converter's components can be obtained from few equations below which are based on [18];

i. Inductor

$$Lcrit = \frac{1-D}{2}(T)(R) \tag{6}$$

The equation for critical inductor value as shown in Eq. (6) above can be used to obtain inductor value. The value for the inductor must be higher than *Lcrit* ($L > Lcrit$) in order to make the buck converter operate in CCM. Thus, the *L* value can be obtained after the *Lcrit* as shown in Eq. (6) has been calculated.

By referring to Figure 12, the operation mode of the buck converter can be obtained from the current flowing through the inductor, *iL*. Besides, the performance of *iL* can be evaluated based on different value of duty cycles applied to the driver from the changes of duty cycle in *M1*.

If the buck converter operates in DCM, the low duty cycle for a high frequency gate driver can be determined. All the graph and results will be shown in section 4.1.4.1.

ii. Capacitor

$$\frac{\Delta V}{Vo} = \frac{1-D}{8LCf^2} \tag{7}$$

D is the duty cycle at the resultant power MOSFET, *M3*. So, to get the duty cycle value at *M3*, the simulation of the driver needs to be performed. Then, the graph of the resultant power MOSFET is measured to obtain the duty cycle value.

In this project, the ripple voltage, ΔV is set to be constant which is 0.005V. However, the low value of ΔV is better for the performance of buck converter.

3.6.1 I_{out} and V_{out} at Lower Duty Cycle

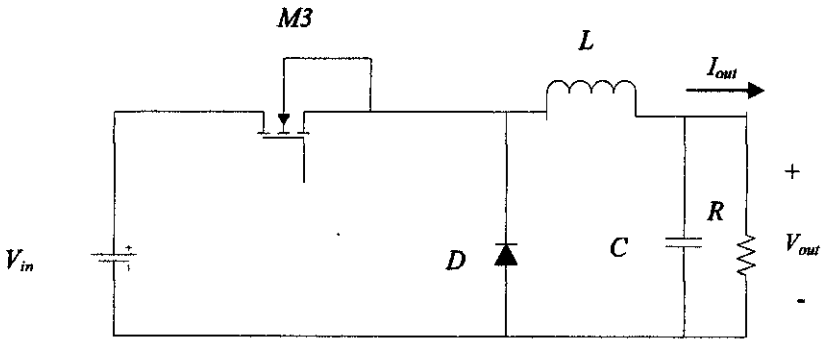

Figure 15: V_{out} and I_{out} Point at Buck Converter

After the lower duty cycle is obtained from the operation mode of buck converter, V_{out} and I_{out} are measured. By taking the voltage and current marker across *R*, the value for V_{out} and I_{out} can be determined as shown in Figure 15 above.

The values of V_{out} and I_{out} from the graph for the buck converter are compared to the calculation from the Eq. (1) and Eq. (2). Thus, the difference between calculation and graph can be determined. The graphs and values for V_{out} and I_{out} will be displayed and discussed in details in section 4.1.7 and 4.1.8. From the V_{out}, the ripple voltage can be measured based on Eq. (8) below;

$$\Delta V = \frac{V_{max} - V_{out}}{V_{max}} \text{ X } 100\% \tag{8}$$

As usual, the performance of the buck converter is evaluated based on different value of duty cycles applied to driver. So, the effect on the duty cycle can be observed clearly from the results.

The low duty cycle for a high frequency gate driver can be obtained from the operation mode of converter, V_{out} and I_{out} characteristic. Thus, more analyses for the buck converter's performance will be shown in Chapter 4.

3.7 Tools and Equipment Required

In this project, it is based on circuit simulation by using Pspice software and the detail for this software is indicated below;

Version : 8.0
Build : July 1997
Copyright : 1997 MicroSim Corporation

Other components used in the Pspice software include the library path shown in Table 6 below with transient analysis setting as tabulated in Table 7;

Table 6: Component Used and Library Path

Components	Types (Library)
IRFP250	PWRMOS.slb
1N6392	DIODE.slb

Table 7: Transient Analysis Setting

Transient Analysis	Duration
Print step	1 ns
Final step	1 ms

The graph will be simulated until 1 ms and will be printed for each 1 ns. This value is verified to all circuits in this project that includes the different value of duty cycle.

CHAPTER 4
RESULTS AND DISCUSSION

4.1 Results

In this section, the results of CGD and RGD are discussed in details. Thus, the lower of duty cycle for high frequency gate driver will be determined from the performance of the buck converter.

4.1.1 Pulse Width Modulation (PWM)

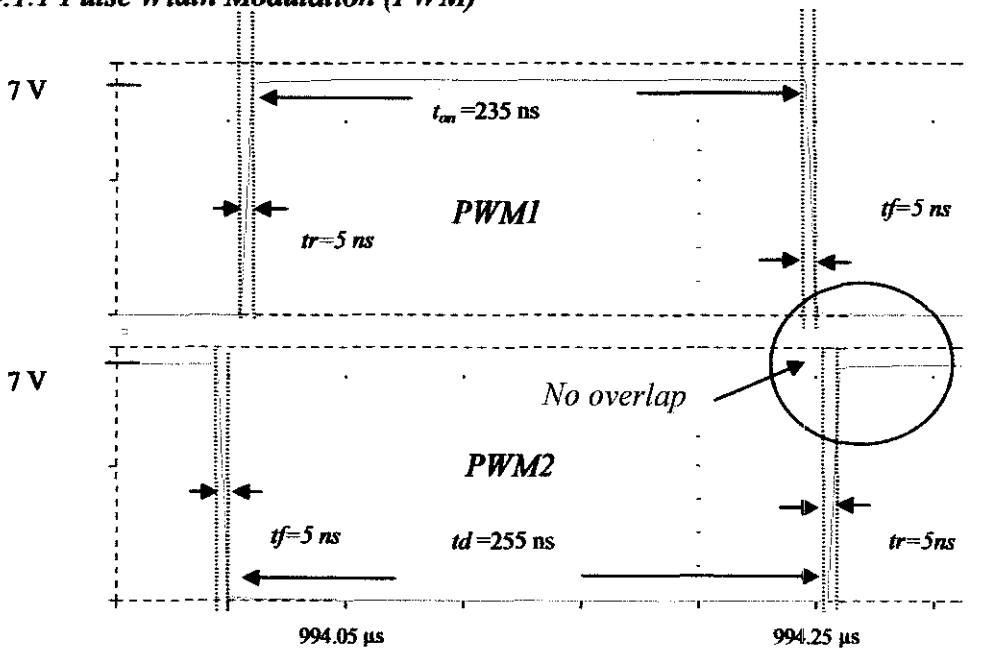

Figure 16: PWM with dead time application

Figure 16 shows the alternating signals between *PWM1* and *PWM2*. By applying *tr*, *tf* and *td*, the total dead time for this alternating signal is 15 ns. In addition, the circle shows no overlap exist between both signals.

Thus, with 15 ns of a dead time, it is sufficient for PWM to generate the signal to the driver without any cross conduction.

In the beginning, the PWM is set to 23.5 % and it is slowly decreased in order to observe the lower duty cycle of gate driver. The t_{on} duration at *PWM1* shown represents the duty cycle of the gate driver at 235 ns. By referring to Eq. (1), the duty cycle for high frequency gate driver is 23.5 %. Therefore, the duration of t_{on} at *PWM2* is 735 ns.

The 15 ns of a dead time is also applied to two different drivers with different value of duty cycle by adjusting the PWM signal at the gate driver. Hence, the summary of the PWM's setting for various value of duty cycle is shown in Table 8 below;

Table 8: PWM's setting for Different Value of Duty Cycle

Duty cycle, *D* at *M1* (%)	23.5	20.0	19.0	18.0	17.0	16.0	15.0	14.0
Pulse width *PWM1* (ns)	235	200	190	180	170	160	150	140
Pulse width *PWM2* (ns)	735	770	780	790	800	810	820	830

When the pulse width at *PWM1* decreases, the pulse width at *PWM2* will increase as shown in Table 8. So the variation of pulse width will result in different value of duty cycle for high frequency gate driver. Even though the duty cycle changes, it is important to ensure there is no overlap occurs between two pulses. Thus, the simulation has verified the PWM's setting before the signals are fed to the drivers.

4.1.2 Conventional Gate Driver (CGD)

4.1.2.1 Node Voltage Output

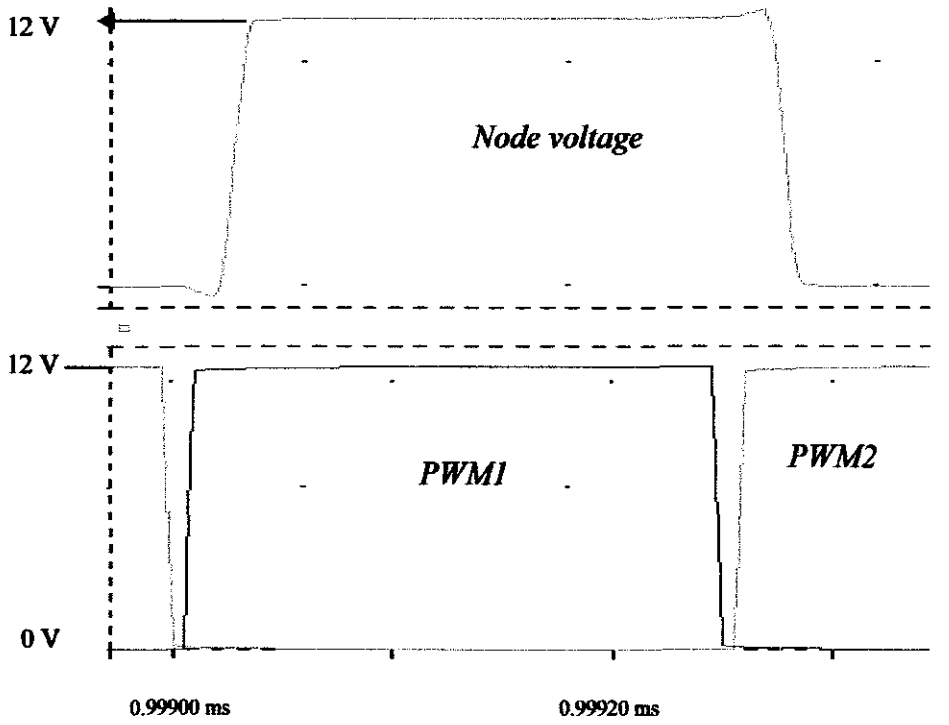

Figure 17: Node Voltage Output with PWM Signal

Node voltage as in Figure 17 shows that the signal starts to turn on when *M1* switch starts triggering. It means, the node voltage pulse is similar to *M1* pulse behavior. Besides, the voltage shown at the node voltage is also similar to the input voltage supply to the gate driver which is 12 V. The pulse from the node voltage is important to supply the sufficient energy to the resultant power MOSFET, *M3*.

4.1.2.2 Body Diode Conduction

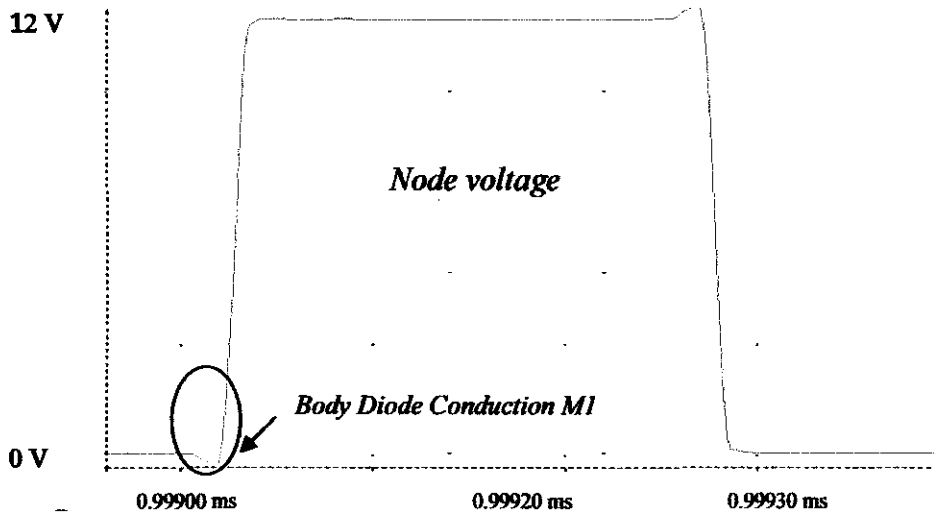

Figure 18: Body Diode Conduction of *M1*=23.5 %

Figure 18 shows the body diode conduction time of *M1* when the switch *M2* turns off for the CGD circuit. It can be seen from the circle in Figure 18 above.

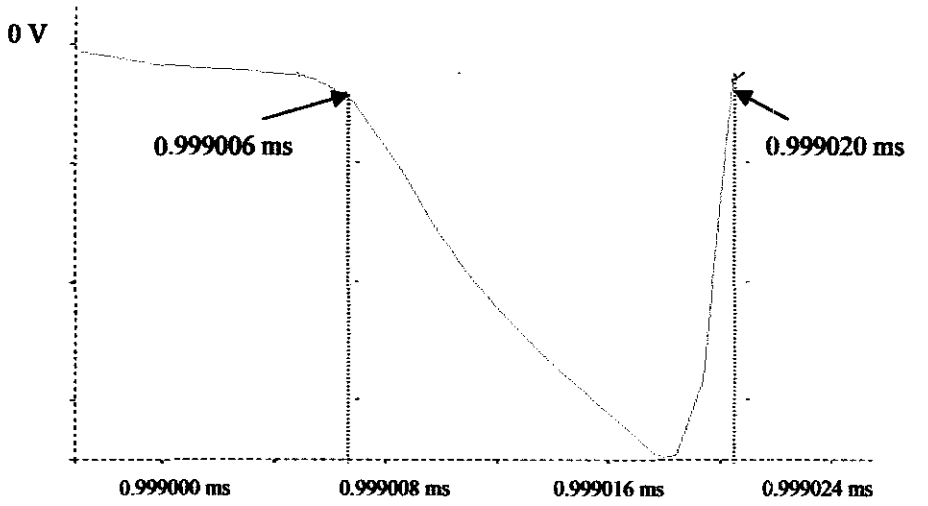

Figure 19: Closed-Up Image Body Diode Conduction Time for CGD at *M1*=23.5 %

Meanwhile, Figure 19 shows the closed-up image from the Figure 18 for body diode conduction time of *M1*. The body diode conduction begins at 0.999006 ms and ends at 0.999020 ms from the Figure 19. Thus, body diode conduction time is 14 ns (0.999020 ms - 0.999006 ms) at *M1*= 23.5 %.

Table 9: Body Diode Conduction Time for CGD

D at *PWM1* (%)	Body Diode Conduction Time (ns)
23.5	14.0
20.0	13.0
19.0	14.0
18.0	14.0
17.0	13.0
16.0	13.0
15.0	13.0

Table 9 above shows the body diode conduction time observed in CGD with different value of duty cycles. It shows the value between 13 ns to 14 ns from 23.5 % to 15 % of duty cycles. That means, the body diode conduction time, *M1* for CGD is less than dead time which is 15 ns.

4.1.2.3 Resultant Power MOSFET, M3

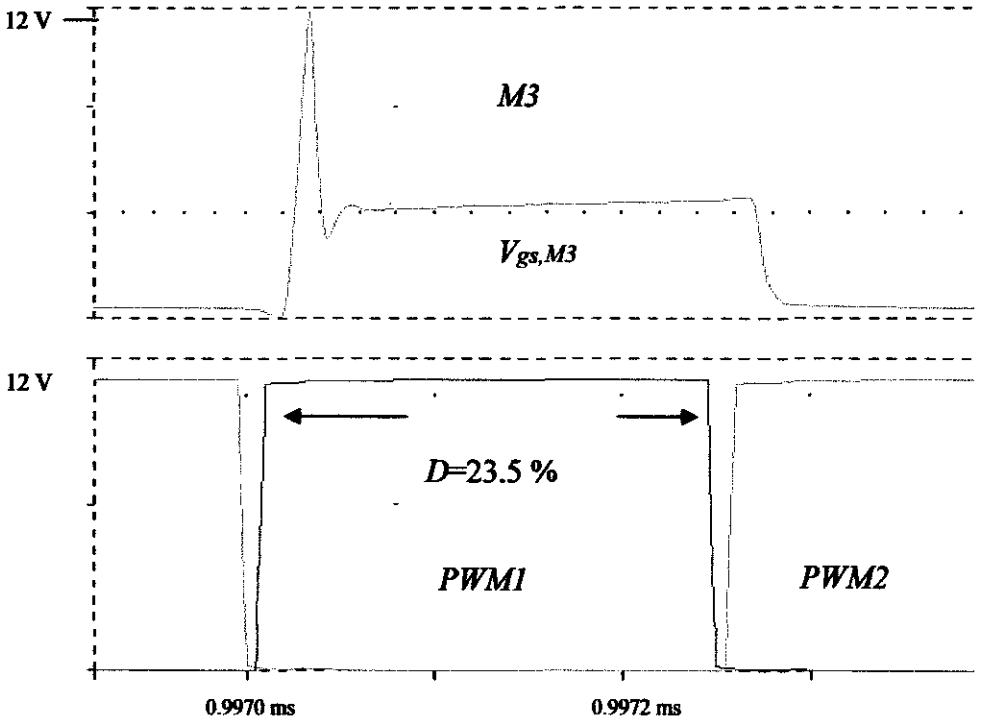

Figure 20: Resultant Power MOSFET for CGD

Figure 20 shows the resultant power MOSFET, *M3* for CGD circuit at *M1* of 23.5 % duty cycle. The *M3* signal is similar to the node voltage whereby it turns on when *PWM1* starts to trigger. It is also known as the gate-source voltage of the *M3* ($V_{gs,M3}$). However, the resultant power MOSFET is an important switch for this circuit in order to complete the operation of the circuit. This is because; the resultant power MOSFET is a main switch to the buck converter that gives a duty cycle value for buck converter operation.

The different value of duty cycle will affect the duty cycle at *M3*. In spite of that, the result for *M3* at CGD and RGD are simplified in Table 10;

Table 10: Duty Cycle at *M3* for CGD

D at *PWM1* (%)	23.50	20.00	19.00	18.00	17.00	16.00	15.00
D at *M3* (%)	14.75	12.43	11.80	11.14	10.46	9.75	9.22

From Table 10, the duty cycle for a high frequency driver at *M1* starts from 23.5 % and results to 14.75 % of duty cycle at *M3*. Then, the duty cycle for the driver will be varied in order to get the lower of duty cycle for the driver, starting from 20 %, 19 %, 18 %, 17 %, 16 % and the lower duty cycle is 15 %. In this situation, every alteration to the duty cycle at *M1* will change the duty cycle at *M3* as shown in Table 10.

The lower duty cycle's setting for CGD in this project is 15 % and results to 9.22 % of *M3*. However, this value is not the targeting value since the duty cycle at *M3* will keep on decreases as duty cycle at *M1* decreases. This is because, the final value of lower duty cycle can be obtained from the buck converter's performance which will be discussed in the section 4.1.4.

4.1.3 Resonant Gate Driver (RGD)

4.1.3.1 Node Voltage Output

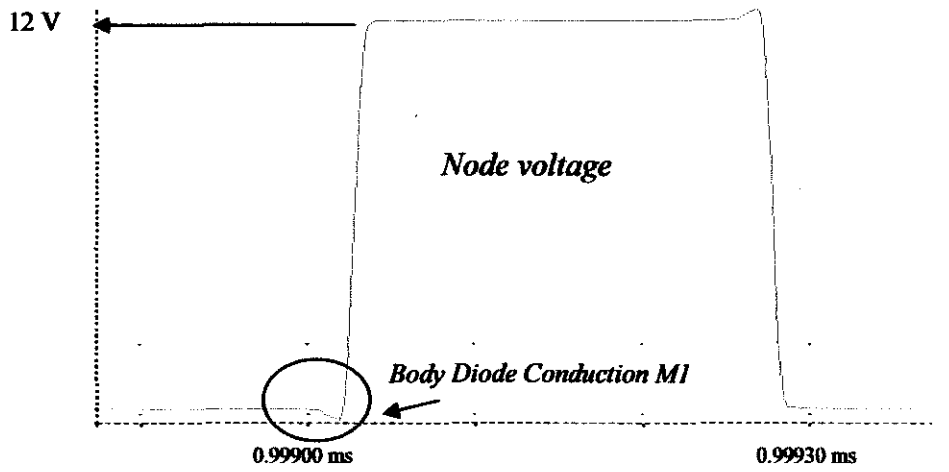

Figure 21: Node Voltage for RGD at *M1*=23.5 %

Most of the simulated node voltage signals have the same pattern for any value of pulse width modulation even though the driver operates in either CGD or RGD. It is proven as shown in Figure 21. From the node voltage, it can be observed that the body diode conduction time of *M1* occurs in the driver, shown in the circle.

4.1.3.2 Body Diode Conduction

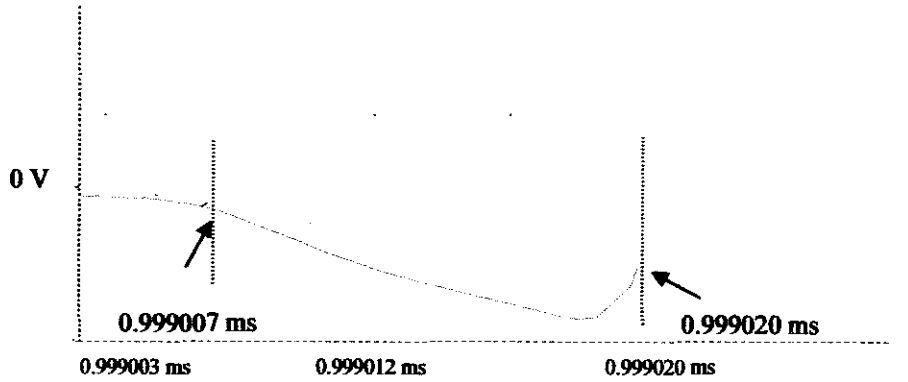

Figure 22: Closed-Up Image Body Diode Conduction Time for RGD at *M1*=23.5 %

The closed-up image for body diode conduction time in RGD with *M1*=23.5 % is shown in Figure 22. It shows the body diode conduction time, *M1* of 13 ns that begins from 0.999007 ms until 0.999020 ms. The body diode conduction time at RGD is 13 ns whereas 14 ns in CGD for *M1*=23.5 %.

Since different duty cycles are applied to *M1*, it affects the result of body diode conduction time. Thus, the body diode conduction time is calculated based on different duty cycles as shown in Table 11.

Table 11: Body Diode Conduction Time for RGD

D at *PWM1* (%)	Body Diode Conduction Time (ns)
23.5	13.0
20.0	14.0
19.0	14.0
18.0	13.0
17.0	13.0
16.0	13.4
15.0	13.4
14.0	14.0

The body diode conduction time for RGD for different duty cycles is shown in Table 11. The values show the body diode conduction time occurred between 13 ns to 14 ns which are similar to CGD. Thus, the body diode conduction is less than dead time which is 15 ns.

For *M1*=23.5 % duty cycle, the body diode conduction time for CGD and RGD is less than dead time as shown in Table 9 and Table 11. Besides, the different value of duty cycle applied to the driver will also affect the body diode conduction time for 15 ns dead time. Thus, the following data tabulated in Table 12 shows body diode conduction time for both drivers at different value of duty cycles at *M1*.

Table 12: Body Diode Conduction Time between CGD and RGD

D at *PWM1* (%)	Body Diode Conduction Time (ns)		Improvement of RGD to CGD (%)
	CGD	RGD	
23.5	14.0	13.0	7.7
20.0	13.0	14.0	7.1
19.0	14.0	14.0	0.0
18.0	14.0	13.0	7.7
17.0	13.0	13.0	0.0
16.0	13.0	13.4	3.0
15.0	13.0	13.4	3.0
14.0	-	14.0	-

Table 12 shows the value for body diode conduction time at different value of duty cycle with 15 ns dead time. It can be noticed that, for any difference in duty cycles applied to the drivers, the body diode conduction for CGD and RGD is between 13 ns to 14 ns which is less than dead time. Besides, the differences between both drivers as shown in Table 12 are acceptable in this project. This is because the difference is within 10 %.

Hence, it shows that the operation of the gate driver is correct based on the node voltage and body conduction time.

4.1.3.3 Maximum Value for L_r

The difference in between conventional gate driver and resonant gate driver is the discharging and charging time operation of the inductor between gate driver and power MOSFET. It is because, the resistor experiences i^2R whereas inductor current is varying with time as shown in Eq. (5).

In order to make the inductor fully charged and discharged within the pulse width, it is important to select the suitable value for the inductor. So, the pulse width will provide sufficient t_{on} of the gate driver. As the value of resonant inductor, iL_r increases, it takes a longer duration of iL_r to conduct. Thus, it will cause the oscillation towards the end of on-time state of *PWM1*.

Based on the theory, the different value of resonant inductor gives different characteristic of the waveform at the specific amount of pulse width. Besides, the graph of *tr* and *trec* is different during the on-state of *PWM1*.

Thus, various value of resonant inductor varying from 15 nH to 30 nH at 23.5 % RGD is used in search of maximum value for L_r, so that, iL_r will be fully charging and discharging within the specific value of pulse width.

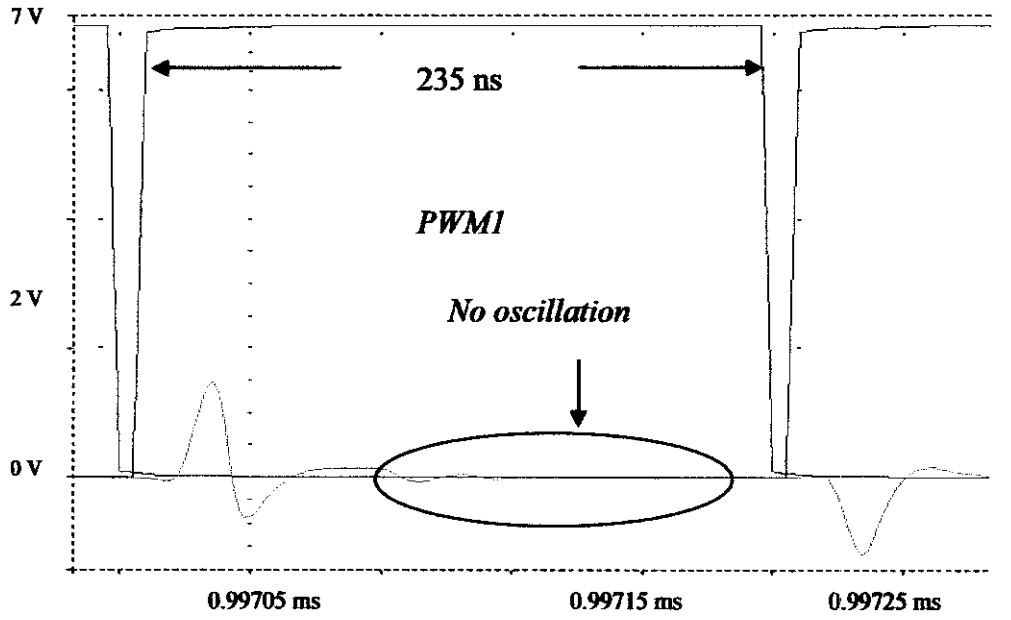

Figure 23: iL_r waveform for L_r = 15 nH

Figure 23 shows iL_r waveform for L_r=15 nH. There is no oscillation inside 235 ns of pulse width. Thus, the value for L_r will be increased to find the maximum value for L_r.

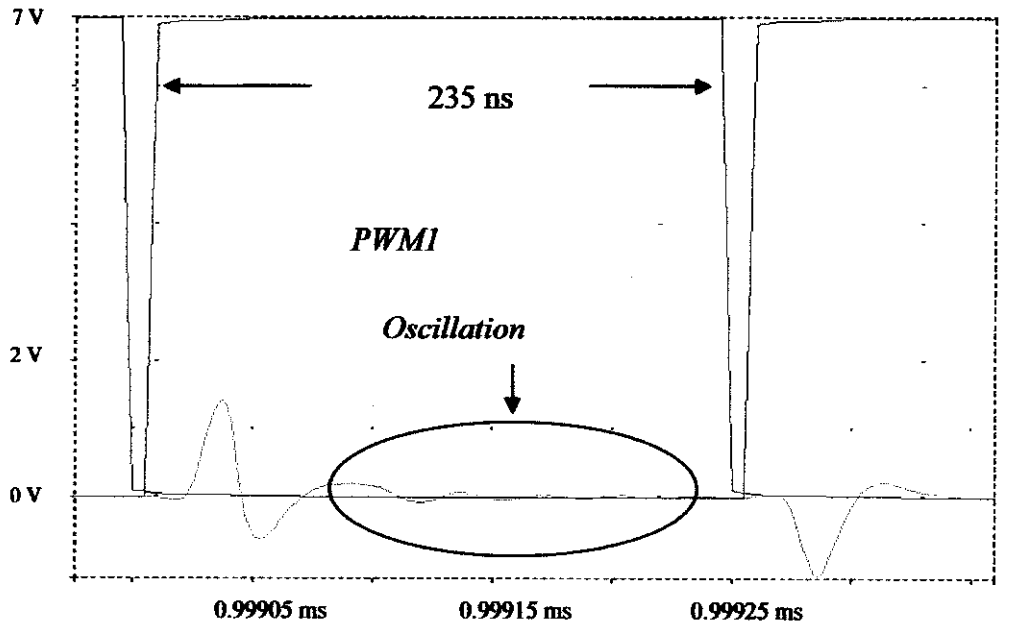

Figure 24: iL_r waveform for L_r = 24 nH

Figure 24 shows the iL_r waveform when L_r = 24 nH at 23.5 %. The iL_r starts to oscillate as shown in the circle. This is because it takes longer time duration to make it stable during discharging within 235 ns window. However the oscillation shows in the circle has just started and smaller.

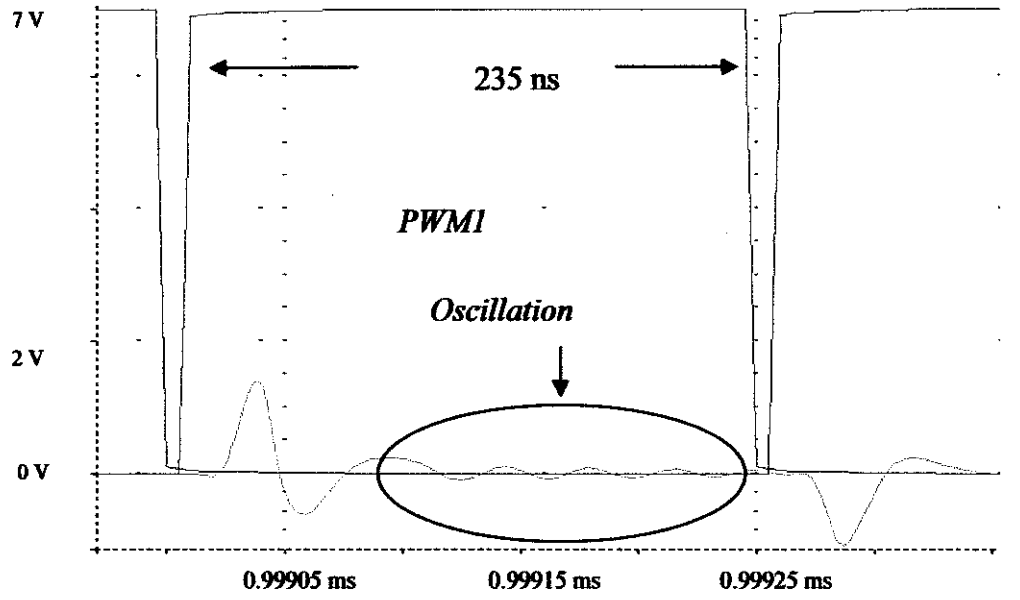

Figure 25: iL_r waveform for L_r = 30 nH

For L_r = 30 nH at the pulse width 235 ns as shown in Figure 25 above, the iL_r shows the oscillation inside the pulse width given. The oscillation shows in the circle is higher compared to L_r = 24 nH. Hence, as the L_r increases there exists oscillation waveform towards the end of on-time state of *PWM1*. For 30 nH, it obviously shows the oscillation inside the pulse. Thus, the higher value of L_r will cause oscillation at the end of the pulse width.

In conclusion, 23 nH is the maximum value of L_r to make the current completely charging and discharging at 235 ns pulse width modulation for RGD. This is because, for L_r equals to 24 nH, the iL_r waveform starts to oscillate inside the pulse width given.

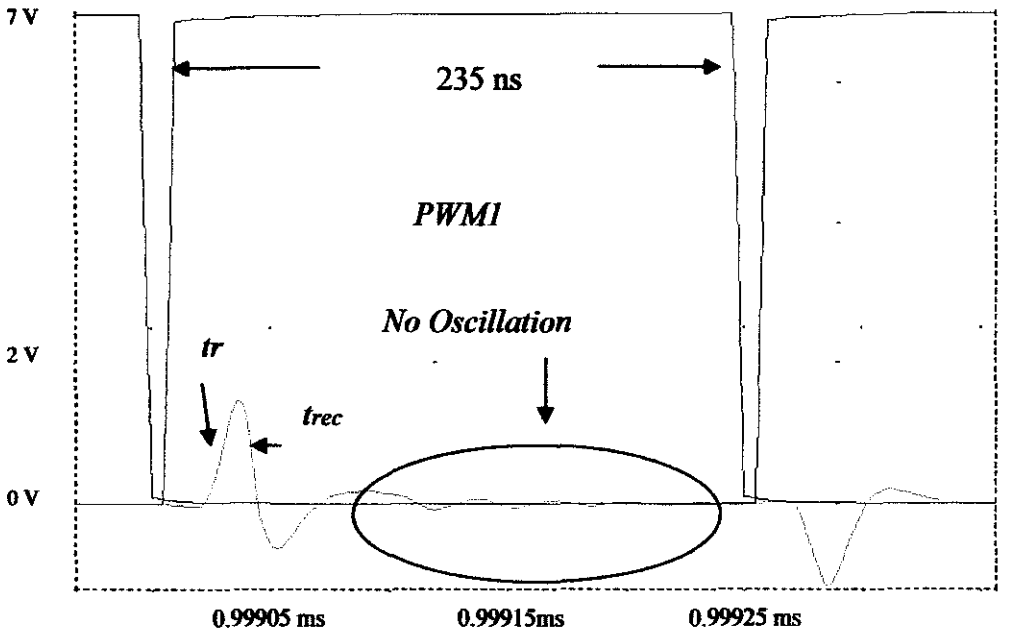

Figure 26: iL_r Waveform with Maximum L_r for RGD at 23.5 %

As shown in Figure 26, when *PWM1* turns on, iL_r starts to charge in L_r represents as *tr*. Mean while, the L_r starts to discharge inside the *PWM1* pulse before the pulse fully turns off. Thus, the recovery time, *trec* is a discharged current of iL_r which requires a considerable amount of time before the *PWM1* turns off.

The 235 ns pulse width at *PWM1* which is 23.5 % of a duty cycle, provides sufficient t_{on} for the gate driver to make iL_r fully charged and discharged with the value of 23 nH. It is shown from the circle in the Figure 26 that there is no oscillation waveform at the end of the iL_r during its t_{off}. So, with 23.5 % of duty cycle at *PWM1* and 15 ns of dead time, it gives sufficient time to the inductor to charge and discharge completely.

4.1.3.4 Resultant power MOSFET, M3

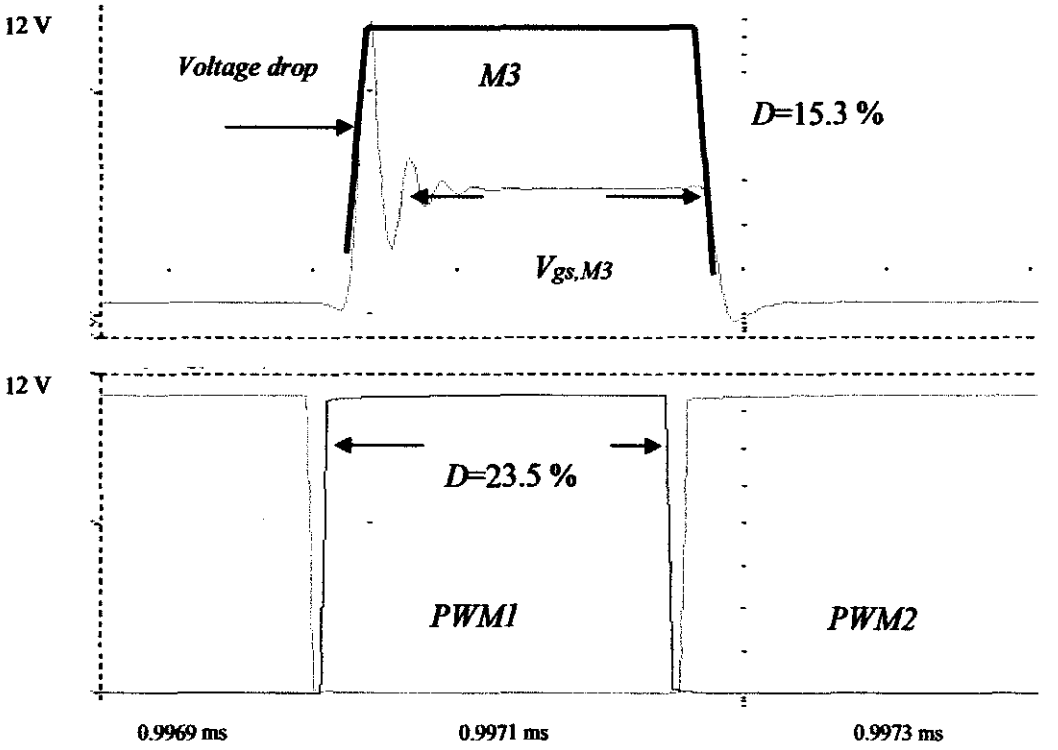

Figure 27: Resultant Power MOSFET for RGD

The resultant power MOSFET, *M3* for RGD as shown in Figure 27 is similar to the *M3* for CGD. For RGD, 23.5 % of *M1* duty cycle gives 15.3 % of duty cycle at *M3*. It is different from CGD which is only 14.7 %. The bolded line shows in Figure 27 is the exact pulse for the *M3* signal. However, the simulation result shows the voltage drop at CGD as well as RGD during the turn on-state of the *M3*. Even though the MOSFET used for this driver is suitable for high switching frequency as shown in the datasheet as attach at APPENDIX B, the switching operation for this MOSFET is still not working properly.

Voltage drop occurs is due to capacitance gate to source inside the power MOSFET. When *PWM1* turns on, the voltage does not charge completely and drop to 5V until the *PWM1* turns off.

Any changes in duty cycle for a high frequency gate driver will affect the duty cycle at *M3*. In spite of that, the result for *M3* at CGD and RGD are simplified in Table 13 below;

Table 13: Duty Cycle at *M3* for RGD

D at *PWM1* (%)	23.50	20.00	19.00	18.00	17.00	16.00	15.00	14.00
D at *M3* (%)	15.32	13.04	11.85	11.80	11.14	10.55	9.88	9.88

From Table 13, the duty cycle for RGD at *M1* starts from 23.5 % and results to 15.32 % of duty cycle at *M3*. Meanwhile, the *M3* duty cycle for CGD gives 14.75 % as shows in Table 10. After that, the duty cycle for RGD will be varied in order to get different value of duty cycle for the driver. Followed by 20 %, 19 %, 18 %, 17 %, 16 %, 15 % and the lowest duty cycle is 14 %. At 15 % of duty cycle at *M1*, it will result to 9.88 % at *M3* which is similar to 14 % of duty cycle at *M1*.

As the duty cycle at *M1* is decreased, the duty cycle at *M3* will be decreased. The lowest duty cycle's setting for RGD is 14 %, but this is not the targeting values similar to CGD. This is because, the final value of duty cycle obtained from the buck converter's performance will be discussed in the section 4.1.4.

4.1.4 Buck Converter's Performance

The different value of duty cycle at *M3* as stated in section 4.1.2.3 and 4.1.3.4 will affect the buck converter's performance. The buck converter's performance consists of output current, I_{out} output voltage, V_{out} and inductor current, *iL* operation mode. So, the lowest duty cycle for high frequency duty cycle can be determined.

From the duty cycle values, all components of a buck converter can be calculated by referring to Eq. (6), Eq. (7) and Eq. (8). Since, the duty cycle at *M3* for CGD and RGD are different, the value for the components of buck converter will also be affected. Thus, the components value at 23.5 % duty cycle of a gate driver is shown in Table 14 and Table 15.

Table 14: Buck Converter Components Value for *M1*=23.5 % (CGD)

Components	**Value**
Duty Ratio *D M3*	14.75 %
Lcrit	1.49 µH
R	3.5 Ω
C	8 µF

Table 15: Buck Converter Components Value for *M1*=23.5 % (RGD)

Components	**Value**
Duty Ratio *D M3*	15.32 %
Lcrit	1.48 µH
R	3.5 Ω
C	3.5 µF

In order to get continuous conduction mode (CCM) operation for buck converter, the inductor value must be higher than critical inductor value. It is because from Eq. (6), *Lcrit* itself represents the minimum value of inductor before the converter enters the discontinuous conduction mode (DCM).

In this simulation, all inductor values selected are approaching 100 % from the critical value. It is because, the difference between *Lcrit* and *L* value is better to be higher to make the converter operates in CCM. Thus, the graph of *iL* for each duty cycle is measured and displayed in this following section.

4.1.4.1 Inductor Current (iL) Operation Mode

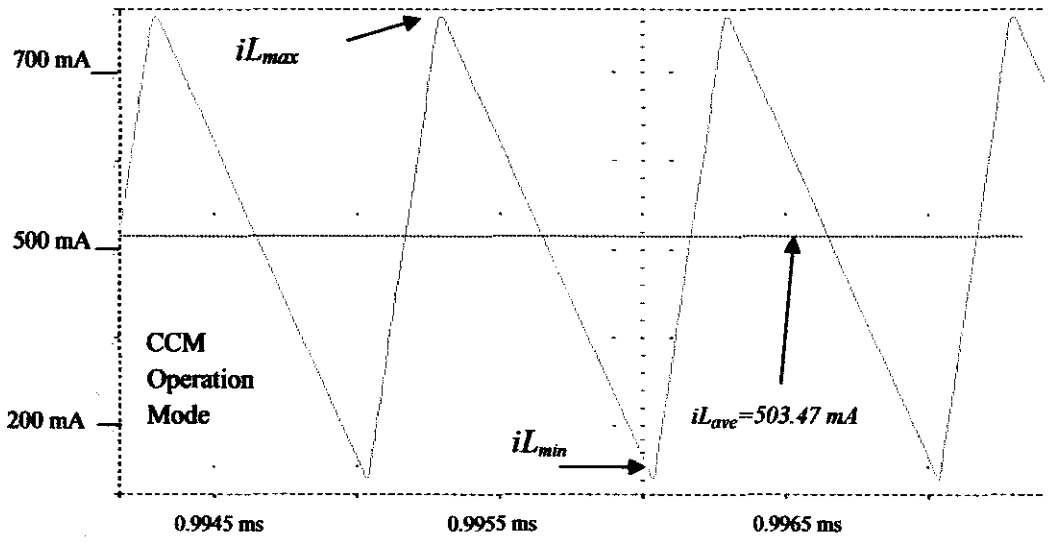

Figure 28: Ripple *iL* of CGD at *M1*=23.5 %, for *R*= 3.5 Ω

The *iL* graph of the buck converter is shown in Figure 28. It shows the triangle waveform from the simulation and the pattern matches theoreticaly. In order to get the iL_{ave} value, the value of iL_{max} and iL_{min} need to be considered. So the result for iL_{ave} of the CGD at *M1*=23.5 % is 503.47 mA. Besides, the graph shows the *iL* operates in CCM mode since it does not return to 0 A.

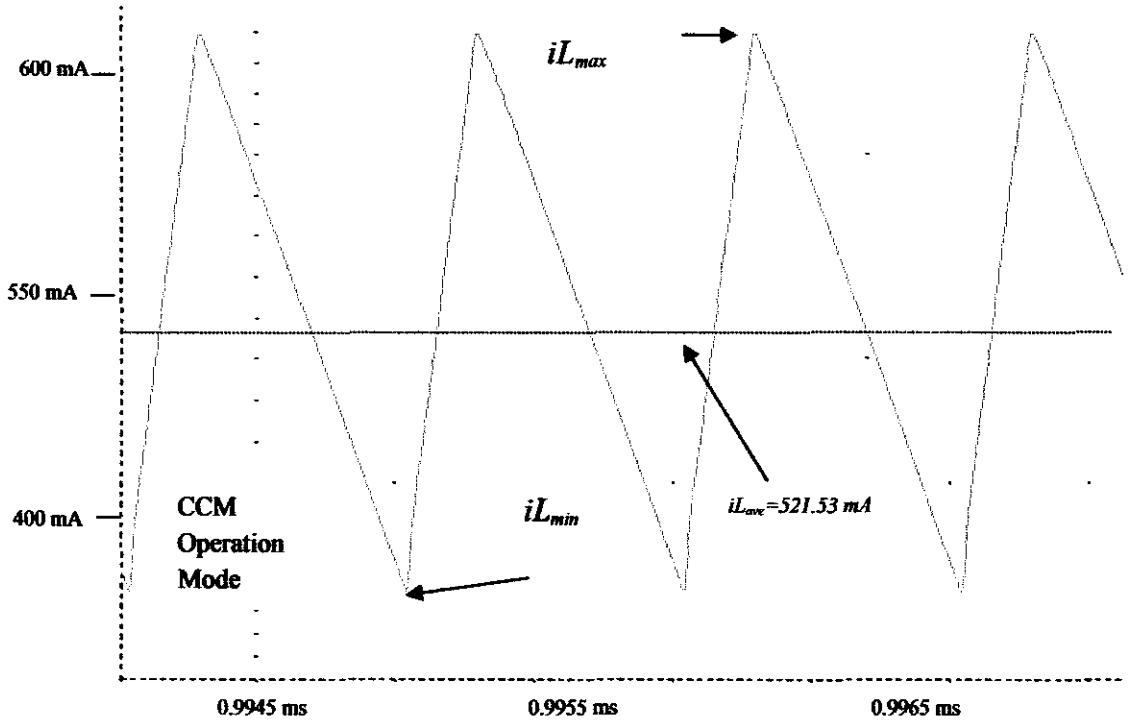

Figure 29: Ripple *iL* of RGD at *MI*=23.5 %, for L_r = 23 nH

Figure 29 shows the ripple *iL* of RGD circuit at *MI*=23.5 %. It shows that, the buck converter is operating in CCM since the *iL* value never goes to 0 V. The average value for *iL* at RGD is 512.53 mV after considering the iL_{max} and iL_{min} values.

The two graphs of CGD (Figure 28) and RGD (Figure 29) for the *iL* of buck converter operate in CCM. However, the value of inductor current of buck converter is different for both drivers. Hence, the value of *iL* and their mode of operations will be shown in Table 16.

Table 16: *iL* value with varies of duty cycle at CGD, for R= 3.5 Ω

D, PWM1 (%)	iL_{max} (mA)	iL_{min} (mA)	iL_{ave} (mA)	Operation Mode
23.5	764.42	242.52	503.47	CCM
20.0	659.00	186.47	422.74	CCM
19.0	615.37	187.69	401.53	CCM
18.0	585.02	171.36	378.19	CCM
17.0	590.95	119.49	355.22	CCM
16.0	634.51	24.84	329.68	CCM
15.0	714.41	-55.94	329.24	DCM

Table 16 shows the iL_{max} and iL_{min} with iL_{ave} for each duty cycle applied at CGD. The iL_{ave} is decreasing as the duty cycle decreases. The operation mode for this buck converter at CGD is CCM unless for duty cycle of 15 %. It is because, the iL_{min} in case of D= 15 % returns to 0 A which is -55.94 mA. Next, the value for each *iL* of the buck converter at RGD is tabulated in Table 17 below.

Table 17: *iL* value with varies of duty cycle at RGD, for L_r =23 nH

D, PWM1 (%)	iL_{max} (mA)	iL_{min} (mA)	iL_{ave} (mA)	Operation Mode
23.5	656.17	386.89	521.53	CCM
20.0	578.70	331.46	455.08	CCM
19.0	663.42	183.99	423.71	CCM
18.0	617.74	182.89	400.32	CCM
17.0	586.63	166.13	376.38	CCM
16.0	598.98	116.47	357.73	CCM
15.0	649.54	17.95	333.75	CCM
14.0	673.53	-38.28	317.63	DCM

The iL_{ave} for the buck converter at RGD decreases when the duty cycle is decreasing as shown in Table 17 above. It is similar with iL_{ave} for the CGD circuit. For RGD, the minimum duty cycle that can be applied to found to be 14 %. In addition, the *iL* operation mode starts at CCM and drops to DCM when duty cycle reaches 14 %.

Theoretically, low duty cycle at buck converter will give better performance. Unfortunately, the 15 % duty cycle at CGD and 14 % at RGD makes the converter operates in DCM. Thus, the 15 % of a duty cycle at CGD and 14 % at RGD are not suitable for the gate driver to operate buck converter.

Table 18: The Summary of the Difference *iL* Between CGD and RGD

D, PWM1 (%)	*iL* at CGD (mA)	*iL* at RGD (mA)	Improvement of RGD to CGD (%)
23.5	503.47	521.53	3.46
20.0	422.74	455.08	7.10
19.0	401.53	423.71	5.23
18.0	378.19	400.32	5.53
17.0	355.22	376.38	5.62
16.0	329.68	357.73	7.84
15.0	329.24	333.75	1.32
14.0	-	317.63	-

Table 18 shows the summary of the *iL* values between CGD and RGD with different duty cycle. The improvement between RGD to CGD will be calculated in order to observe the performance of the buck converter.

It is shown that, the *iL* for RGD is better than CGD since it gives the positive improvement. In addition, when the duty cycle reaches to 15 %, the buck converter operates in DCM and leading to instability for the buck converter's operation. Hence, the lowest duty cycle for the high frequency CGD is 16 % whilst 15 % for RGD.

4.1.5 I_{out} and V_{out} at 16% of Duty Cycle for CGD

The lowest duty cycle for high frequency CGD at *M1* is 16 % and this gives 9.75 % of duty cycle at *M3*. Thus, the I_{out} and V_{out} for buck converter will be focused on this *M3* duty cycle.

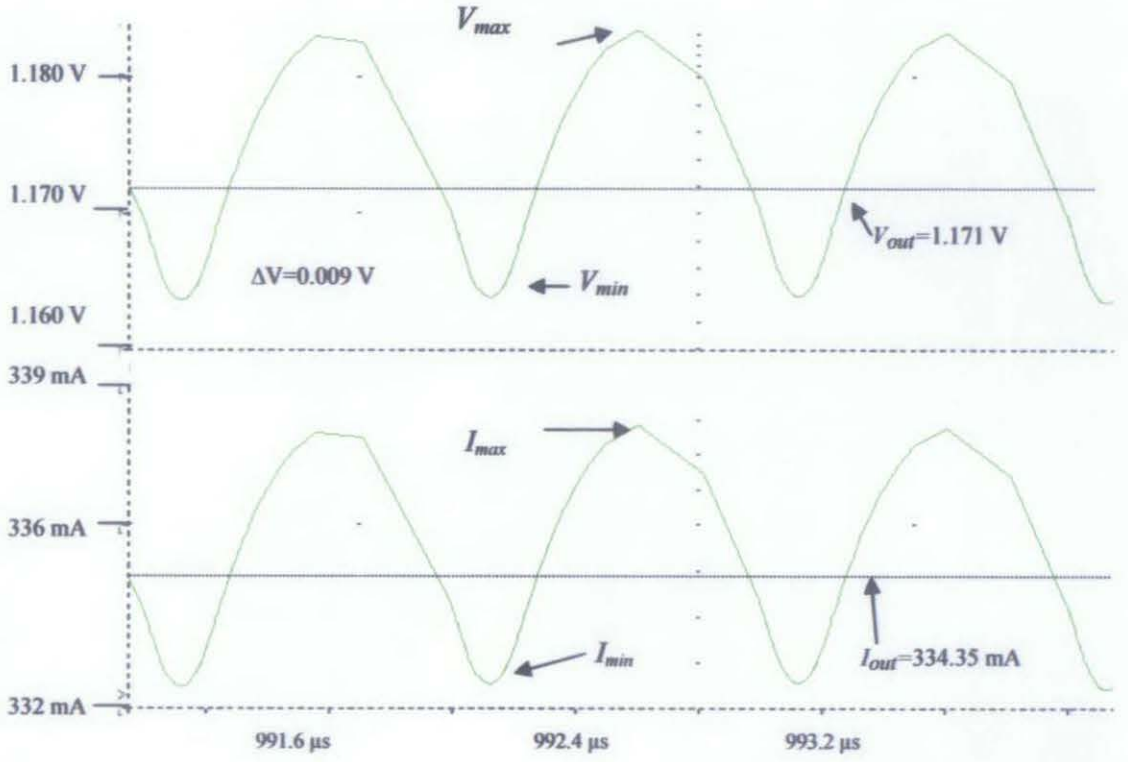

Figure 30: V_{out} *and* I_{out} of Buck Converter for CGD at *M1*=16 %

Figure 30 shows the V_{out} and I_{out} of the buck converter at lowest duty cycle in CGD. There is a ripple voltage and current for the buck converter's output. Hence, the V_{max}, V_{min}, I_{max} and I_{min} can be considered to get the value of V_{out} and I_{out}. The V_{out} is 1.171 V while I_{out} is 334.35 mA. From Eq. (8), the ripple voltage, ΔV for this waveform results to 0.009V.

4.1.6 I_{out} and V_{out} at 15% of Duty Cycle for RGD

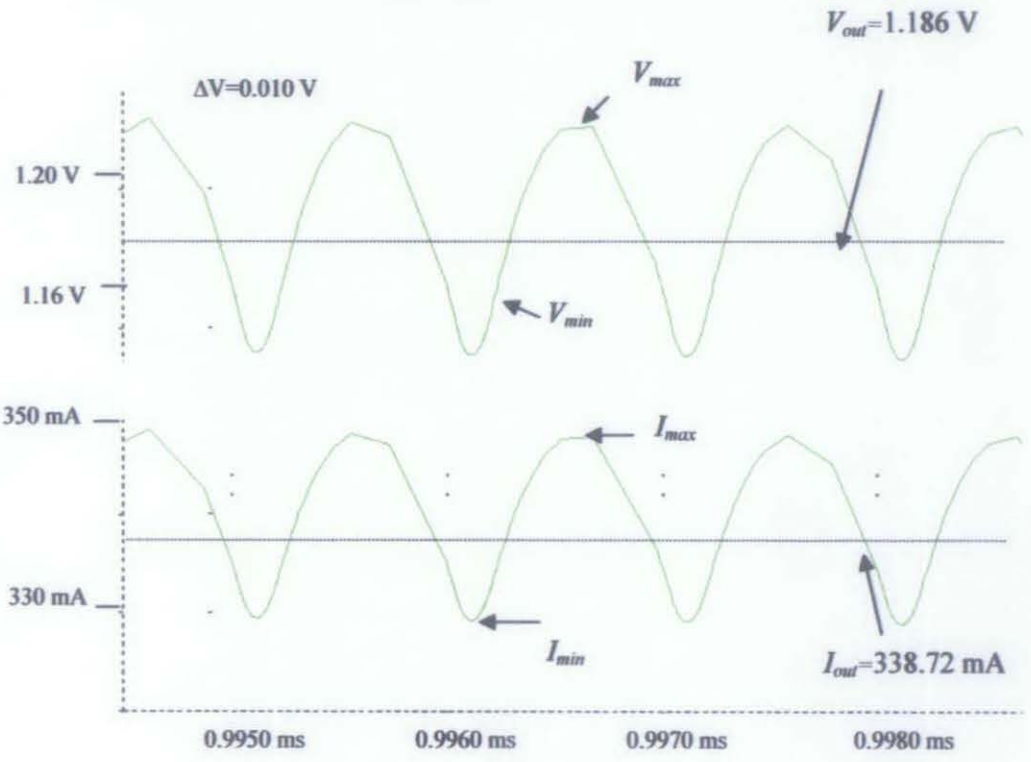

Figure 31: V_{out} *and* I_{out} of Buck Converter for RGD at *M1*=15 %

Then, the buck converter with RGD at *M1*=15 % is evaluated by observing the V_{out} and I_{out} as shown in Figure 31 above. It shows the ripple voltage and ripple current imitate the values at RGD operation. After considering the value of V_{max}, V_{min}, I_{max} and I_{min}, the value for V_{out} and I_{out} can be determined. Thus, the value for the V_{out} is 1.186V and I_{out} is 338.72mA.

Next, the value of V_{out} and I_{out} at RGD and CGD operation are summarized in section 4.1.7 and 4.1.8 at different duty cycle values.

4.1.7 V_{out} for CGD and RGD

Table 19: V_{out} for CGD and RGD at different Duty Cycle of *M1*

D, PWM1 (%)	V_{out} (V)		Improvement RGD to CGD (%)
	CGD	RGD	
23.5	1.770	1.838	3.70
20.0	1.492	1.569	4.90
19.0	1.412	1.422	0.70
18.0	1.337	1.416	5.58
17.0	1.256	1.337	6.06
16.0	1.171	1.266	7.50
15.0	1.107	1.186	6.66
14.0	-	1.185	-

All data for V_{out} at CGD and RGD are recorded as in Table 19 above. The V_{out} for RGD is different with CGD since the V_{out} is depends on duty cycle at *M3* as shows in Eq. (2). However, V_{out} for RGD is better compared to CGD. It is because, the improvement of RGD to CGD gives the positive value. The highest improvement is operated at 15 % of duty cycle, *M1* which is 6.66%. Unfortunately, 15 % of *M1* makes the buck converter operates in DCM. Next, the data from Table 19 is plotted in Figure 32.

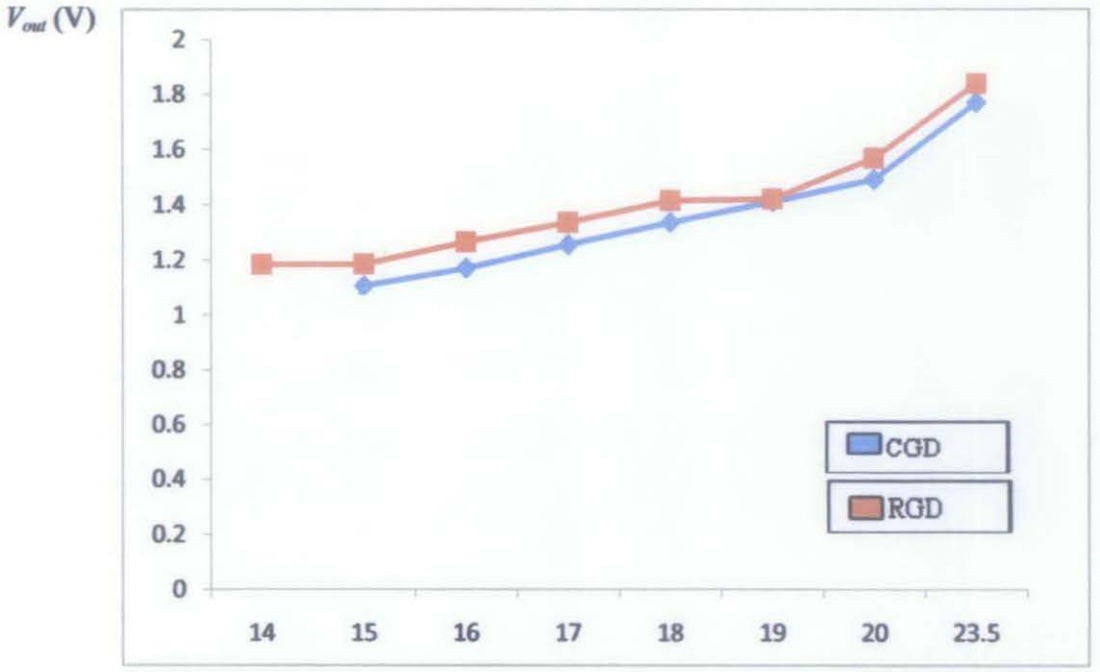

Figure 32: V_{out} VS Duty Cycle, D

Figure 32 shows the V_{out} variation for buck performance with different duty cycle values based on Table 19. The red color indicates V_{out} for buck converter at RGD while the blue color for CGD.

As the duty cycle decreases, the V_{out} will also decrease. This is because, as stated in Eq. (2), V_{out} is inversely proportional to the D with constant input voltage, V_{in} to the buck converter.

4.1.8 I_{out} for CGD and RGD

Table 20: I_{out} for CGD and RGD at different Duty Cycle of *M1*

D, PWM1 (%)	I_{out} (mA)		Improvement RGD to CGD (%)
	CGD	RGD	
23.5	506.47	525.01	3.53
20.0	426.41	448.43	4.91
19.0	409.43	426.93	4.10
18.0	381.89	404.53	5.60
17.0	358.79	381.81	5.84
16.0	334.35	361.63	7.54
15.0	316.25	338.72	6.63
14.0	-	319.61	-

Table 20 shows the result for I_{out} at CGD and RGD with different duty cycle valued at *M1*. The I_{out} of buck converter depends on duty cycle at *M3* for both drivers. The results have shown the good improvement of RGD to CGD from 23.5 % *M1* duty cycle to 14 %. It is can be shown from the positive value of improvement as tabulated in Table 20.

When the duty cycle of *M1* is decreasing, the V_{out} value is decreasing as well as I_{out} as shown in Table 19 and Table 20. When the voltage decreases, the current will also decrease. However, this result is opposed from Eq. (3) which stated that, I_{out} will be higher if the duty cycle is decreasing. Therefore, all the data in Table 20 is plotted in Figure 33.

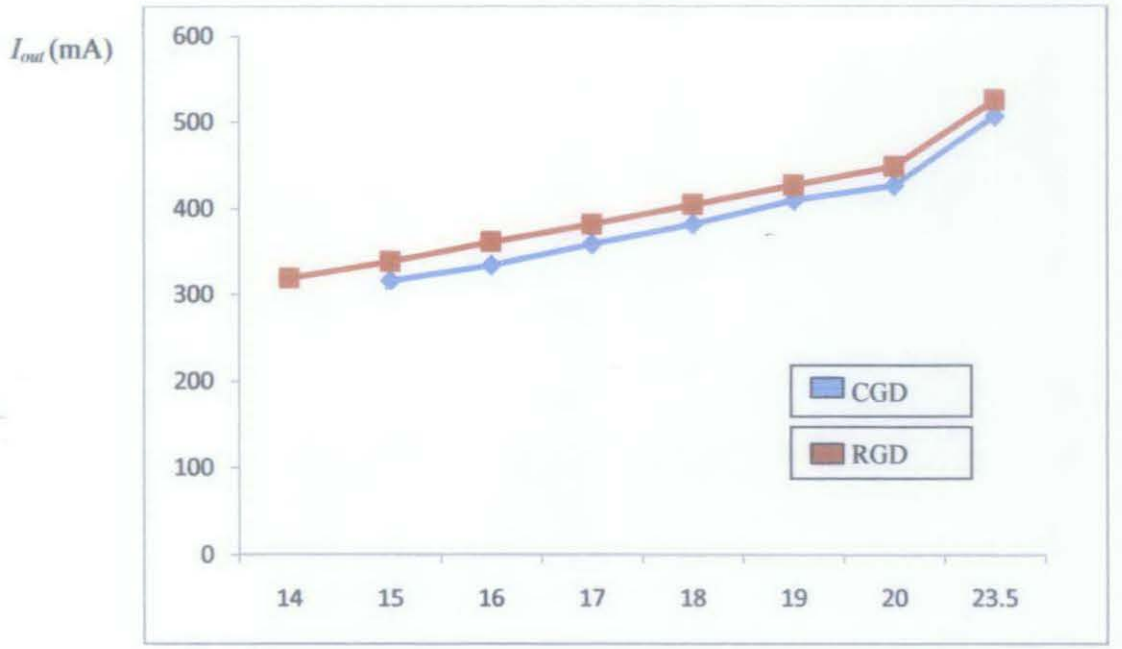

Figure 33: I_{out} VS Duty Cycle, D

Figure 33 shows I_{out} versus duty cycle for buck converter. There is not much difference between CGD and RGD circuit in order to turn on the buck converter as shown in Figure 32 and Figure 33 in terms of their output performance. In addition both figures have same pattern as duty cycle decreases. From V_{out} and I_{out} value as shown in Table 19 and Table 20, the value is decreasing as the duty cycle of *M1* decreasing.

In order to observe the differences between calculation and graph for both output performance, all data are simplified in Table 21 for CGD and Table 22 for RGD shown in the next page.

Table 21: V_{out} and I_{out} Differences for CGD at *M1* Duty Cycle

D, PWM1 (%)	V_{out} (V)		Tolerance (%)	I_{out} (mA)		Tolerance (%)
	Calculated	Graph		Calculated	Graph	
23.5	1.764	1.770	0.34	504.00	506.47	0.49
20.0	1.488	1.492	0.27	425.14	426.41	0.30
19.0	1.410	1.412	0.28	402.86	409.43	1.60
18.0	1.334	1.337	0.22	381.14	381.89	0.20
17.0	1.248	1.256	0.64	356.57	358.79	0.62
16.0	1.165	1.171	0.51	332.86	334.35	0.45
15.0	1.106	1.107	0.09	316.00	316.25	0.08

Table 22: V_{out} and I_{out} Differences for RGD at *M1* Duty Cycle

D, PWM1 (%)	V_{out} (V)		Tolerance (%)	I_{out} (mA)		Tolerance (%)
	Calculated	Graph		Calculated	Graph	
23.5	1.835	1.838	0.16	524.29	525.01	0.14
20.0	1.565	1.569	0.25	447.14	448.43	0.29
19.0	1.420	1.422	0.14	405.71	406.29	0.14
18.0	1.410	1.416	0.42	402.86	404.53	0.41
17.0	1.335	1.337	0.15	381.42	381.81	0.39
16.0	1.265	1.266	0.08	361.43	361.63	0.06
15.0	1.185	1.186	0.08	338.57	338.72	0.04
14.0	1.183	1.185	0.17	338.60	319.61	5.60

The RGD circuit gives better results as shown in Table 21 and Table 22. This can be shown from a low tolerance at RGD either for V_{out} or I_{out} compared to tolerance at CGD. It is because, RGD is designed to improve the CGD performance as mentioned in section 2.2.2. Thus, RGD circuit is the best choice for the buck converter.

Both gate drivers will results to different V_{out} and I_{out} with buck converter's application which is based on duty cycle at *M3*.Therefore, it can be concluded that the lowest duty cycle for CGD is 16 % and 15 % at RGD. Table 23 and Table 24 below show in details the result of low duty cycle for both high frequency gate drivers.

Table 23: Lowest Duty Cycle for CGD

Lower *D* (%)	*M3* (%)	V_{out} (V)	I_{out} (mA)	*iL* (mA)	Operation Mode
16.0	9.75	1.171	334.35	329.68	CCM

Table 24: Lowest Duty Cycle for RGD

Lower *D* (%)	*M3* (%)	V_{out} (V)	I_{out} (mA)	*iL* (mA)	Operation Mode
15.0	9.88	1.185	338.72	333.75	CCM

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

Throughout this project, two types of gate driver have been used to drive buck converter which are CGD and RGD. The both drivers need to operate at low duty cycle in order to observe the impact to the driver and buck converter. Thus, the lowest duty cycle of a CGD has been determined to be 16 % and 15 % for RGD. When both gate drivers operate below these values, the buck converter starts to operate in DCM. The lowest duty cycle of CGD results in 9.75 % of duty cycle at *M3*. As for RGD, 9.88 %.

The 23 nH of L_r has been selected as maximum value for RGD. It is because, when 24 nH is chosen, the oscillation waveform will occur inside the predetermined pulse width during the discharging of the inductor current. Hence, the iL_r does not have a completely charging and discharging.

For every change of duty cycle at *M1* of a gate driver, it will result in different duty cycle at *M3*. Thus, the V_{out}, I_{out} and *iL* operation mode of buck converter will also be changed. In addition, the different duty cycle at *M3* will affect the value of *L* and *C* for buck converter.

5.2 Recommendation

Further analysis could be done on both drivers. Even though the RGD gives better results, more testing should be done in order to verify the analyses. Besides, the power MOSFET used should be chosen correctly to avoid voltage drop at *M3* with lower capacitance gate to source [19]. The performance of the buck converter can be improved if there is no voltage drop at *M3*. In addition, the value of switching frequency should be increased for both drivers for further analyses.

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APPENDIX A1

GANTT CHART

NO	DETAIL/WEEK	1	2	3	4	5	6	7		8	9	10	11	12	13	14	15
1	Progress work continued																
2	Submission of Progress Report																
3	Progress Continued																
4	Draft Report																
5	Final Report (soft Cover)																
6	Technical Paper																
7	Viva																
8	Final Report (Hard Cover)																

APPENDIX A2

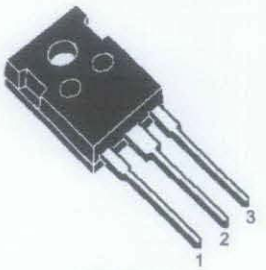
IRFP250 Datasheet

IRFP250

N-CHANNEL 200V - 0.073Ω - 33A TO-247
PowerMesh™ II MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRFP250	200V	< 0.085Ω	33 A

- TYPICAL $R_{DS}(on)$ = 0.073Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED



TO-247

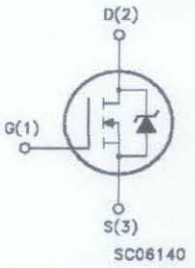
DESCRIPTION

The PowerMESH™ II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns swithing speed, gate charge and ruggedness.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- UNINTERRUPTIBLE POWER SUPPLIES (UPS)
- DC-AC CONVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate- source Voltage	±20	V
I_D	Drain Current (continuos) at T_C = 25°C	33	A
I_D	Drain Current (continuos) at T_C = 100°C	20	A
I_{DM} (•)	Drain Current (pulsed)	132	A
P_{TOT}	Total Dissipation at T_C = 25°C	180	W
	Derating Factor	1.44	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	5	V/ns
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1)I_{SD} ≤33A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.66	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
Rthc-sink	Thermal Resistance Case-sink Typ	0.1	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	33	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	600	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	200			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			50	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 16A		0.073	0.085	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, V_{GS} = 10V	33			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, I_D = 16A	10	25		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2850		pF
C_{oss}	Output Capacitance			420		pF
C_{rss}	Reverse Transfer Capacitance			120		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 100V, I_D =16 A		25		ns
t_r	Rise Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 3)		50		ns
Q_g	Total Gate Charge	V_{DD} = 160V, I_D = 33 A,		117	158	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10V, R_G = 4.7Ω		15		nC
Q_{gd}	Gate-Drain Charge			50		nC

SWITCHING OFF

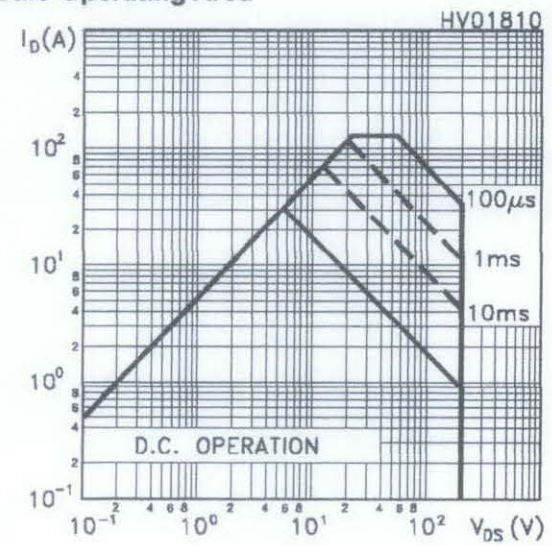
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 160V, I_D = 16 A,		60		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		40		ns
t_c	Cross-over Time			100		ns

SOURCE DRAIN DIODE

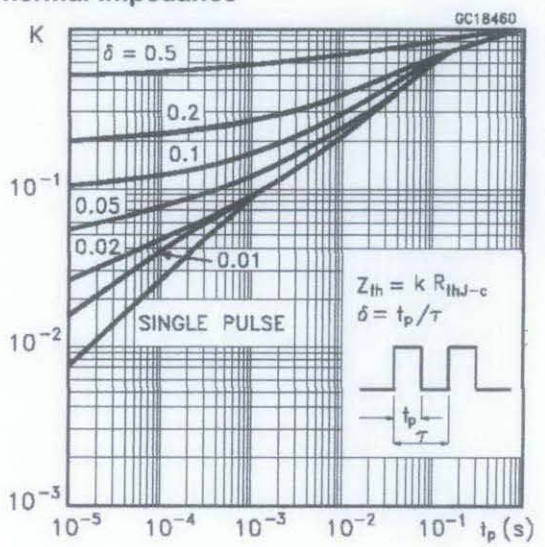
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				33	A
I_{SDM} (2)	Source-drain Current (pulsed)				132	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 33 A, V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 33 A, di/dt = 100A/µs,		370		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 100V, T_j = 150°C (see test circuit, Figure 5)		5.4		µC
I_{RRM}	Reverse Recovery Current			29		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

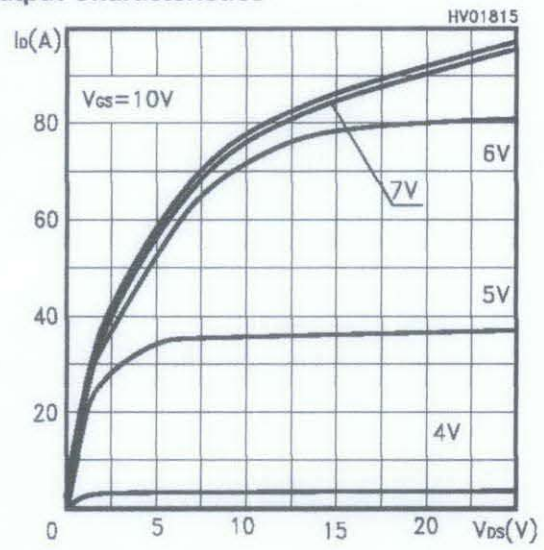
Safe Operating Area



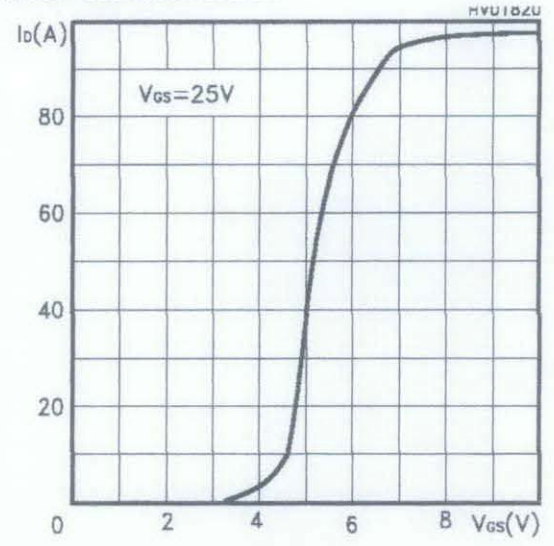
Thermal Impedance



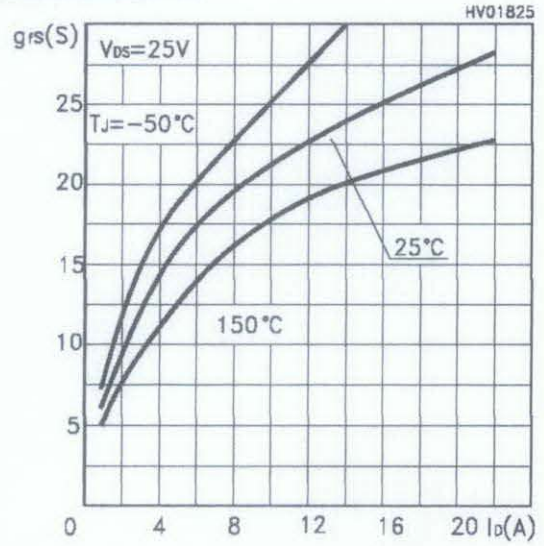
Output Characteristics



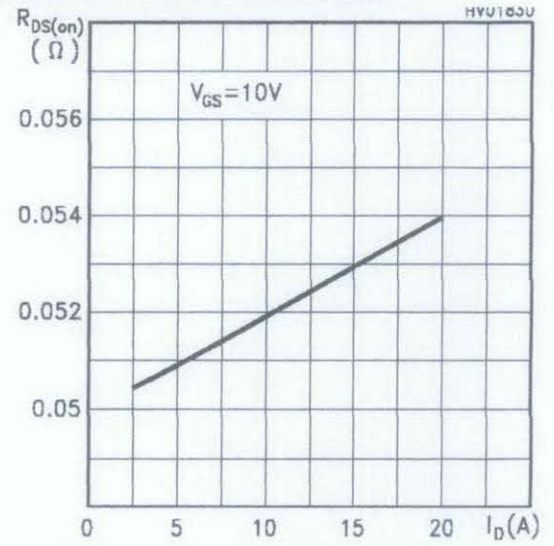
Tranfer Characteristics



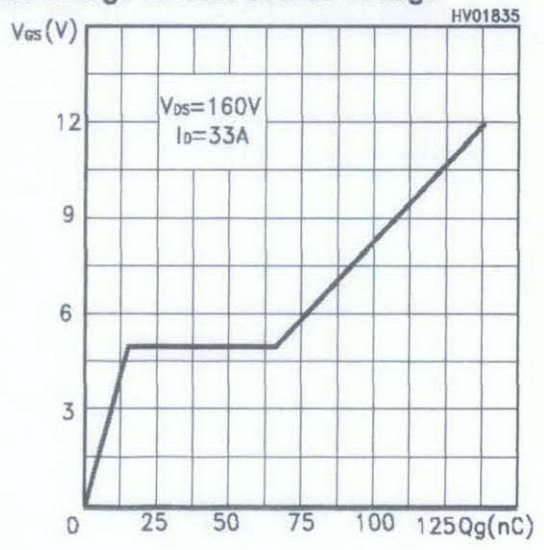
Tranconductance



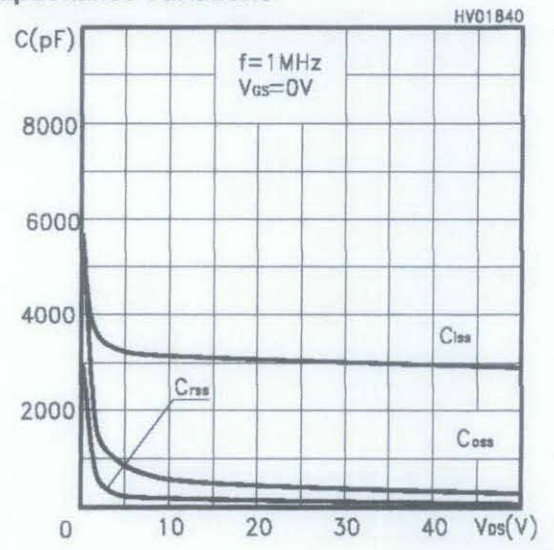
Static Drain-Source On Resistance



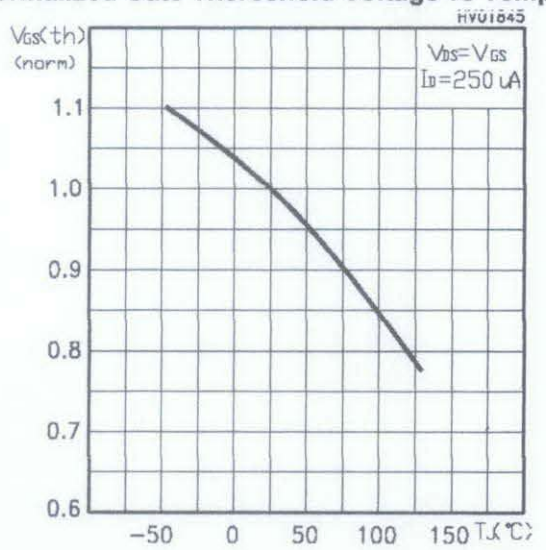
Gate Charge vs Gate-source Voltage



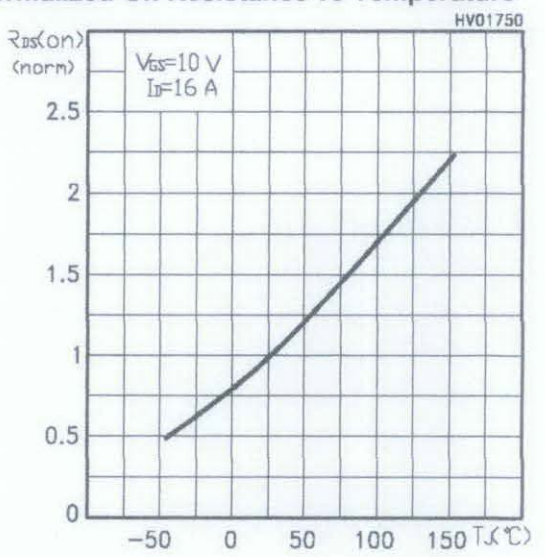
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

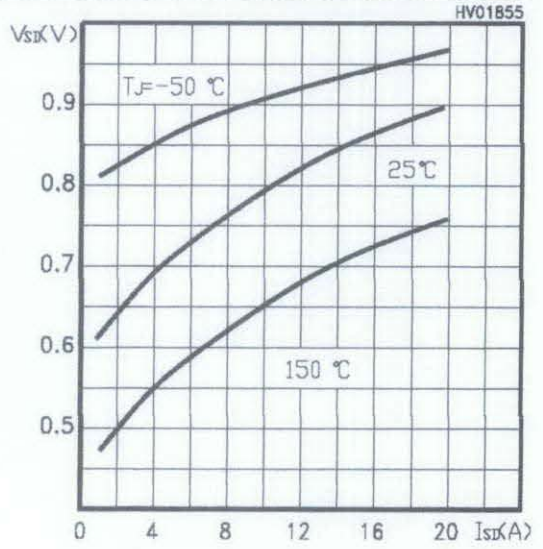


Fig. 1: Unclamped Inductive Load Test Circuit

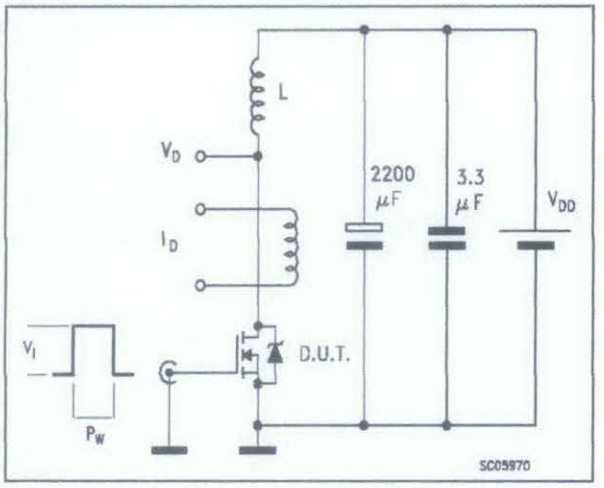


Fig. 2: Unclamped Inductive Waveform

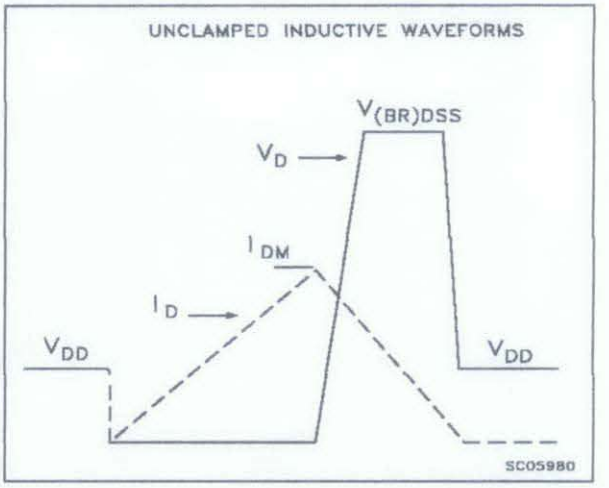


Fig. 3: Switching Times Test Circuit For Resistive Load

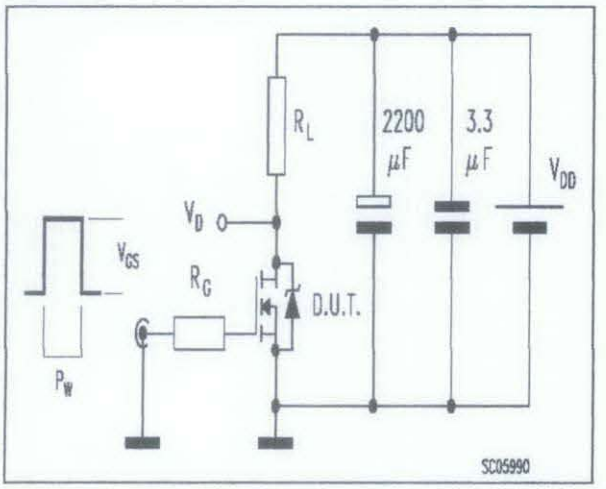


Fig. 4: Gate Charge test Circuit

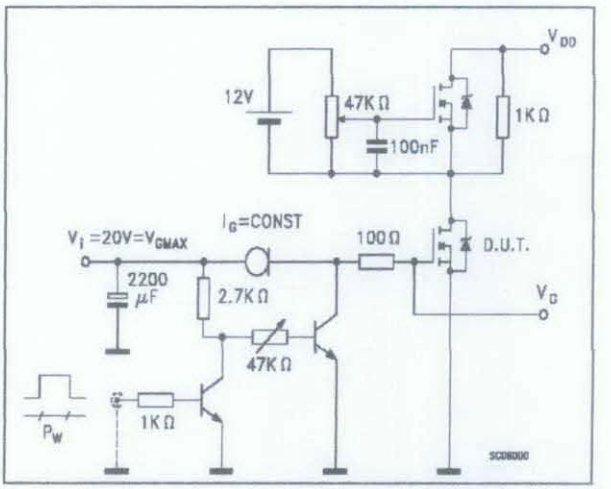
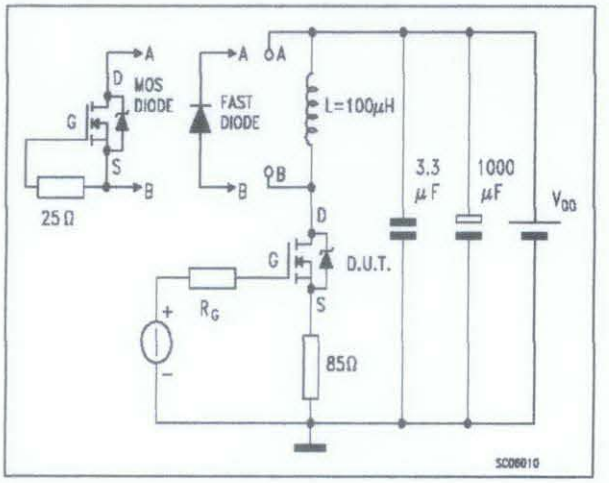


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118