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THE STUDY AND ANALYSIS OF MPPT CONTROLLER FOR SRBC

By

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FINAL REPORT

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CERTIFICATION OF APPROVAL

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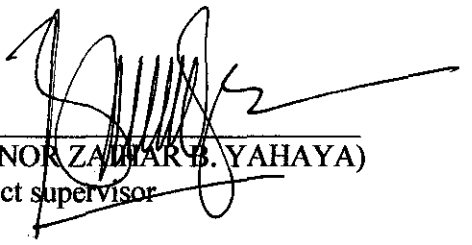
Approved by,



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MAY 2011

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

AHMAD AFIFY AFZAN BIN ABU ZAMIR

ABSTRACT

This work is about designing Maximum Power Point Tracker (MPPT) with Synchronous Rectifier Buck Converter (SRBC) circuit where the main purpose is to improve the performance and increase the output voltage and current. The MPPT controller controls the output current of the input (usually solar array) so that the output power converges on the maximum based on the linearity between the maximum output power and the optimal current. In this work, MPPT's characteristics, performance, operation modes, advantages, and disadvantages are analyzed and observed. Then, combination of MPPT and adaptive gate drive (AGD) will be applied to SRBC as the output circuit. PSPICE software is used in designing and simulating both circuits. The comparison is carried out based on the average output voltage and current, node voltage, output ripple voltage and current, gate-to-source voltage, and body diode conduction loss of the MPPT circuit and MPPT with AGD circuit. The details are discussed thoroughly that include limitations and advantages in the design of the controllers using 1 MHz switching frequency. It is found that by implementing MPPT controller with SRBC, the output voltage and output current have increased by approximately 12 % - 13 % for both CCM and DCM conditions. Besides that, it also reduces output voltage ripple and current around 70 % for CCM mode. However, in DCM condition, the output peak-to-peak ripple for both voltage and current have increased by 20 %.

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First and foremost, I would like to praise to Allah the Almighty for His guidance and time given to me for completing this course. With His guidance and blessings upon me, I managed to overcome all obstacles in completing this project. Here, I would like to use this opportunity to express my heartfelt thanks to everyone that has contributed to the completion of this project.

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CHAPTER 1
INTRODUCTION

1.1 Background of Study

Maximum Power Point Tracker (MPPT) controller is widely used in the photovoltaic (PV) solar panel applications. It extracts maximum power from PV panels and delivers to the load or a battery. The advantages of MPPT controller have triggered the idea to implement and integrate it with SRBC in order to study the outcome and performance. The application circuit used in this project is the Synchronous Rectifier Buck Converter (SRBC) since it is widely used in industry for lower power conversion, power management and microprocessor voltage-regulator (VRM) applications. By driving this project, the significant differences between SRBC and the combination of MPPT and SRBC can be used as benchmark in proposing new solutions to solve some of the SRBC issues. This work is also intended to perform analysis of the controller implemented on the SRBC, to look for its advantages, disadvantages and drawbacks that affect the overall performance. Significant differences and comparison between conventional SRBC and the new combination of MPPT and SRBC will also be studied.

1.2 Research Rationale

In this work the resultant outputs such as the output voltage and current, body diode conduction losses, and output ripple peak-to-peak for both voltage and current are observed based on the implementation of SRBC with MPPT controller. MPPT is chosen in this project because it is seldom used for SRBC application, thus this work is more about the study and observation of its behavior

and characteristics. All effects for example switching characteristics, node voltage and resultant outputs of the combination of SRBC with MPPT will be analyzed and compared to the conventional SRBC. Besides, this project also can show which circuit combination could give better performance for high frequency converter design.

1.2.1 Problem Statement

The new combination of MPPT controller with SRBC will be studied for its effectiveness even though the controller is seldom applied with SRBC. Besides that, SRBC's performance decreases when it operates at high frequency range due to excessive power loss. Looking into this problem, MPPT controller is introduced to improve the performance of the converter and increase the output voltage and current. MPPT controller will be designed and analysis regarding the performance will be done. By analyzing all related issues as well as advantages and disadvantages, this can lead to a proper solution which can contribute to the improvement of the converter.

1.3 Objective

Upon completing this project, few objectives will be achieved. The objectives are as follows:

- To understand the theory and concept of the gate driver and MPPT controller.
- To design MPPT controller and apply the controller and adaptive control technique to the SRBC circuit.
- To perform simulation of the circuits using PSPICE.
- To analyze the advantages and disadvantages of the controller.

1.4 Scope of Study

The study is divided into 3 major stages as follows:

- Literature Review

  In the literature review stage, the information regarding SRBC, MPPT controller and AGD are gathered and studied.

- Construction and Simulation of the circuit

  At this stage, the circuit of MPPT controller will be constructed. Then, it will be integrated with the SRBC before the simulation of the overall circuit using PSPICE can be carried out according to the specific input and output voltage and also the switching frequency.

- Analysis and Performance

  The results obtained from the simulation will be analyzed and concluded. Then, the performance assessment will be conducted according to the simulation test results.

- Fixed value for inductor (L_1), capacitor (C_1) and resistor (R_1) for CCM and DCM conditions.

- Switching frequency = 1 Mhz

CHAPTER 2
LITERATURE REVIEW

2.1 Pulse Width Modulation (PWM)

In power electronics applications, the pulse width modulation (PWM) principle is commonly used for controlling power converters. Most of the power converters apply PWM technique as the gate driver which is used to drive the MOSFET to either ON or OFF state to achieve the desired input.

There are few types of PWM techniques. The common technique used is known as equal-pulse PWM technique. It is used to generate an equal pulse width by comparing the triangular waveform voltage, *Vtri* with a constant direct current (DC) reference voltage, *Vref* [1].

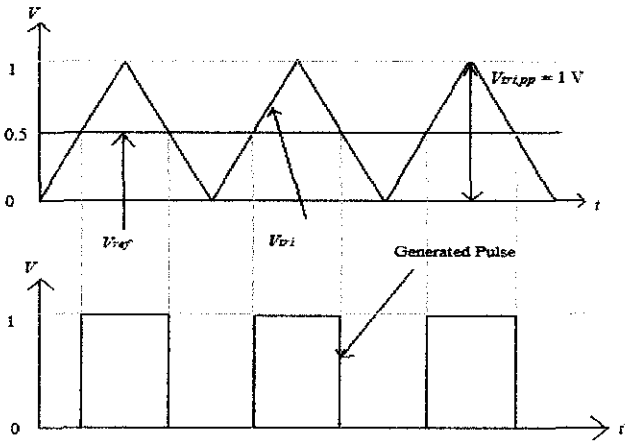

Figure 1: Example of PWM signal

For this type of pulse modulator, the pulse width can be varied by varying the *Vref* and the output voltage generated by the comparator depends on the swing voltage applied to the comparator. For example, if the swing voltage is from 0 V to 1 V, the comparator will generate 1 V when *Vtri* is greater than *Vref* and 0 V when *Vtri* is less than *Vref*. This is illustrated in the Figure 1. Next, Figure 2 shows the Pulse Modulator circuit.

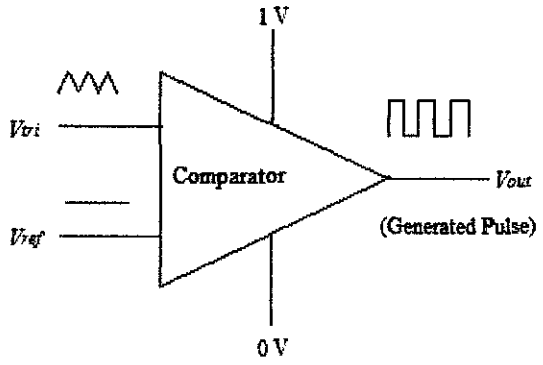

Figure 2: Operation of comparator in generating pulses

It is clear that the *Vref* determines the frequency of the output. Besides that, the PWM signal can be generated using the combinational logic circuits in digital circuit.

In driving MOSFET switch, an accurate design of PWM is required especially for the gate driver application because the range of the gate voltage has to be above its threshold voltage so that it can turn on with sufficient charge. However, when it comes to high frequency switching, for example in megahertz, the output of the PWM usually contains high harmonic distortion and noise making the design more complex.

2.2 MPPT controller

MPPT is an acronym of Maximum Power Point Tracker which is an electronic DC to DC converter that has been widely used in the photovoltaic solar panel applications. It takes the DC input from the solar panels, changes it to high frequency AC and converts it back to a different DC current to match with the batteries. This is a solely electronic tracking system and not concerned with the panel system at all. It uses standard switch-mode power supply technologies with the combination of switching transistors, diodes, capacitors and some control algorithms. The controller's circuit is shown in Figure 3.

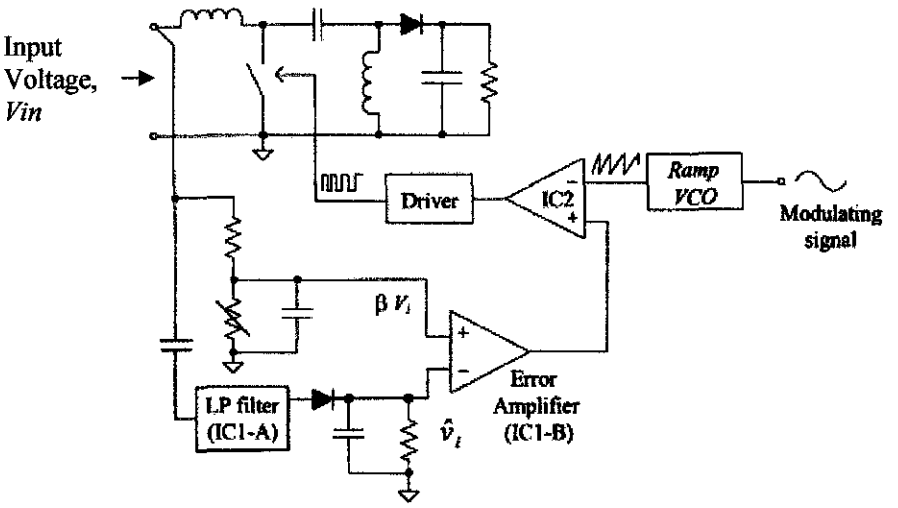

Figure 3: MPPT controller circuit [2]

MPPT will take the maximum power from the input at any time irrespective of the weather and it is a controller which quickly charges the maximum power obtained by the MPPT control while maintaining the electric capacity which input can generate at that time. The MPPT controller controls the output current of the input (usually solar array) so that the output power converges on the maximum based on the linearity between the maximum output power and the optimal current [3]. Most MPPT charge controllers are based on either the buck converter (step-down), boost convert (step-up) or buck-boost converter setup [4].

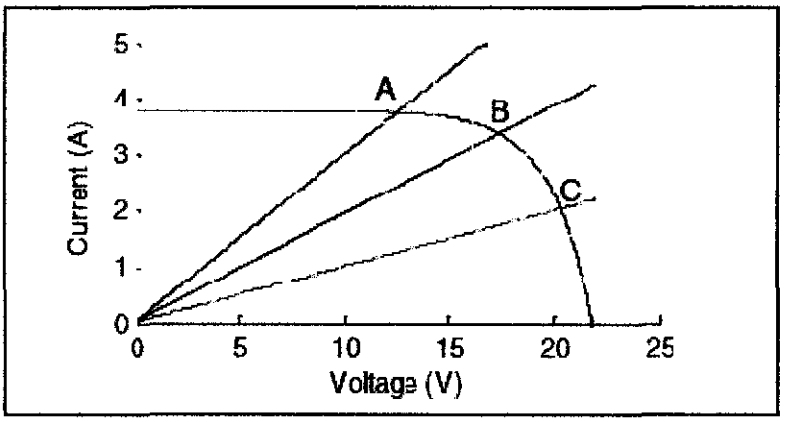

Figure 4: The adjustment principal of MPPT [5]

The usual approach for maximizing the power drawn from Photovoltaic panels under varying atmospheric conditions is to use a MPPT algorithm that provides a reference current or voltage for the power electronic converter that interface the PV array to a battery or load. Figure 4 shows the principal of MPPT. The operation point of the PV array may be point A or point C when it is connected to a battery or load directly and the PV array will work at point B through the MPPT technology.

According to the maximum power transfer theory, the power delivered to the load is maximum when the source internal impedance matches the load impedance [6]. For the system to operate at or close to the maximum power point of the solar panel, the impedance seen from the input of the MPPT needs to match the internal impedance of the solar panel. Since the impedance seen by the MPPT is a function of voltage (V = I * R), the main function of the MPPT is to adjust the solar panel output voltage to a value at which the panel supplies the maximum energy to the load.

There are two main groups of MPPT:

1) MPPT that uses analog circuitry and classical feedback control
2) MPPT that uses a microprocessor to maintain control of the operating point.

Analog systems have the advantage of having low cost components, but are more problematic to control. It is difficult to develop a stable system which is able to maintain its accuracy even under extreme operating conditions such as the wide temperature variations that occur in an outdoor vehicle.

The digitally controlled MPPT systems have the advantage that a power point tracking algorithm will not be influenced by changes in temperature and therefore will always be very reliable. Additionally, the use of an algorithm allows for additional control modes to cope with certain system states such as a fully charged battery buffer. The digital controller also allows for operational data logging to monitor system behavior and performance.

Various MPPT methods and techniques have been proposed in recent years such as Perturb and Observe (P&O) method, Incremental conductance technique (ICT), MPPT using short circuit current of PV-module, MPPT method using open circuit voltage of PV-module, curve fitting technique, hill climbing method and others. Here, some issues and advantages of selected MPPT methods are presented in Table 1.

Table 1: Summary of selected MPPT methods

Description of MPPT methods	Issues	Advantages
Perturb and Observe (P&O) method [7,8]	–Unsuitable for applications in rapidly changing atmospheric condition	– Not requiring solar panel characteristics – Relatively simple control algorithm
Incremental conductance technique (ICT) [9,10]	– Increased in whole system cost because associated with a microcomputer or digital signal processing(DSP) –Response speed of tracking maximum power point (MPP) is declined because calculation time of DSP is increased by relatively complicated control algorithm.	– Among the most accurate compare to other methods – Good performance under rapidly changing conditions
MPPT using short circuit current of PV-module [11]	– Complicated control circuit – Conduction loss and cost of MPPT increased due to added switch and diode to sample the short circuit current of PV-module	– Fast response speed of tracking MPP under rapidly changing atmospheric condition
MPPT method using open circuit voltage of PV-module [12]	– Considerable error power always occurs because the output voltage of PV-module only follows the unchanged reference voltage during one sampling period.	– Very simple control circuit because does not use DSP – Cost efficient

2.3 Dead Time or Time Translation

Dead time, T_D is the duration when both switches are turn-off at the same time. The switches can be MOSFET, IGBT or other ideal switches. It has advantages and disadvantages depending on the applied duration. When both switches conduct complimentarily, it will produce the waveform as shown in Figure 5.

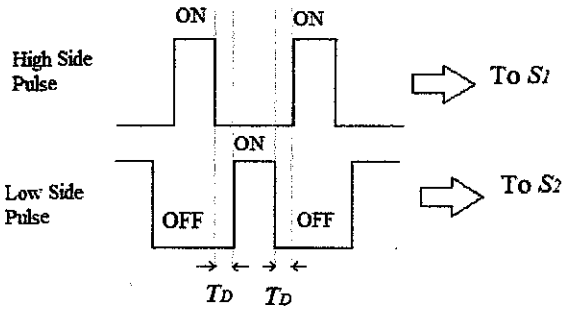

Figure 5: Dead time timing chart

Depending on its applied duration, T_D has its own advantages and disadvantages. T_D is among the important parameters in designing a gate drive because it relates with the total losses. If T_D is too short, it will cause simultaneous conduction of the control switch, S_1 and the synchronous rectifier, S_2 [13]. On the other hand, if T_D is too long, it will introduce losses due to the body diode conduction [14] and may also add a subinterval of negative voltage to node switch which tends to reduce average of drain voltage of S_2 switch. Furthermore, T_D can also be used to avoid shoot through currents in converter with SRBC. Further discussion regarding the effects of T_D such as body diode conduction will be discussed in section 2.6. Unlike dead time, cross conduction occurs when the switches are fully or partially turn-on. It provides a path for current to shoot through from supplied voltage to ground. The cross conduction will lead to power dissipation in both switches.

Various dead-time adjusting techniques and controllers have been developed such as dynamic dead-time controller, sensorless dead-time controller, load dependent dead-time controller and many more.

Table 2: Summary of selected dead-time adjusting techniques and controllers

	Application	Issues	Advantages
sensorless optimization of dead-time[13]	– digital controller implementation	– Complex digital algorithm to search the optimal dead time through a long period, which is not suitable for portable analogue power converters.	– it requires no additional analog components or modifications of standard gate-drive circuitry
analog Dead-Time Locked-Loops (DTLL) [15]	– low voltage application for achieving fast dead time error rejection and low steady-state switching losses	– Complex algorithm	– allow quick and accurate adjustments of the dead time
dynamic dead-time controller [16]	– many applications because it has optimal value under different load conditions	– Complex circuit which contains dead-time detector, finite state machine and dead-time adjustor	– Dead time is automatically adjusted to the optimal values under different load conditions, which minimizes the loss due to body diode conduction and thus improve the power efficiency by 6.5%.
Digital Delay-Locked-Loop (DLL) [17]	– Unsuitable for applications with frequent load variations such as microprocessor	– Poor transient performance, requiring numerous switching cycles to reach steady state	– Robust scheme – Higher output current and efficiency compare to adaptive technique

2.4 Power Electronics Converter Circuit

A power electronics converter is commonly used to convert one form of electrical power to another form (such as alternating current, AC or direct current, DC). There are many applications of converter in our daily life, for example, DC-DC converters are used in cellular phones, laptop computers and DC motor drives. The most common and basic converters used are:

a. Boost converter (step-up)
b. Buck converter (step-down)
c. Buck-boost converter (step-down / step-up)

2.4.1 Synchronous Rectifier Buck Converter

The modified version of buck converter is synchronous buck converter (SBC) or sometimes known as synchronous buck rectifier converter (SRBC). The diode in the basic buck circuit is replaced with a second switch, M_2. By replacing the diode with a switch, the efficiency of the SRBC is more than the conventional buck converter. Figure 6 below shows a SRBC circuit.

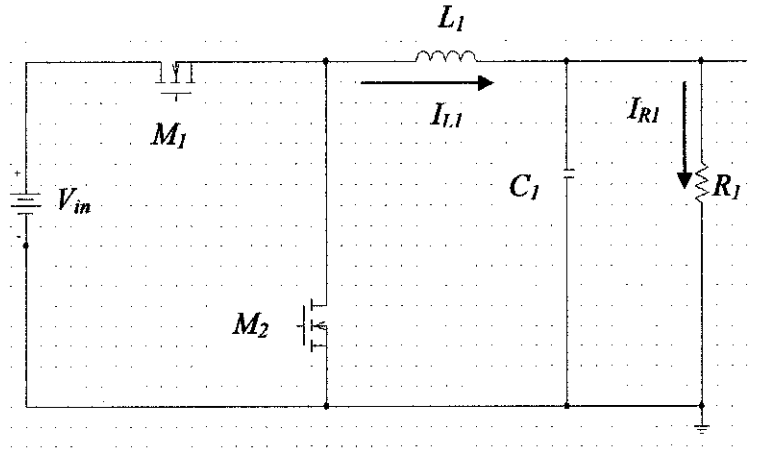

Figure 6: Synchronous Rectifier Buck Converter circuit

The advantages of using SRBC compared to buck converter are:

a) It allows bidirectional power flow.

b) Increased in efficiency because on-state voltage drops of M_2 is less than forward voltage of diode.

Meanwhile, having diode replaced with M_2, may also decrease the performance of the converter at light load where it allows I_{LI} from entering the Discontinuous Conduction Mode (DCM) and maintaining operation in Continuous Conduction Mode (CCM). This means that the SRBC can operate at higher switching frequency but will produce lower performance at low output power. Furthermore, the lower switch typically costs more than the freewheeling diode in the basic buck converter circuit. The complexity of the converter is vastly increased due to the need for a complementary-output switch driver [18].

2.4.1.1 Conduction Mode

The operation of the SRBC is not so complicated, only with an inductor and two switches that control the inductor. It alternates between connecting the inductor to source voltage (to store energy in the inductor) and discharging the inductor into the load.

1) Continuous Conduction Mode (CCM) means that the current in the energy transfer inductor never goes to zero between switching cycles. The inductor current cannot be instantaneously interrupted. When there is one switch is switched, it will result in a sudden change in the inductor current [1].
2) Discontinuous conduction mode (DCM) occurs when the current through the inductor falls to zero during part of the period. The only difference compared to CCM is that the inductor is completely discharged at the end of the commutation cycle [18].

2.5 Adaptive Gate Drive (AGD)

Figure 7 shows Adaptive Gate Drive (AGD) scheme. This technique of gate driver control scheme was introduced to overcome the limitation in the Fixed Duty Ratio (FDR) which is the first PWM controller for synchronous rectifier converter circuit. The advantage of FDR is that it has a simple control circuit. However, when the switching frequency increases, finite T_D associated with the fixed scheme starts to become a significant part of the switching cycle, making the performance to decrease drastically.

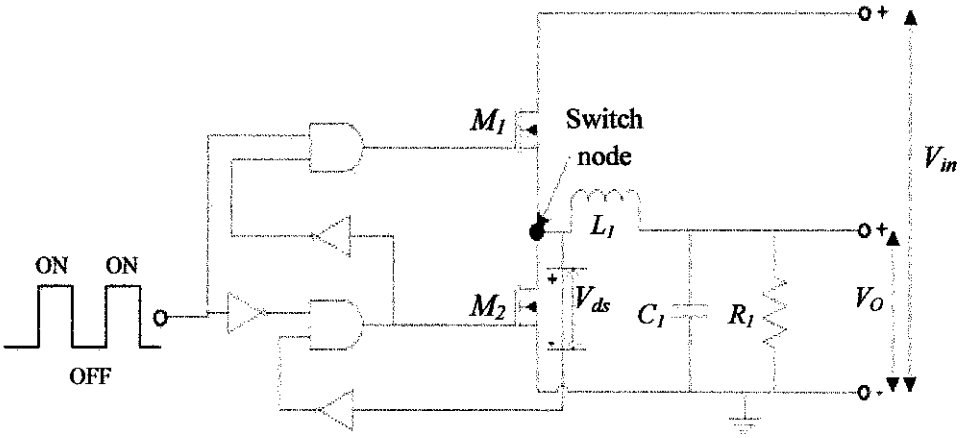

Figure 7: Adaptive Gate Drive (AGD) scheme

To improve the performance of the power conversion, T_D has to be minimized as possible. However it could not be too small since it can bring damage to the component. AGD uses a control loop that includes a digital delay line where it senses the drain to source voltage, V_{ds} of the M_2 and adjusts the digital delay line according to the amount of delay that should be applied to turn on M_2 [19]. Consequently, M_2 is turned on only when the switch node voltage equals to zero.

The advantage of using AGD is that adjustment of the delay can be made adaptively according to the type of MOSFET. On the other hand, the disadvantage is variation of body diode conduction time interval due to the logic components that are used as the feedback.

2.6 Body Diode Conduction

Body diode conduction occurs when negative voltage occurs at Node Voltage, V_{node}. When M_1 and M_2 are off, parasitic body diode of M_2 is forward biased and eventually will generate an undershoot of negative voltage [20]. This body diode conduction is related proportionally with the dead time, T_D. If the dead time is longer, the body diode will also be longer. Allowing the output current to flow through the body diode of the SRBC will degrade the overall efficiency because it will contribute to the body diode losses, P_{bd}. These losses are proportional to the body diode conduction time. The longer the conduction time, the more conduction losses will occur. Thus, a shorter T_D is required in order to have a low body diode loss, P_{bd}. The effect of body diode conduction is shown in Figure 8.

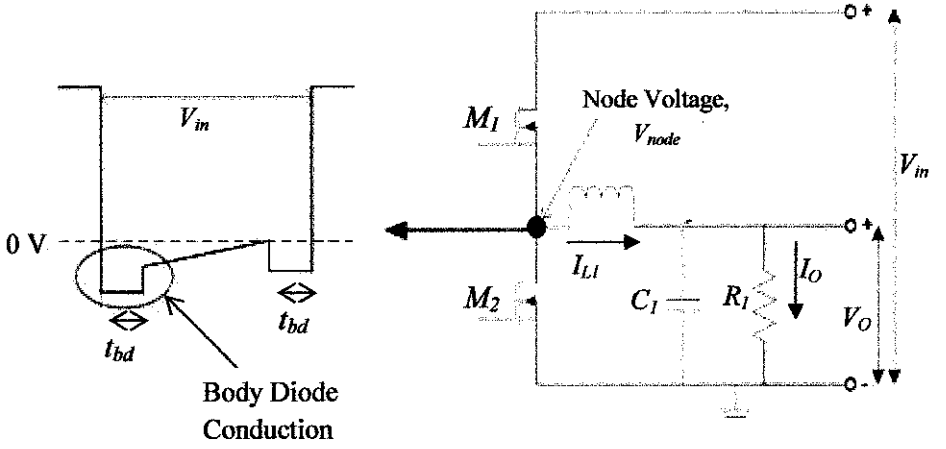

Figure 8: Effect of Body Diode Conduction [20].

The equation to calculate the loss contributed by the body diode conduction:

$$P_{BD} = 2t_{bd} \times V_f \times I_o \times f_{sw} \quad (1)$$

assuming that $t_{bd(rise)} = t_{bd(fall)}$

where: V_f= body diode forward voltage drop

I_O = output current

f_{sw} = switching frequency

t_{bd}= body diode conduction time

CHAPTER 3

METHODOLOGY

3.1 Procedure Identification

The project is about study and research on MPPT controller and construction of MPPT with SRBC circuit and MPPT and AGD with SRBC. The work then proceeds with the simulation work and analysis on the results. The Gantt chart is attached in Appendix A and the overall design methodology throughout this project is shown in Figure 9 below:

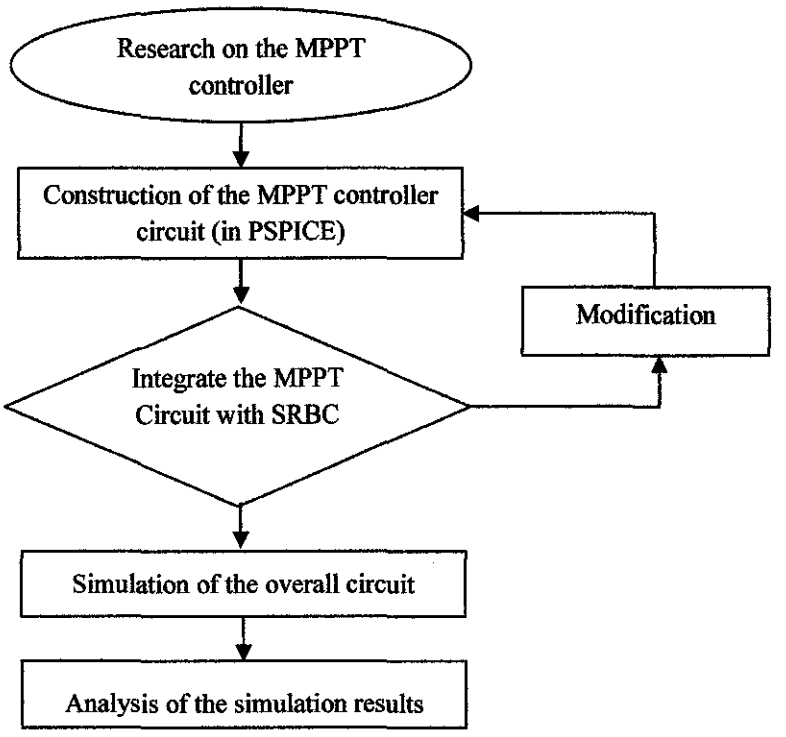

Figure 9: Flow chart of the methodology used in this work.

3.2 Tools and Software Required

The project is mainly based on research and simulation work. Thus, there is no specific tool or equipment required. The simulation will be done using PSPICE circuit simulator. The detail about the PSPICE software used is stated in Table 3.

Table 3: Details about PSPICE Software.

Name	PSPICE
Version	9.2
Build	225
Developer	Cadence Design System Inc.

3.3 Research

Throughout this project, a lot of research needs to be carried out regarding the theory, basic operation and concept for SRBC and MPPT controller. All information such as advantages and disadvantages, related waveforms, issues and associated techniques in designing the controller are gathered from journals, internet and thesis. This step is very essential and crucial to gain the full overview of the project, understand the basic concept, and investigate the issues raised. Further research has also been done on the improvement and performances of the controller and this will be based on the application circuit, the SRBC.

3.4 Circuit design

In this project, SRBC and MPPT controller are designed. All related topologies, selection of suitable components, parameters and calculations will be determined. Here, the designed are based on the specifications as follows:

a) $D = 0.25$

b) V_{in}=12 V

c) V_O= 3 V

d) Switching frequency, f_s = 1 MHz

The purpose having SRBC circuit as the application circuit is because this circuit is widely used in industry for lower power conversion applications. In this project, circuits that will be designed are:

a) SRBC

b) MPPT controller with SRBC

c) MPPT controller and AGD with SRBC

3.4.1 Circuits schematics

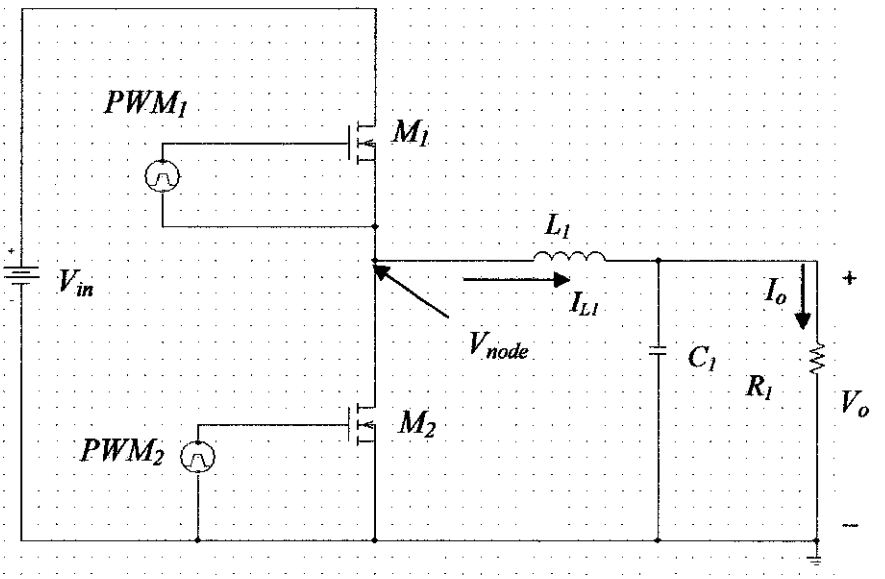

Figure 10: SRBC circuit schematic

SRBC schematic is shown as in Figure 10. The PWM setting for both M_1 and M_2 are based on Table 6. The value of inductor, capacitor and resistor for this circuit are calculated based on the design Eq. (2) to Eq. (7) [1].

$$\text{Inductor voltage,} V_{L1} = L1\frac{di}{dt} = V_{in} - V_o \quad (2)$$

$$\text{Output Ripple voltage,} \Delta V_{L1}(t) = \frac{\Delta I_{L1}(t) T_S}{8C_1} \quad (3)$$

$$\text{Inductor ripple current,} \Delta I_{L1}(t) = 8C_1 f_s . \Delta V_{L1}(t) \quad (4)$$

$$\text{Output inductor, } L_1 \geq DT_S \frac{V_{in} - V_o}{\Delta I_{L1}(t)} \quad (5)$$

$$\text{Output capacitor,} C_1 = \frac{\Delta I_{L1}}{8 f_s \Delta V_o} \quad (6)$$

$$\text{Output filter cut-off frequency, } f_c = \frac{1}{2\pi\sqrt{L_1 C_1}} \quad (7)$$

After that, the circuit is simulated and the voltage node, output voltage, current and also the inductor current are observed. Voltage node is observed to ensure the PWM or switching pulses are generated correctly. Meanwhile for the output voltage and current are measured based on their average values. Then the inductor current is obtained to check the operation of the SRBC whether it is in CCM or DCM.

For SRBC circuit such as in Figure 10, there are two sets of parameters that have been calculated and determined because the circuit can conduct in either CCM or DCM mode. Therefore, each of the conduction modes has its own parameters that are shown in Table 4.

Table 4: Value of R_1, C_1 and L_1 for CCM and DCM [21]

	CCM	DCM
Resistor, R_1	3.5 Ω	4 Ω
Capacitor, C_1	0.625 μF	9.375 μF
Inductor, L_1	15 μH	1 μH

There are several factors to be considered when selecting the key devices or components to be used in the circuit of the MPPT circuit but one of the most important is the power loss associated with each device. Since the objective of the tracker is to deliver maximum power from the input which is the SRBC circuit to the load, power losses associated with the tracker itself should be minimal. The primary parts of the MPPT are simple and readily available and they include the MOSFET, diodes, operational amplifiers, inductors, capacitors and resistors. Each component has definite power loss associated with it. A power loss comparison is used to select the specific type of element which is best for the design.

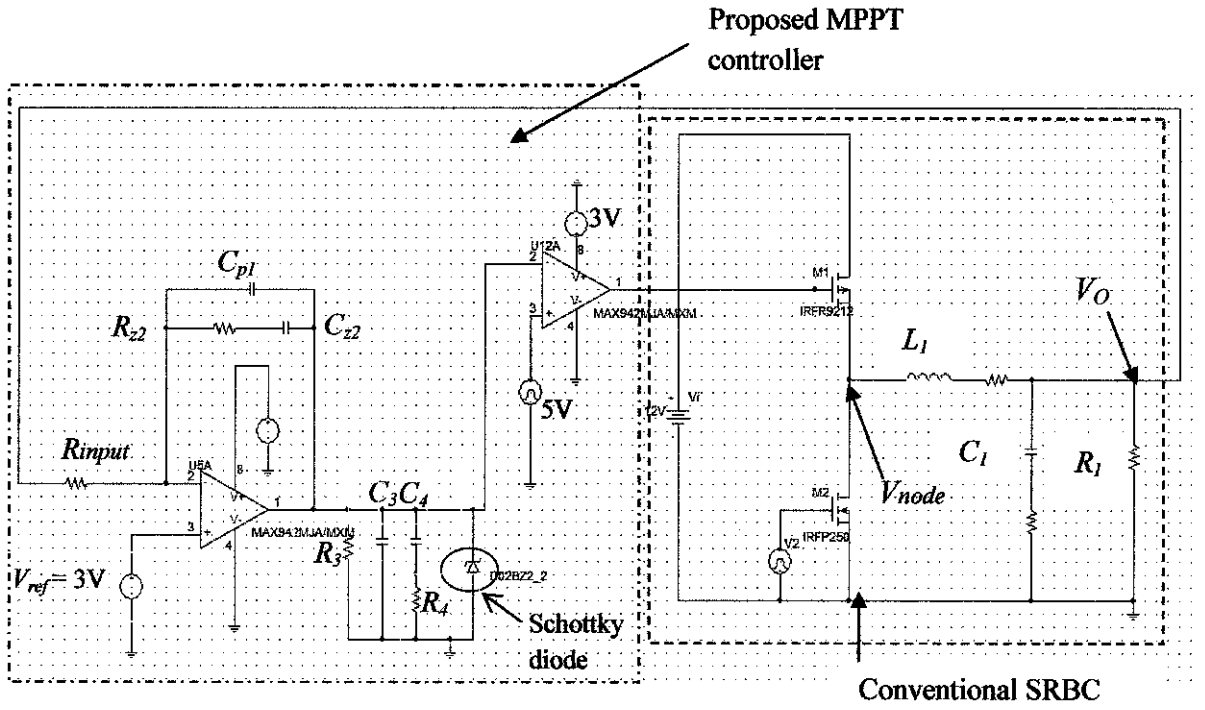

Figure 11: SRBC circuit connected with MPPT controller

Figure 11 shows the SRBC circuit with M_1 connected to the output amplifier of MPPT circuit. In this circuit M_2 is turned on by the PWM signals supplied from the PWM_2 while M_1, the PWM signals used to turn it on are controlled by the MPPT circuit.

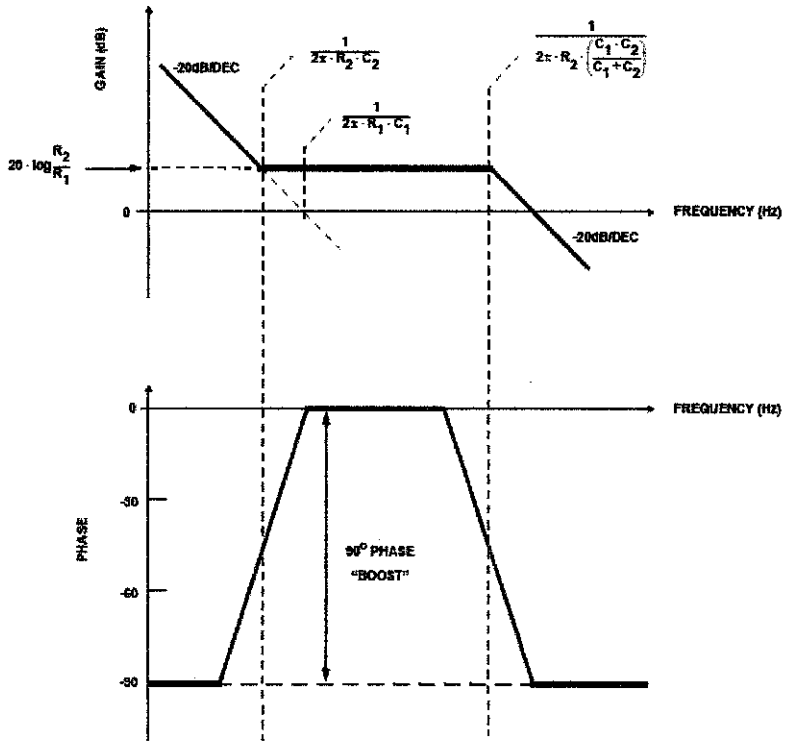

Figure 12: Generic Type II compensator [22]

Figure 12 shows the Generic Type II compensator which shows the placement of the poles and zeros. From it, the transfer function of Type II compensator is obtained:

$$\frac{1}{R_{input} \cdot C_{p1}} \left[\frac{\left(s+\frac{1}{R_{z2}C_{z2}}\right)}{s\left(s+\frac{C_{p1}+C_{z2}}{R_{z2}C_{p1}C_{z2}}\right)} \right] \tag{8}$$

The following guidelines will help to calculate the component values for MPPT circuit (which have some similarities with Type II network) [22].

1. Choose a value for R_{input}, usually between 2k and 5kΩ. In this project, 3k is chosen.
2. Pick a gain (R_2/R_1) that will shift the Open Loop Gain up to give the desired bandwidth. The following equation will calculate an R_{Z2} that will accomplish this given the system parameters and a chosen R_1.

$$R_{Z2} = \left(\frac{FESR}{FLC}\right)^2 \cdot \frac{DBW}{FESR} \cdot \frac{\Delta VOSC}{VIN} \cdot R_{input} \quad (9)$$

$$FLC = \frac{1}{2\pi\sqrt{LC}} \quad (10)$$

$$FESR = \frac{1}{2\pi.RC.C} \quad (11)$$

$$DBW = 0.3 \times fsw \quad (12)$$

3. Calculate C_{z2}:

$$C_{Z2} = \frac{10}{2\pi.R_{Z2}.FLC} \quad (13)$$

4. Calculate C_{p1}:

$$C_{p1} = \frac{C2}{(\pi.R_{z2}.C_{Z2}.fsw)-1} \quad (14)$$

Table 5: Simulation parameters of MPPT circuit

	CCM	DCM
Rinput (Ω)	3k	3k
R_{z2} (kΩ)	1414	94.2
C_{z2} (pF)	21.66	86.12
C_{p1}(pF)	0.2275	325.87
R_3(Ω)	3k	3k
R_4(Ω)	2k	2k
C_3(F)	10p	10p
C_4(F)	0.2u	0.2u

The diode (in red circle) is one of the components of the MPPT with the highest power loss. The power loss is mainly due to the forward voltage drop of the diode, which can be significant for some diodes. The forward voltage drop is the voltage required before the diode is turned on and current is allowed to flow. The Schottky diode has the lowest on-voltage when compared to other silicon general purpose and fast recovery diodes. There is a trade-off between the recovery speed, the breakdown voltage and the forward voltage drop. In this case, the lower forward

voltage drop is preferable to the fast recovery speed and therefore the Schottky diode in Figure 11 is suitable for the design.

Another component where power loss varies as a function of frequency is the inductor. All inductors have some internal resistance, and the power loss is due to this resistance. Hence, the lower the internal resistance of an inductor, the lower the power loss will be. The internal resistance varies inversely with the wire gauge; i.e. as the wire gauge increases, the internal resistance decreases. In general, a bigger inductor will have less internal resistance than a smaller inductor as more current passes through the bigger inductor. The drawback is the size and cost of the bigger inductor. Therefore, when selecting an appropriate inductor, it is important to strike a balance between a low internal resistance, the size and cost of a bigger inductor.

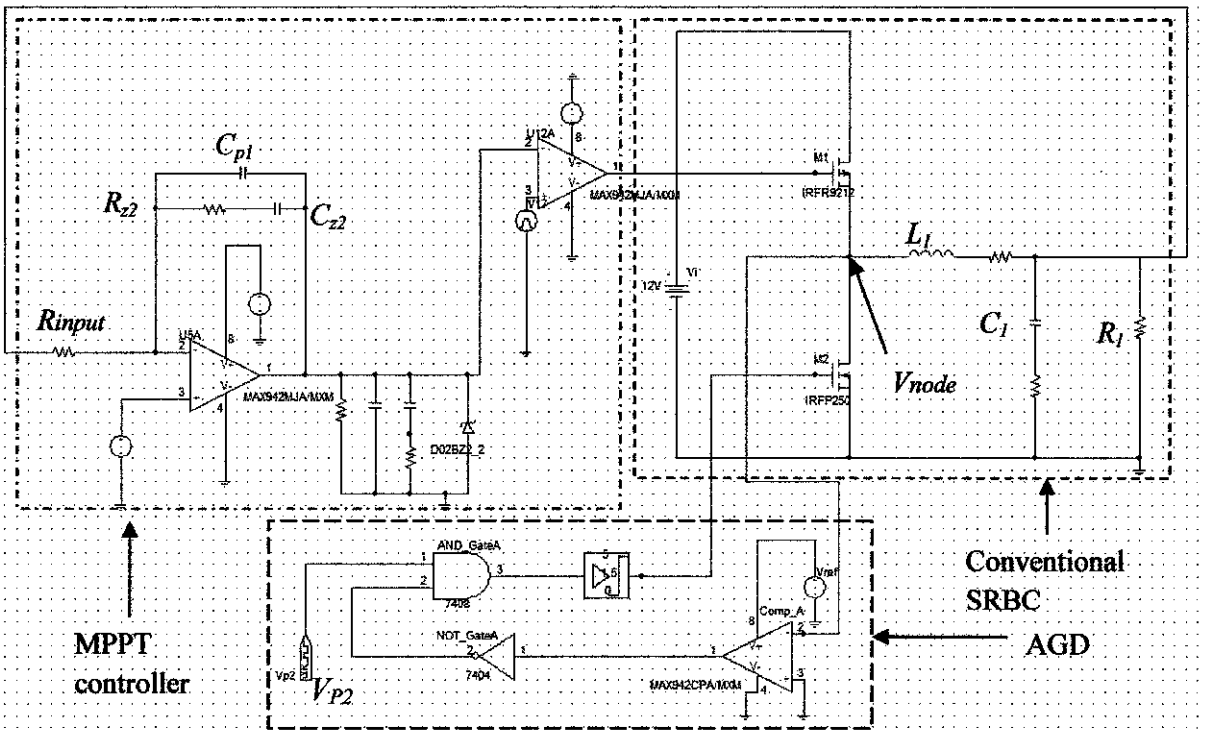

Figure 13: MPPT and AGD with SRBC

Figure 13 shows the last circuit in this project which is the combination of MPPT controller and AGD with SRBC. In this circuit M_1 is connected to the output of MPPT controller circuit while M_2, the PWM signals used to turn it on are controlled by the AGD circuit. Here the V_{p2} is set based on the duty ratio of M_1. This is to ensure there will be no cross conduction between the two switches. The parameters are determined according to the SRBC conduction modes.

3.5 PSPICE Simulation and Analysis Performance

The purpose of this simulation is to check whether the designed circuit meets the expectation and produces the desired output. Here all parameters are set in the PSPICE simulation. The graphs obtained will be observed. This is to ensure the correct output from the designed circuit can be determined. If simulation results do not show the expectation graph, the circuit will be re-designed. Table 6 below shows the simulation parameters for SRBC, combination MPPT with SRBC and combination of MPPT controller and AGD with SRBC.

Table 6: Parameters of SRBC and MPPT controller for f_s= 1 MHz

Components	Parameter Settings in PSPICE simulator and Component used.
PWM_1	V1=0, V2=5V, T_d = 0ns T_r = 5ns, T_f = 5ns, PW = 240ns, PER= 1000ns
PWM_2	V1=0, V2=5V, T_d = 265ns, T_r = 5ns, T_f = 5ns, PW = 710ns, PER= 1000ns
V_{p2}	Delay = 255ns, On time = 729ns, Off time = 271ns
M_1, M_2,	IRFP250

Every circuit will start with the observation of PWM signal graph in order to ensure correct PWM signals are fed into the switch. Next, the voltage at node or V_{node} is observed to ensure that it is equal to the input voltage and it will be used to turn on both of the switches. Besides that, graph for the inductor current is used to indicate the operation of SRBC either in CCM or DCM mode. Thorough analysis on the performance of the SRBC will be done in the discussion part.

3.6 Comparative Assessment

In this part, both circuits for MPPT-SRBC and MPPT-AGD with SRBC circuit are compared with the combination of CGD [21], AGD-SRBC [23], Compensator-AGD [23] and parallelism [24]. The comparatives are done based on the output voltage, current, output ripple peak-to-peak voltage and current and the body diode conduction loss. Each of the data will be compiled in the tables to see the significant differences among them.

CHAPTER 4
RESULT AND DISCUSSION

4.1 Result and Discussion

This chapter discusses the results obtained from the simulation and evaluates the performance of the circuits. The simulation starts with designing and simulating the basic SRBC circuit, followed by SRBC with MPPT controller and the last circuits are MPPT-AGD with SRBC. Adding those circuits to SRBC will result in self driven behaviour where it generates the PWM signal without using the V_{pulse}.

From the circuits, graphs on PWM signals, node voltage, inductor voltage, inductor current, output voltage and output current are obtained. Those graphs are observed and analysis regarding the performance of the circuit will be discussed.

4.1.1 Simulation of Conventional SRBC circuit

For SRBC circuit such as in Figure 11, there are two sets of parameters that have been calculated and determined because the circuit can conduct in either CCM or DCM mode. Therefore, each of the conduction modes has its own parameters as shown in Table 4.

The following waveforms are from circuit designed in Figure 11. For the PWM pulses, they are set using the same PWM setting as in Table 6.

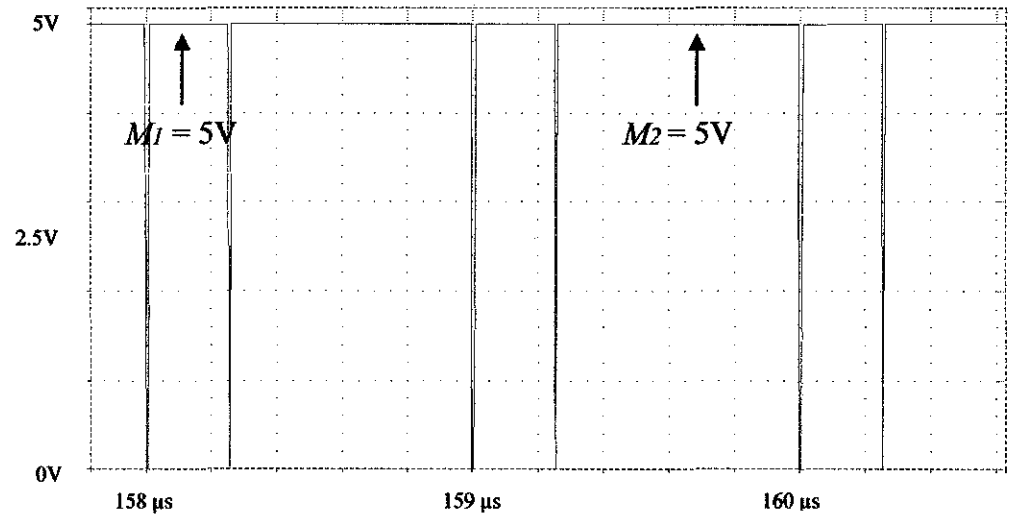

Figure 14: PWM of SRBC circuit

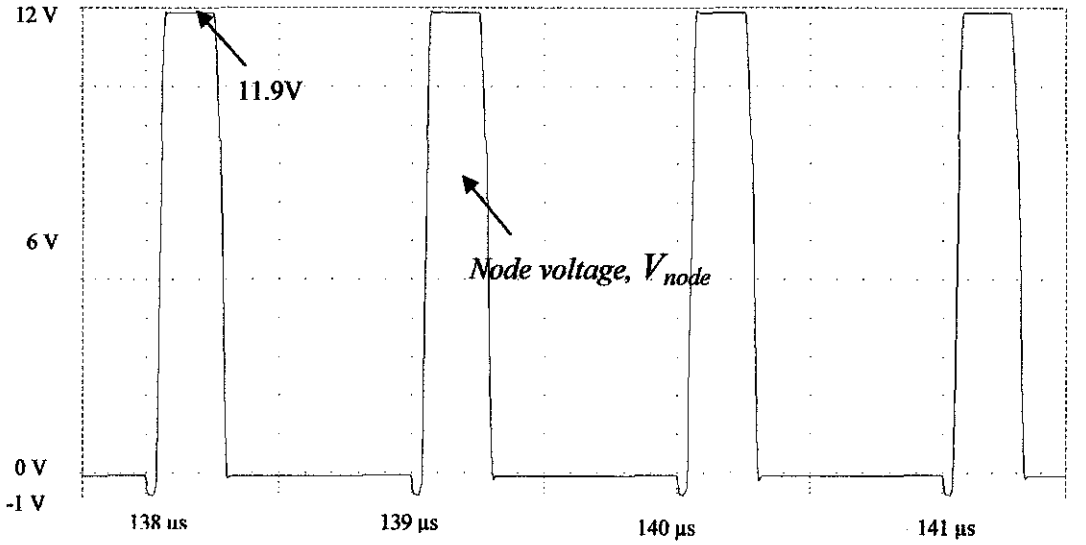

Figure 15: Node Voltage, V_{node} of SRBC

Figure 14 and Figure 15 show the PWM signals and the node voltage, V_{node} of the SRBC circuit respectively. Theoretically, node voltage, V_{node} has to be equal to the input voltage, V_i in order to ensure that the PWM signal is generated correctly. In this case, the value of 11.9 V in Figure 15 which is almost 12 V shows that the correct PWM signal has been generated to turn on both of the switches. PWM_1 and PWM_2 are set as in Table 6. The PWM specifications are determined based on the 1

MHz switching frequency, f_s. In this simulation, high switching frequency is used to reduce the size of the inductor and capacitor.

4.1.1.1 SRBC Simulation Graph for CCM

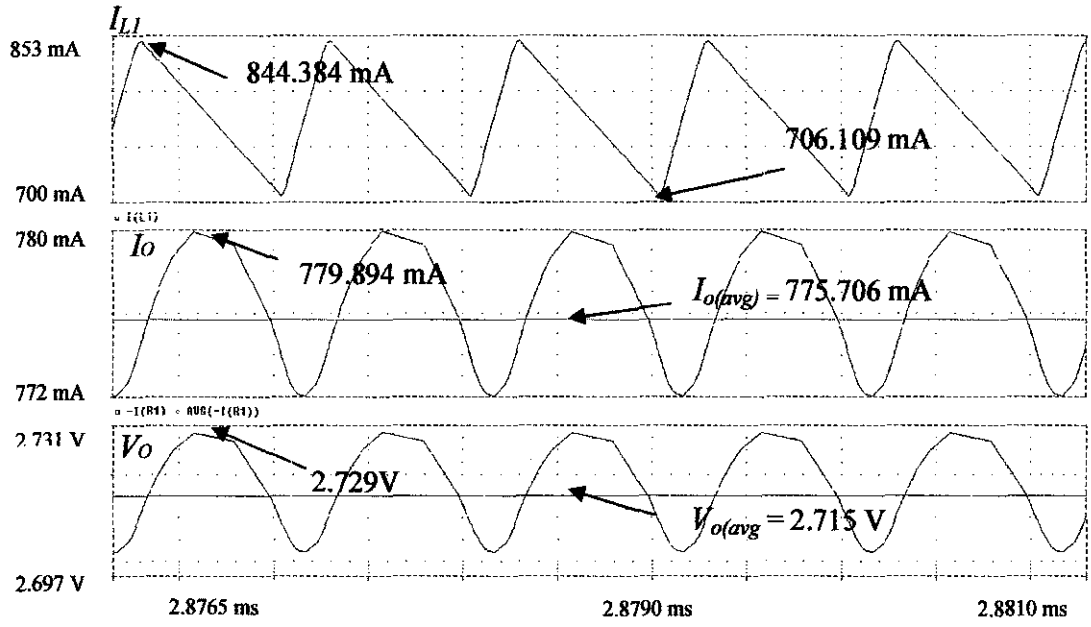

Figure 16: Inductor current, I_{L1}, output current, Io and Output Voltage, Vo (CCM)

Figure 16 shows the average output voltage, $V_{o(avg)}$ which is 2.715 V and the average output current $I_{o(avg)}$ which is 775.706 mA. Theoretical value for voltage output is 3 V but the slightly difference result obtained for this circuit occurs due to the high ripples at the resultant output and because of this reason it is important to ensure that the ripples are small in order to have an accurate result.

CCM is a condition when current in the inductor does not fall to zero between the switching cycles. Figure 16 shows that SRBC operates in the CCM where there is no negative portion at inductor current. The maximum peak is 844.384 mA while the minimum is 706.109 mA. This CCM operation implies low output power in SRBC.

4.1.1.2 SRBC Simulation Graph for DCM

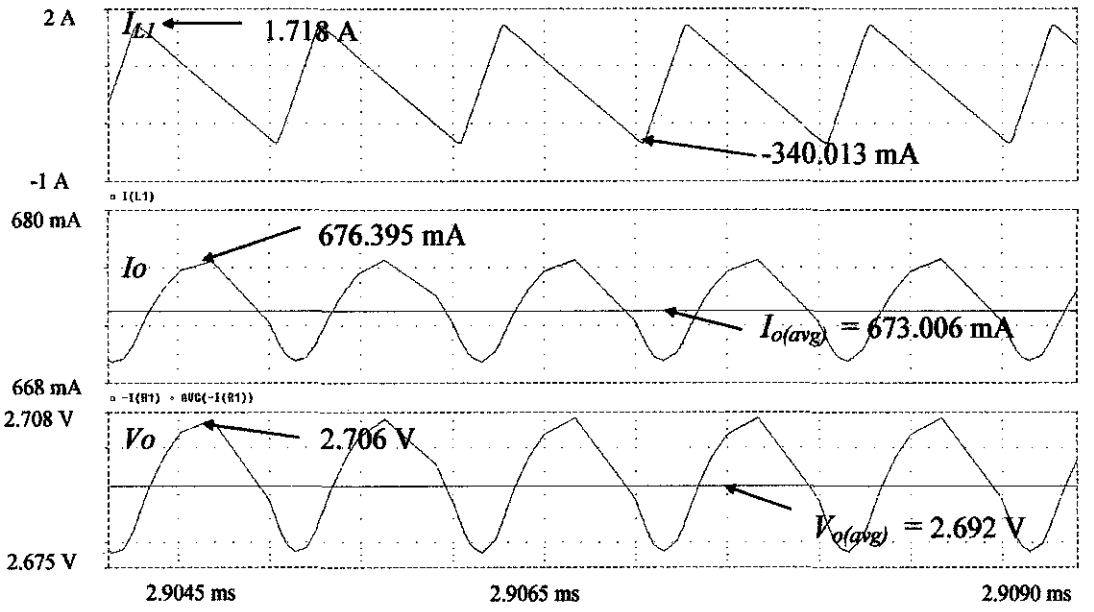

Figure 17: Output Voltage, Vo, output current, Io and inductor current, I_{L1} (DCM)

Figure 17 shows the average output voltage and current for this circuit. The $V_{o(avg)}$ is observed to be 2.692 V and $I_{o(avg)}$ obtained is lower than when it is operated in CCM which is 673.006 mA. From the inductor current graph, it shows that it is operating in DCM mode because current in the inductor falls to zero and remains at zero for some portion of switching cycle. The maximum peak I_{L1} is 1.718 A while the minimum is -340.013 mA.

Table 7: SRBC for CCM and DCM

	CCM	DCM	Differences between CCM and DCM(%)
$V_{o(avg)}$, (V)	2.715A	2.692	0.85
I_{oavg}, (mA)	775.706	673.006	13.24
$I_{L1,max}$ peak (A)	0.844	1.718	50.87
$\Delta V_{op\text{-}p}$ (%)	1.055	1.027	2.65
$\Delta I_{op\text{-}p}$ (%)	1.074	1.002	6.7
P_{BD} (W)	0.423	0.119	71.87

Table 7 shows the comparisons between CCM and DCM mode of SRBC circuit. It can be seen from the table that the average output current is reduced by 13.24% ($\frac{775.706-673.006}{775.706} \times 100\%$) when the SRBC operates in DCM condition. On the other hand, in DCM mode, the body diode conduction loss, P_{BD} is reduced to 71.87% ($\frac{0.423-0.119}{0.423} \times 100\%$). This is because by allowing inductor current, I_{L1} to operate in DCM can help minimize the losses caused by the switches.

4.1.2 MPPT controller with SRBC

Next stage of this project is having MPPT controller connected to M_1 of the SRBC circuit as shown in Figure 11 and PWM signal for M_2 is supplied from pulse voltage source, V_{pulse} with the same setting as mentioned in Table 6. Similarly, all the parameters for the output circuit are determined based on its conduction mode.

A proper controller or compensator network has to be designed so that the system can allow the predictable bandwidth with unconditionally stability. An ideal Bode plot with a gain that roll off at a slope of -20dB/decade, crossing 0dB at the desired bandwidth and phase margin which greater than 45° has to be obtained [22]. Before the parameters are chosen, transfer functions of SRBC, compensator type II and the combination of both of them have to be determined. For Type II compensator transfer function, it is obtained after the positioning of zeros and poles location and it is given as in Eq. (8).

4.1.2.1 Bode plot for SRBC system

There are two parts of bode plot for this system. First is when the SRBC is conducting in CCM and another one is when it is in DCM. These bode plots will show the stability of the SRBC systems before and after adding the controller.

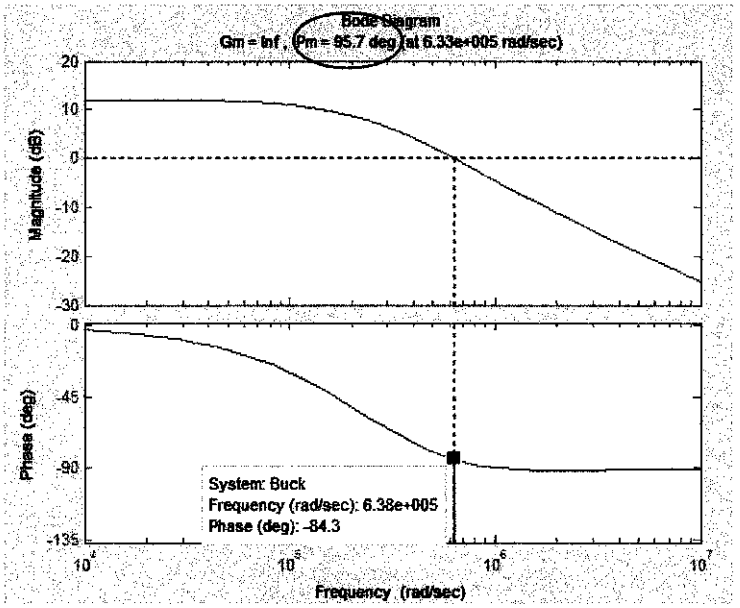

Figure 18: Bode plot of SBRC (CCM)

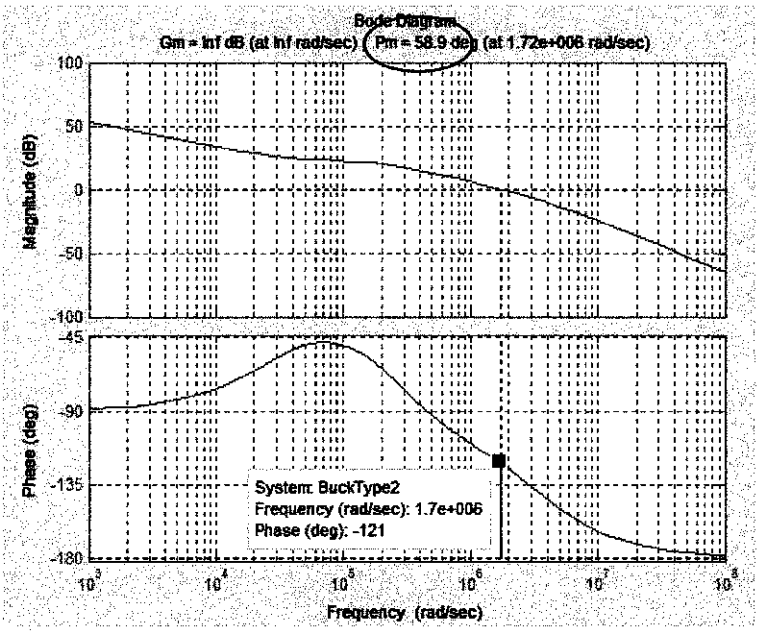

Figure 19: Bode plot of SRBC with Compensator type II (CCM)

Figure 18 and Figure 19 show the bode plot of SRBC before and after combining with the compensator type II which is a part of MPPT circuit. The phase margin is decreased from 95.7° to 58.9°. The phase margin is determined by the differences between the phase at 0dB gain to the -180°, where -180° is the critical output phase angle of the operational amplifier. Before the compensator is added, the

resultant phase margin is -83.4° - (-180°) = 95.7° which is almost accurate to the MATLAB simulation as in Figure 18. But once the type II compensator is added, the phase margin is given by -121°-(-180°) = 58.9°. This shows that the stability of the combination of MPPT with SRBC system because the phase margin obtained is greater than 45°.

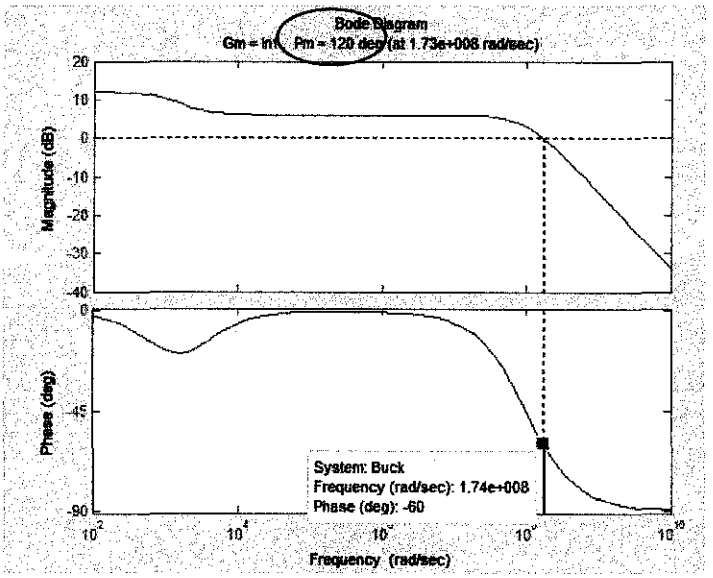

Figure 20: Bode plot of SBRC (DCM)

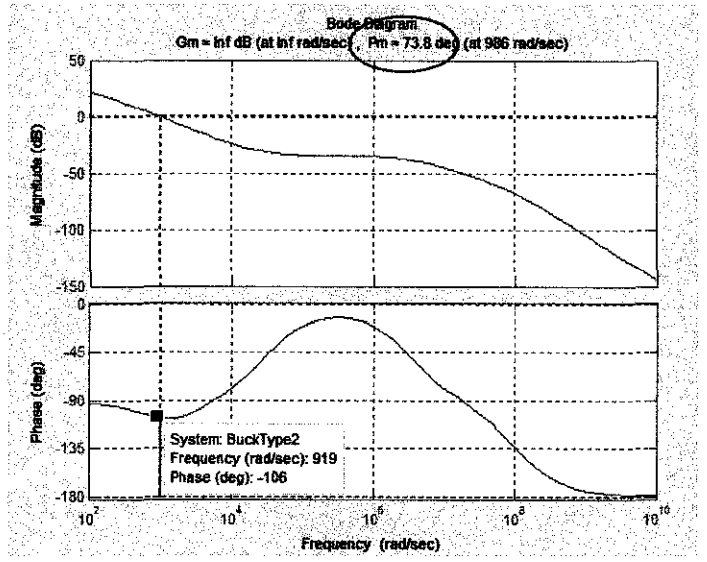

Figure 21: Bode plot of SRBC with compensator type II (DCM)

Same goes when it is conducted in DCM. The phase margin for the SRBC system without the compensator is given by $-60^{o} - (-180^{o}) = 120^{o}$.Same as in CCM, the value obtained is almost same to the MATLAB simulation result. After the system is modified with the compensator, the phase margin is obtain as $-106^{o}-(-180^{o}) = 73.8^{o}$. It still consider to be in the stabilized condition because it satisfied the feedback design characteristic where to ensure the stability of a system, the phase margin has to be more than 45^{o}.

4.1.2.2 MPPT controller with SRBC Simulation Graph for CCM

After the controller is designed, the SRBC is ready to be simulated with V_{pulse} at M_2 and the resultant waveforms for the circuit are observed and analyzed.

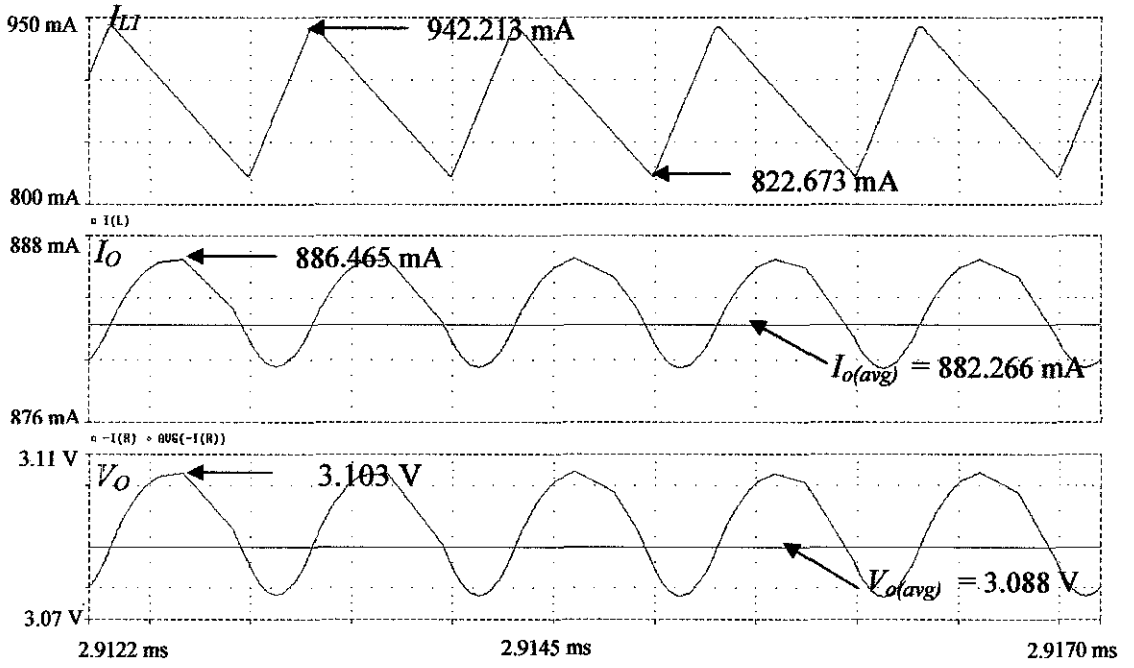

Figure 22: I_{LI}, I_O *and* V_O of MPPT with SRBC (CCM)

Figure 22 shows the output voltage, output current and inductor current for SRBC. It is noticed that the output voltage and current have increased compared to the SRBC circuit. Besides the waveforms are much smoother due to the small ripples. Output ripple voltage peak-to-peak, $\Delta V_{op\text{-}p}$ and output ripples current, $\Delta I_{op\text{-}p}$ are 0.947 % $(\frac{3.103-3.088}{3.103} \times 100\% \times 2)$ and 0.947 % $(\frac{886.465-882.266}{886.465} \times 100\ \% \times 2)$ respectively. From the graph of inductor current I_{L1}, it proves that the operation of the controller is in CCM because there is no negative polarity shown in the waveforms. The value for $V_{o(avg)}$ and $I_{o(avg)}$ are 3.088 V and 882.266 mA. The value of the voltage almost satisfies the theoretical value which is 3 V.

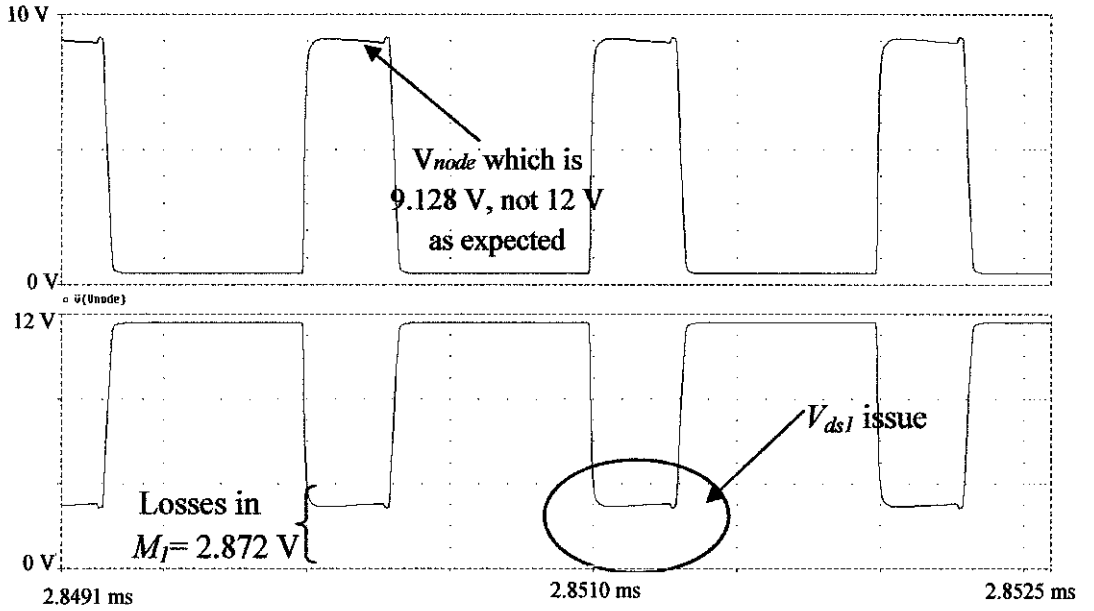

Figure 23: Node Voltage, V_{node} and V_{ds1} for MPPT with SRBC (CCM)

Figure 23 shows that the node voltage, V_{node} is not 12 V. It only reaches to 9.128 V. Another 2.872 V is still consumed in M_1. This is shown in the circle where the switching characteristic of the V_{ds1} is different from expectation and the issues need to be solved. However, V_{node} obtained is considered to be enough to produce 2.872 V of output voltage since the voltage drop at the output inductor, L_1 is around 6 V as shown in Figure 24.

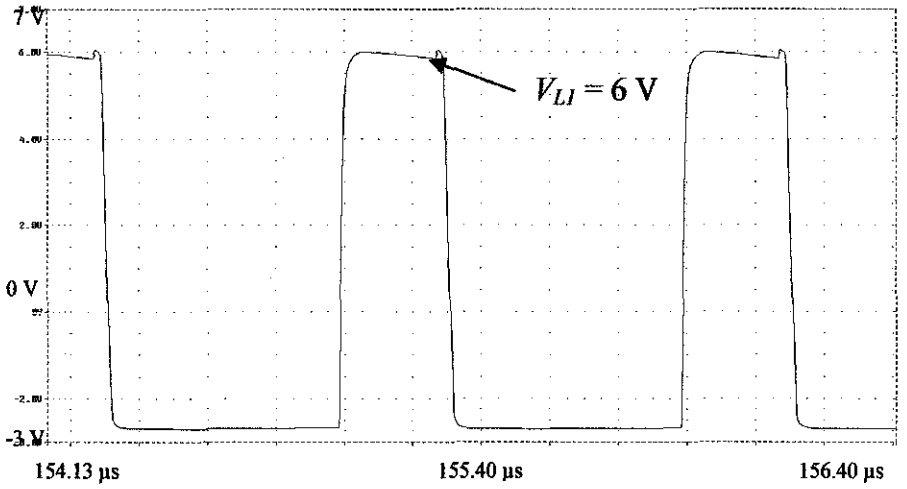

Figure 24: V_{LI} for MPPT controller with SRBC (CCM)

4.1.2.3 Simulation of MPPT controller with SRBC for DCM

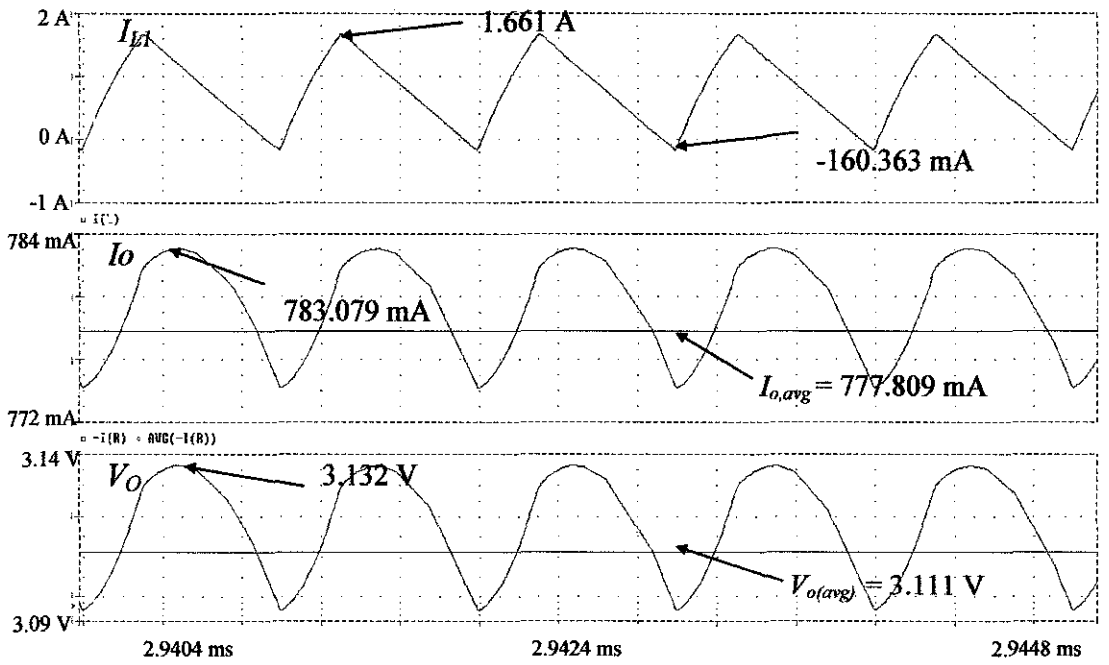

Figure 25: I_{LI}, I_o, *and* V_o, for MPPT controller with SRBC (DCM)

Figure 25 illustrates the output voltage, output current and inductor current for MPPT controller with SRBC in DCM mode. The $V_{o(avg)}$ is 3.111 V and the I_{oavg} is 777.809 mA. Here, the current ripples are higher than in CCM and due to that reason, the average output current is lowered by 11.84 % ($\frac{882.266-777.809}{882.266} \times 100\%$).

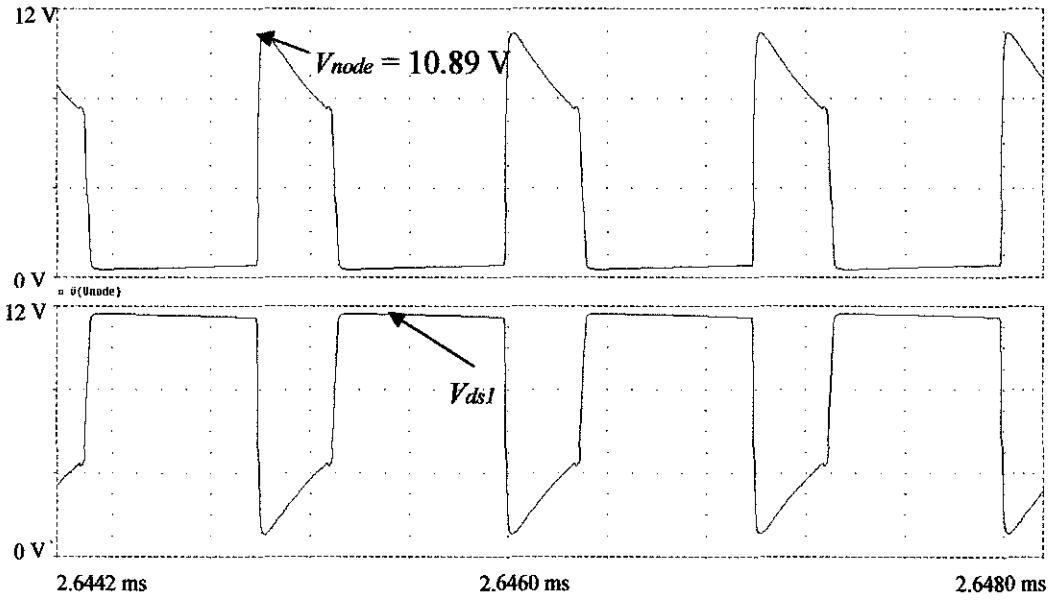

Figure 26: V_{node} and V_{ds1} for MPPT controller with SRBC (DCM)

Besides that, the SRBC also experiences the issue where the node voltage, V_{node} is just 10.89 V and not equal to 12 V. This is shown in Figure 26. This issue occurs due to the same reason as in CCM where the V_{ds1} does not meet the switching characteristics. However, the resultant waveforms for this controller still produce 3 V for the output voltage because the voltage across the inductor is 7.79 V as shown in Figure 27.

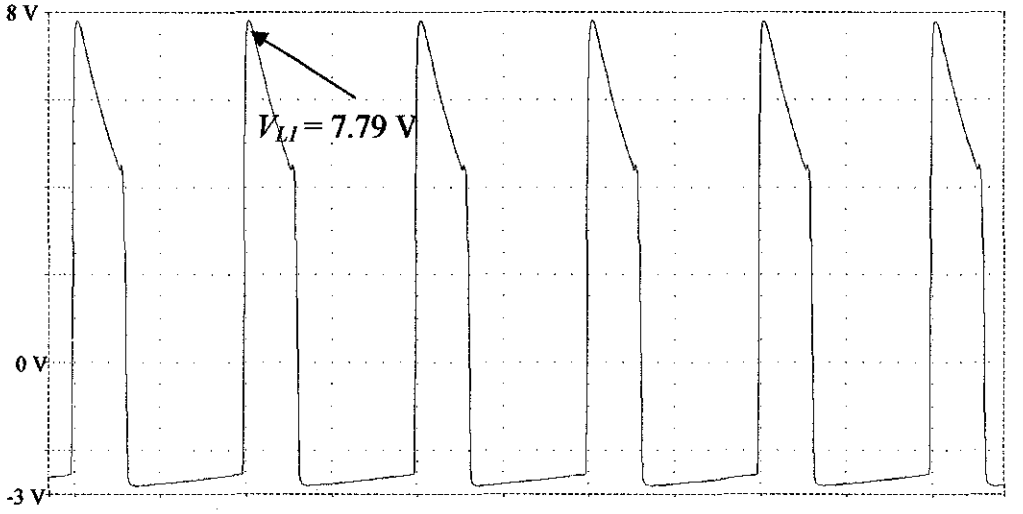

Figure 27: V_{LI} for MPPT controller with SRBC (DCM)

Table 8: MPPT controller with SRBC for CCM and DCM

	CCM	DCM	Differences between CCM and DCM (%)
$V_{o(avg)}$ (V)	3.088	3.111	0.74
$I_{o(avg)}$ (mA)	882.266	777.809	11.84
$I_{Lmax\ peak}$ (A)	0.942	1.661	43.29
ΔV_{op-p} (%)	0.948	1.347	29.6
ΔI_{op-p} (%)	0.947	1.346	29.6
P_{BD} (W)	none	none	-

Based on Table 8, it has same results as the previous conventional SRBC circuits where the resultant output for voltage and current have higher value in CCM and slightly lower in DCM. Besides, it also has fewer ripples on the output where the waveforms are smoother compared to the conventional SRBC circuits. But the ripple increases as it enters the DCM.

4.1.3 MPPT controller and AGD with SRBC Circuit

Next part in this project is having MPPT controller connected to M_1 while AGD connected to M_2 of the SRBC circuit as shown in Figure 13. For the AGD circuit, the delay is set by digital clock stimulus, V_{p2}. In order to avoid the cross conduction between the two switches, the setting of V_{p2} has to be based on the V_{pulse} at M_1. The purpose of AGD in the circuit is to control the dead time between the two switches. It can also improve the performance of SRBC by reducing the body diode conduction loss.

4.1.3.1 MPPT controller and AGD with SRBC Simulation Graph for CCM

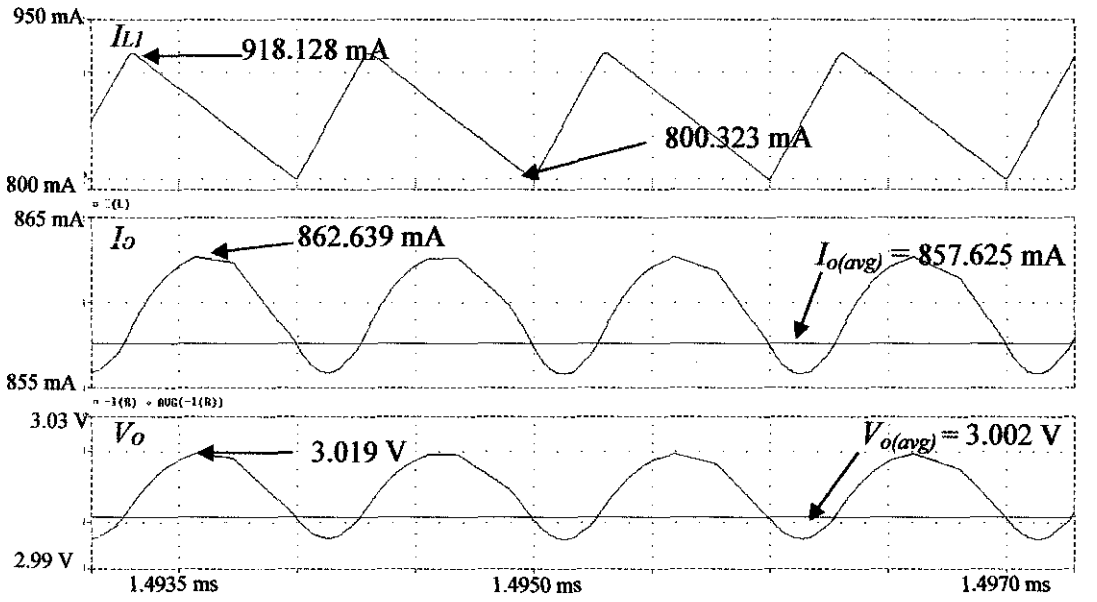

Figure 28: I_{L1}, I_o, V_o for MPPT controller and AGD with SRBC (CCM)

Figure 28 shows the output voltage, current and inductor current for MPPT and AGD with SRBC. It is noticed that the output voltage and current have increased compared to the SRBC circuit. Besides the waveforms are much smoother. For I_{L1}, it proves that the operation of the converter is in CCM. Figure also shows the $V_{o(avg)}$ and

$I_{o(avg)}$ where the values are 3.002 V and 857.625 mA respectively. The value of the voltage almost satisfies the theoretical value of 3 V.

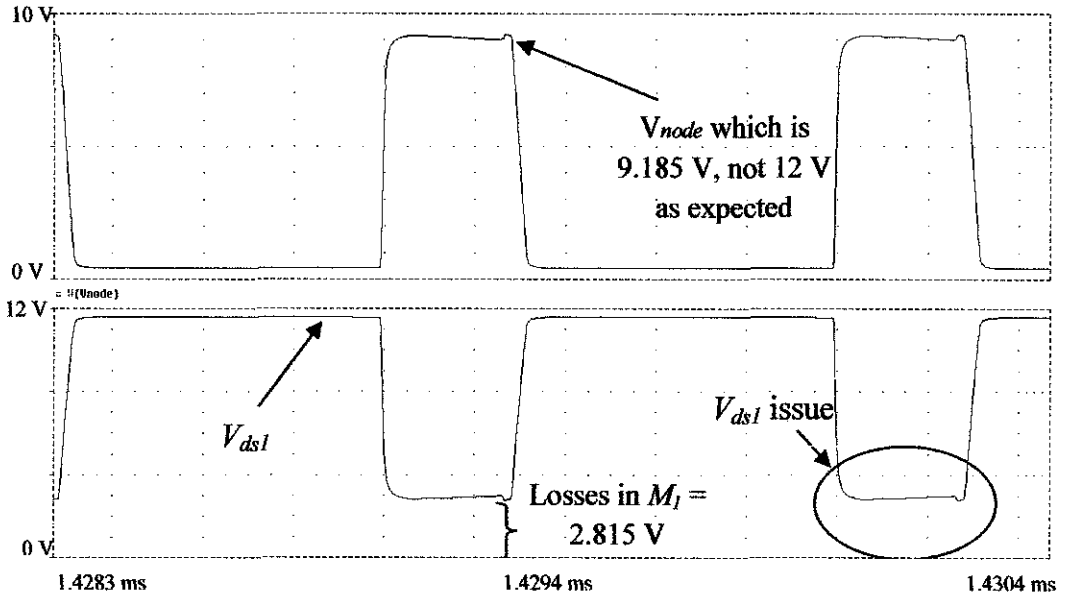

Figure 29: V_{node}, $V_{ds1}$for MPPT and AGD with SRBC (CCM)

Figure 29 above shows that V_{node} is not 12 V. It only reaches 9.185 V. Another 2.815 V is still consumed in M_1. This is shown in the black circle where the switching characteristic of the V_{ds1} does not meet the expectation. However, V_{node} obtained is considered to be enough to produce 3 V of output voltage since the voltage drop at the output inductor, V_{L1} is approximately 6.15 V. This is illustrated in Figure 30.

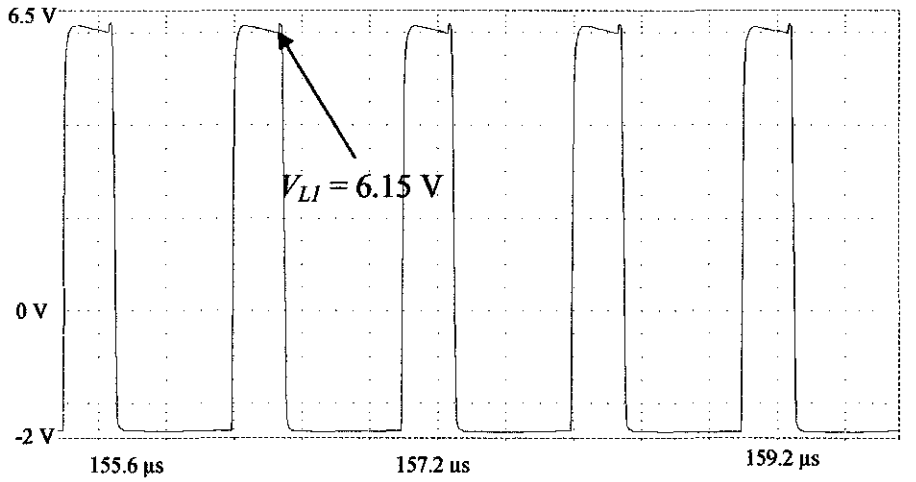

Figure 30: V_{L1} for MPPT and AGD with SRBC (CCM)

4.1.3.2 Simulation of MPPT and AGD with SRBC for DCM

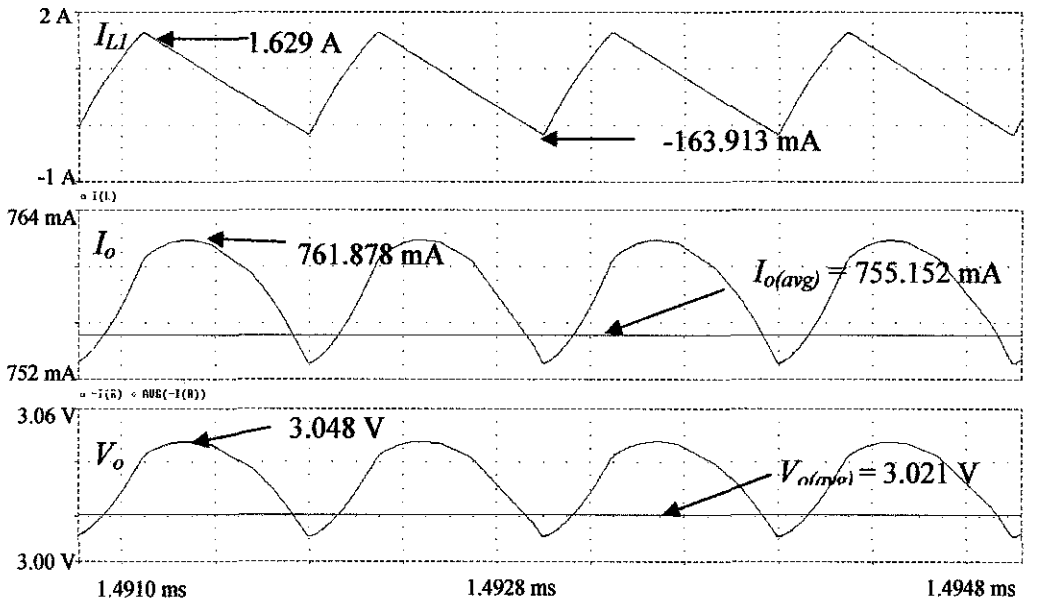

Figure 31: I_{L1}, I_o, *and* V_o for MPPT and AGD with SRBC (DCM)

Similarly, in CCM, Figure 31 illustrates the output current, voltage and inductor current for MPPT and AGD with SRBC for DCM. Here the ripples are higher than it is operating in CCM and due to high ripples, the $I_{o(avg)}$ is decreased by

11.95 % ($\frac{857.625-755.152}{857.625} \times 100\%$) compared to CCM. For $V_{o(avg)}$, the value of 3.021 V also shows that the resultant output is almost 3 V.

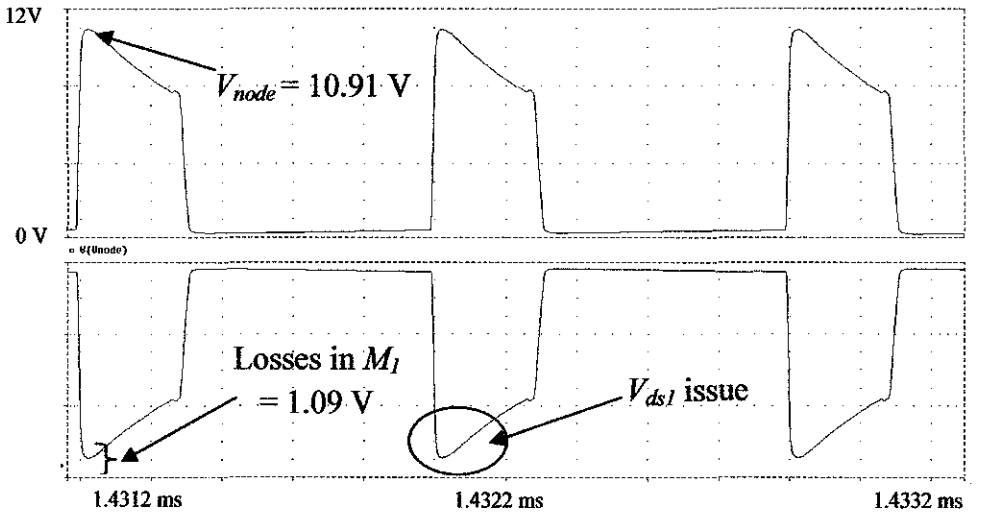

Figure 32: V_{node} *and* V_{ds1} for MPPT controller and AGD with SRBC (DCM)

The circuit also experiences the issue where V_{node} is just 10.91 V and not equal to 12 V as shown in Figure 32. This is due to the same reason as in CCM where the V_{ds1} does not meet the switching characteristics. The resultant waveforms for this controller still produce 3 V for output voltage because the voltage across the inductor is 7.79 V as shown in Figure 33.

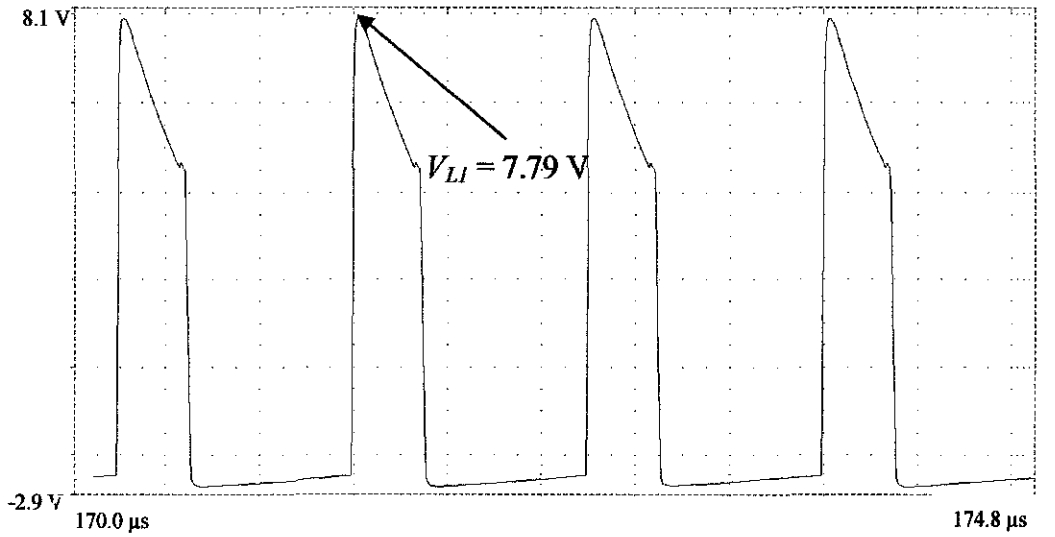

Figure 33: V_{L1} for MPPT controller and AGD with SRBC (DCM)

Table 9: MPPT controller and AGD with SRBC for CCM and DCM

	CCM	DCM	Differences between CCM and DCM (%)
$V_{o(avg),}$ (V)	3.002	3.021	0.63
$I_{oavg,}$ (mA)	857.625	755.152	11.95
$I_{Lmax\ peak}$ (A)	0.918	1.629	43.65
ΔV_{op-p} (%)	1.126	1.772	36.46
ΔI_{op-p} (%)	1.162	1.766	34.20
P_{BD} (W)	none	none	none

Based on Table 9, it has same results as the conventional SRBC and MPPT with SRBC circuit where the resultant outputs for voltage and current have higher values in CCM and slightly lower in DCM mode. Besides, it has more ripples on the output than the conventional SRBC and MPPT with SRBC circuit. But the ripple increases as it enters DCM.

4.2 Comparison of the circuits' performance.

In this part, the differences between all the circuits are narrowed down to their voltage node, output voltage and current, and the gate voltages, V_{gs} for M_1. After all simulations are done, some improvements are seen at the output voltage and current as well as drawbacks when the controllers are applied to both switches.

4.2.1 Output Voltage and Current

Having MPPT at M_1 of the SRBC, it has slightly increased the output voltage and current. Besides that, the output current also increases for CCM and DCM compared to conventional SRBC circuit. However, the combination of MPPT and

AGD results in high ripples at the output voltages and current when it is operated in DCM. It has the highest ripples percentage compared to the conventional SRBC and MPPT with SRBC.

4.2.2 Voltage node

Each of the waveforms obtained is compared in order to see the significant differences between all the designed circuits for both of the conduction modes.

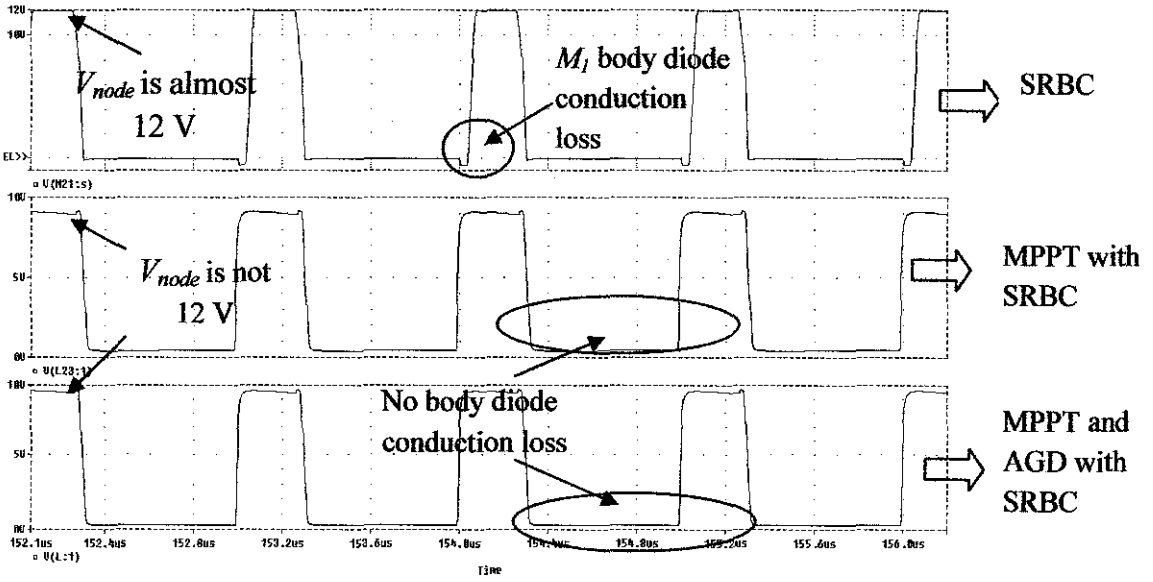

Figure 34: V_{node}, body diode for SRBC, MPPT and MPPT with AGD (CCM)

As mentioned before, voltage node is one of the important parts that need to be observed. This is because it indicates the correct switching signal that will be fed into the converter. For all the conduction modes V_{node} has to be almost the same with the input voltage. Figure 34 shows the V_{node} of all the designed circuit in CCM. On the other hands, Figure 35 shows the V_{node} in DCM.

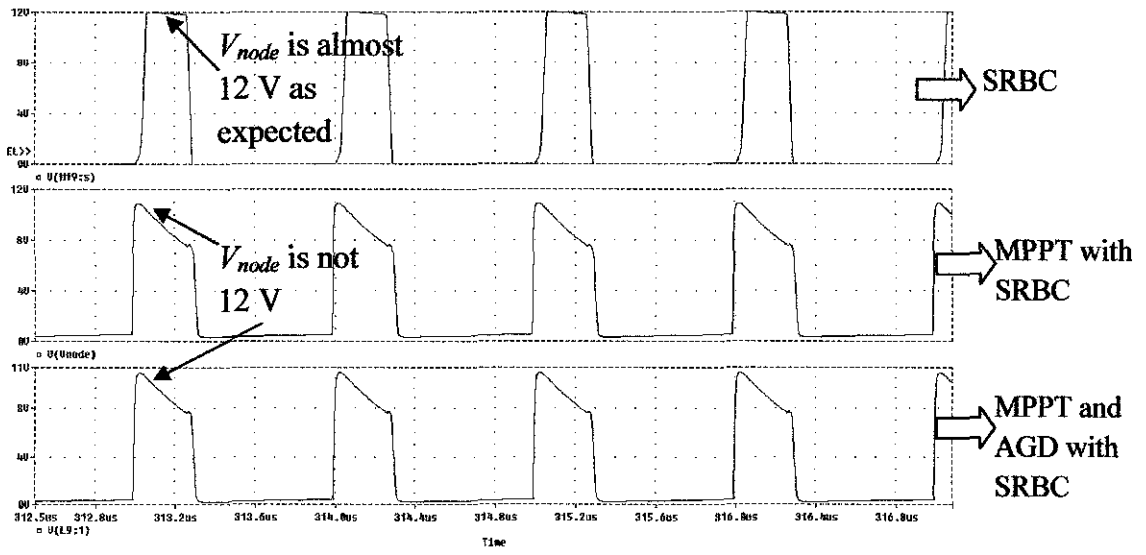

Figure 35: V_{node}, body diode for SRBC, MPPT and MPPT with AGD (DCM)

From both Figure 34 and Figure 35, it can be seen that V_{node} for both combination of MPPT-AGD with SRBC and MPPT-SRBC are not equal to the input voltage. It has the value of 9.159 V for CCM and 10.91 V for DCM. The remaining voltages are consumed in M_1 as the other losses in it. This is also same goes to the SRBC as it is operated in DCM. Although it can be said that the switching signal is not really accurate when the MPPT and AGD are applied, it still enough to produce 3 V of the output voltage. This is because, the voltage across the inductor for CCM and DCM are around 6 V and 7 V respectively.

4.3 Comparative Assessment

In this section, the performance of SRBC is analyzed with respect to Conventional Gate Drive (CGD), AGD, compensator and AGD, MPPT controller and MOSFET parallelism of both switches. The analyses are done based on the average output voltage and current, peak-to-peak ripple voltage and current and the last one is the body diode conduction losses. In MOSFET parallelism for CCM, M_1 is paralleled with four MOSFET. Meanwhile for DCM, M_1 is also paralleled with four MOSFETs and for M_2, three MOSFETs are paralleled. All data are tabulated as in Table 10 and Table 11 for the CCM mode and Table 12 and Table 13 for DCM.

Table 10: Comparison between conventional SRBC, AGD, Compensator and AGD, parallelism and MPPT controller (CCM)

	CCM					
	CGD[21]	AGD[23]	Compensator and AGD[23]	Parallelism[24]	MPPT	MPPT and AGD
$V_{o(avg),}$ (V)	2.70	2.68	2.99	2.69	3.09	3.00
$I_{oavg,}$ (mA)	770.26	765.76	853.77	863.84	882.27	857.63
$\Delta V_{o\ p\text{-}p}$ (%)	1.66	2.23	2.10	1.86	0.95	1.16
$\Delta I_{o\ p\text{-}p}$ (%)	1.62	2.21	2.08	2.36	0.95	1.16
P_{BD} (mW)	16.87	20.79	0	10.70	0	0

Table 11: Improvement of CGD, AGD, Compensator-AGD, Parallelism, and MPPT (CCM)

	CCM				
	Improvement of MPPT to CGD [21] (%)	Improvement of MPPT to AGD [23] (%)	Improvement of MPPT to Compensator and AGD [23] (%)	Improvement of MPPT to Parallelism [24] (%)	Improvement of MPPT to MPPT-AGD (%)
$V_{o(avg),}$ (V)	12.62	13.27	-3.24	12.94	-2.91
$I_{oavg,}$ (mA)	12.7	13.21	3.23	2.09	2.79
$\Delta V_{o\ p\text{-}p}$ (%)	42.77	57.40	54.76	48.92	18.10
$\Delta I_{o\ p\text{-}p}$ (%)	41.36	57.01	54.33	59.75	18.10
P_{BD} (mW)	100	100	0	100	0

4.3.1 Comparison in CCM

Table 10 and Table 11 illustrate the comparisons and improvements of the CGD, AGD, compensator and AGD, parallelism of the SRBC and MPPT controller in CCM mode respectively. From Table 10, it shows that MPPT with SRBC achieved the highest average output voltage and current while AGD with SRBC has the lowest value for output voltage and current compared to others. For the output voltage, MPPT with SRBC almost satisfies design requirement of 3V has to be achieved but better value is achieved by the compensator and AGD circuit.

In terms of body diode conduction losses, AGD and SRBC has the highest losses which is 20.79 mW compared to other circuits. Besides that, in terms of output voltage ripples, this circuit has the highest value where the ripple is 2.23 % as in Table 10. However, when SRBC is integrated with MPPT controller or combination of Type III compensator and AGD, the body diode losses is almost zero. This is because; there are some improvements to the output voltage, current and also reduction in body diode losses. High peak-to-peak output voltage ripples are achieved when AGD and AGD with Compensator is connected to SRBC which is more that 2 % for both circuits. For the output peak-to-peak ripple current, the SRBC results in highest value when M_1 is paralleled with four MOSFETs.

Furthermore, from observations, it can be seen that when SRBC is implemented with AGD, this results in a decrease in output voltage and current and increase in voltage ripple and current ripple compared to CGD. It does not meet the expectation and desired results. It also increases the body diode conduction losses by 3.92 % (20.79 mW – 16.87 mW) compared to CGD. The CGD with SRBC can produce higher output voltage and current which are 2.70 V and 770.26 mA compared to just 2.68 V and 765.76 mA when it is modified with the AGD.

Table 12: Comparison between CGD, AGD, Compensator and AGD, parallelism and MPPT controller (DCM)

	DCM					
	CGD [21]	AGD [23]	Compensator and AGD [23]	Parallelism [24]	MPPT	MPPT and AGD
$V_{o(avg)}$, (V)	2.70	2.68	2.99	2.7362	3.11	3.02
$I_{o(avg)}$, (mA)	676.13	670.60	748.86	758.52	777.81	755.15
$\Delta V_{o\ p\text{-}p}$ (%)	1.02	1.65	3.48	1.34	1.35	1.77
$\Delta I_{o\ p\text{-}p}$ (%)	1.06	1.62	3.41	1.00	1.35	1.77
P_{BD} (mW)	6.29	4.63	0	0	0	0

Table 13: Improvement of CGD, AGD, Compensator-AGD, Parallelism, and MPPT (DCM)

	DCM				
	Improvement of MPPT to CGD [21] (%)	Improvement of MPPT to AGD [23] (%)	Improvement of MPPT to Compensator and AGD [23] (%)	Improvement of MPPT to Parallelism [24](%)	Improvement of MPPT to MPPT-AGD (%)
$V_{o(avg)}$, (V)	13.18	13.83	-3.86	12.02	-2.89
I_{oavg}, (mA)	13.07	13.78	3.72	2.48	2.91
$\Delta V_{o\ p\text{-}p}$ (%)	-24.44	18.18	61.21	0.74	23.73
$\Delta I_{o\ p\text{-}p}$ (%)	-21.48	16.67	60.41	25.93	23.73
P_{BD} (mW)	100	100	0	0	0

4.3.2 Comparison in DCM

Table 12 and Table 13 show the comparisons and improvements of the CGD, AGD, compensator, MPPT and parallelism of the SRBC in DCM mode respectively. Comparison is almost same as in CCM when implemented MPPT to SRBC, this results in the highest average output voltage and current which is 3.11 V and 777.81 mA. Improvement of 13.18 % $(\frac{3.11-2.7}{3.11} \times 100\%)$ for output voltage and 13.07 % $(\frac{777.81-676.13}{777.81} \times 100\%)$ for output current are achieved when MPPT is implemented with SRBC compared to CGD. Even though it is still accepted, the best output voltage can be achieved when SRBC is connected with compensator and AGD because the output voltage is close to 3 V. Here, AGD with SRBC still gives the lowest average output voltage and current.

Output ripple voltage and current for MPPT with SRBC is considerable low which is around 1.35 % but the lowest can be achieved with CGD circuit which are 1.02 % and 1.06 % respectively. Besides that, compensator and AGD with SRBC circuit gives the highest output peak-to-peak ripple voltage and current which are 3.48 % and 3.41 % respectively as shown in Table 12. Having more ripples at the output can decrease the overall performance of the circuit. Compared to AGD and the parallelism, both of them have fewer output ripples for voltage and current especially at output peak-to-peak ripple current. It is observed when SRBC's switches are paralleled with more than one MOSFET where the output ripple current has the value of 1 %.

Furthermore, SRBC also experiences reduction in body diode conduction losses in DCM when it is connected to MPPT controller, compensator and AGD and when the switches are paralleled. Body diode conduction loss is almost zero and it is shown in Table 12.

CHAPTER 5
CONCLUSION AND RECOMMENDTIONS

5.1 Conclusion

The SRBC has been modified by adding MPPT controller which has improved the performance as this results in almost zero P_{BD} and decreases ripples compared to conventional SRBC It is found that by implementing MPPT controller with SRBC, the output voltage and output current have increased by approximately 12% - 13% for both CCM and DCM conditions. Combination of MPPT and SRBC in CCM mode is better compared to DCM because the output current is higher. Moreover, it has lower output ripple peak-to-peak for both voltage and current. For all evaluated circuits namely: the conventional SRBC, MPPT with SRBC and MPPT-AGD with SRBC, it shows that CCM can produce higher output current when operating compared to DCM. On the other hands, the output peak-to-peak ripple for both voltage and current are higher when it is operated in DCM compared to CCM for MPPT-SRBC and MPPT-AGD with SRBC.

In addition to that, the MPPT and MPPT-AGD with SRBC circuits are compared with AGD-SRBC, compensator with AGD and the parallelism of the SRBC's switches. It has shown that by applying MPPT directly to M_1 switch, this produces the highest output current and reduces output peak-to-peak ripple for voltage and current. It also produces approximately 3V for both CCM and DCM. Improvement of almost 12%, 13%, 3% and 2% for output current are achieved when MPPT is implemented with SRBC compared to CGD, AGD-SRBC, Compensator-AGD and parallelism respectively for both CCM and DCM conditions.

5.2 Recommendations

Some improvements and modifications have to be done in order to upgrade the MPPT controller. This is because some drawbacks have been detected when the controller is applied to the SRBC circuit. Investigations on the issues of V_{ds1} and V_{node} of the MPPT with SRBC have to be investigated thoroughly so that an accurate output can be achieved. Even though simulations have shown that MPPT controller can improve the performance of the conventional SRBC, a real prototype needs to be constructed in order to prove to the theory.

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APPENDICES

APPENDICES A

GANTT CHART FOR FINAL YEAR PROJECT 1

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	Selection and Confirmation of Project Title	■																			
2	Literature review of SRBC and dead time	■	■	■	■																
									M												
3	Submission of Preliminary Report				●				I												
									D								S		E		
4	Circuit design SRBC					■	■	■									T		X		
									S								U		A		
5	Submission of Progress Report								E	●							D		M		
									M								Y				
6	Literature review on MPPT controller						■	■	E	■	■										
									S								W		W		
7	Literature review on MPPT controller								T	■	■	■	■	■	■	■	E		E		
									E								E		E		
8	Seminar								R		●						K		K		
9	Simulation PSpice								B			■	■	■	■	■					■
									R												
10	Submission of Interim Draft Report								E				●								
									A												
11	Submission of Interim Final Report								K						●						
12	Oral Presentation															●					

APPENDIX B

ype II compensator MATLAB codes:

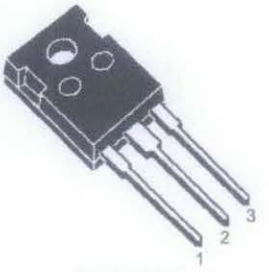
```
 Calculates all the values and plots all the graphs for a Type II

nction buck()

d = input(' Enter input voltage ');
o = input(' Enter output voltage ');
r = input(' Enter reference voltage ');
 =  input(' Enter the load ');
sw = input(' Enter Switching Frequency in MHz ');
ipple = input(' Enter allowed percentage ripple ');
sw = fsw*1E6
eltaV = (Ripple/100)*Vo
C = Vo/Vd;
 = input(' Enter value of Cin uF ' );
 = C*1E-6;
 = input (' Enter value of Lin uF ');
 = L*1E-6;
1 = input(' Enter value of R1 (K) between 2 & 5 ');
1 = R1*1E3;
C = input(' Enter value of ESR ');
L = input(' Enter value of DCR ');
BW = 0.3*fsw
ESR = 1/(2*3.1415926535*rC*C)
LC = 1/(2*3.1415926535*sqrt(L*C))
z2 = (FESR/FLC)^2*(DBW/FESR)*(Vr/Vd)*R1
z2 = 10/(2*3.14159*Rz2*FLC)
p1 = Cz2/((3.14159*Rz2*Cz2*fsw)-1)
 = tf('s');
 Transfer Function of Buck Converter
 = Vd/Vr; % 1/Vr is the effect of PWM
 = 1+s*(rC*C);
 = 1+s*((L+((rC+rL)*R*C))/R)+(s^2)*(L*C);
uck = (G*(N/D));
igure(1)
argin(Buck)
% transfer function of compensator
1 = 1/(s+(1/Rz2*Cz2));
1 = s+(1/(Rz2*Cz2));
N2= s+(1/((R1+Rz3)*Cz3));
0 = s;
1 = s+((Cp1+Cz2)/(Rz2*Cp1*Cz2));
D2 = s+(1/(Rz3*Cz3));
ype2 = G1*((N1)/(D0*D1));
igure(2)
ode(Type2)
rid
%Total open loop transfer function of Buck Converter.
uckType2 = Buck*Type2
igure(3)
argin(BuckType2)
rid
```

IRFP250

N-CHANNEL 200V - 0.073Ω - 33A TO-247
PowerMesh™ II MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
RFP250	200V	< 0.085Ω	33 A

TYPICAL $R_{DS}(on)$ = 0.073Ω
EXTREMELY HIGH dv/dt CAPABILITY
100% AVALANCHE TESTED
NEW HIGH VOLTAGE BENCHMARK
GATE CHARGE MINIMIZED



TO-247

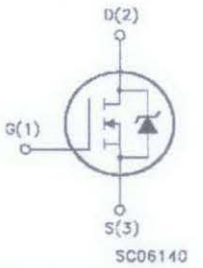
ESCRIPTION

ıe PowerMESH™ II is the evolution of the first ɜneration of MESH OVERLAY™. The layout re-ıements introduced greatly improve the Ron*area ɟure of merit while keeping the device at the lead-g edge for what concerns swithing speed, gate ıarge and ruggedness.

PPLICATIONS

HIGH CURRENT, HIGH SPEED SWITCHING
UNINTERRUPTIBLE POWER SUPPLIES (UPS)
DC-AC CONVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT

INTERNAL SCHEMATIC DIAGRAM



BSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate- source Voltage	±20	V
I_D	Drain Current (continuos) at T_C = 25°C	33	A
I_D	Drain Current (continuos) at T_C = 100°C	20	A
I_{DM} (●)	Drain Current (pulsed)	132	A
P_{TOT}	Total Dissipation at T_C = 25°C	180	W
	Derating Factor	1.44	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	5	V/ns
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

)Pulse width limited by safe operating area

(1)I_{SD} ≤33A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$

HERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.66	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
Rthc-sink	Thermal Resistance Case-sink Typ	0.1	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

VALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	33	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	600	mJ

LECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

FF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	200			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			50	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30V			±100	nA

N (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 16A		0.073	0.085	Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, V_{GS} = 10V	33			A

YNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 16A	10	25		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2850		pF
C_{oss}	Output Capacitance			420		pF
C_{rss}	Reverse Transfer Capacitance			120		pF

.ECTRICAL CHARACTERISTICS (CONTINUED)

VITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 100V, I_D =16 A		25		ns
t_r	Rise Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 3)		50		ns
Q_g	Total Gate Charge	V_{DD} = 160V, I_D = 33 A,		117	158	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10V, R_G = 4.7Ω		15		nC
Q_{gd}	Gate-Drain Charge			50		nC

VITCHING OFF

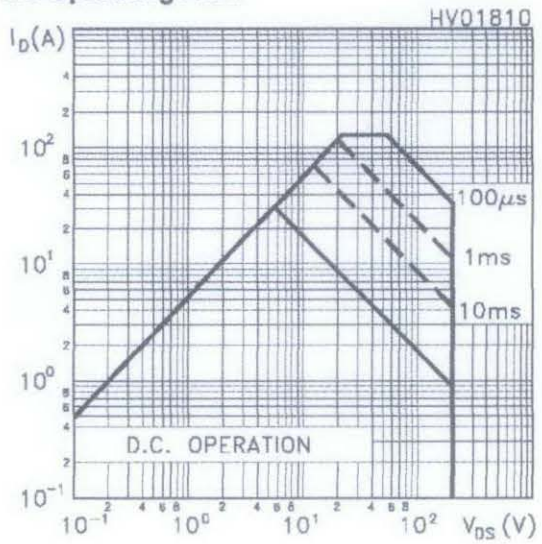
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 160V, I_D = 16 A,		60		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		40		ns
t_c	Cross-over Time			100		ns

)URCE DRAIN DIODE

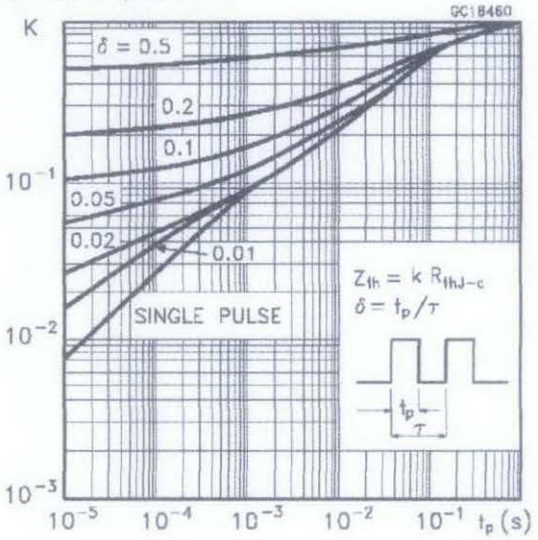
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				33	A
I_{SDM} (2)	Source-drain Current (pulsed)				132	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 33 A, V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 33 A, di/dt = 100A/µs,		370		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 100V, T_j = 150°C (see test circuit, Figure 5)		5.4		µC
I_{RRM}	Reverse Recovery Current			29		A

e: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

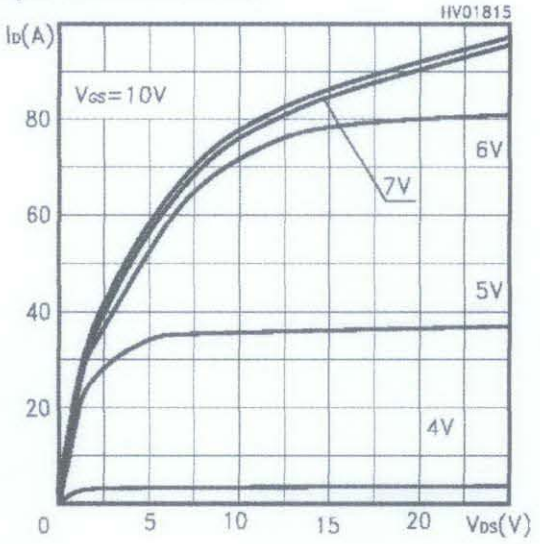
afe Operating Area



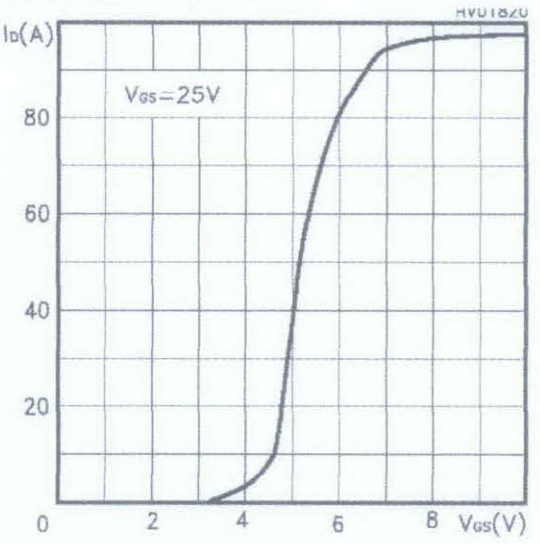
Thermal Impedance



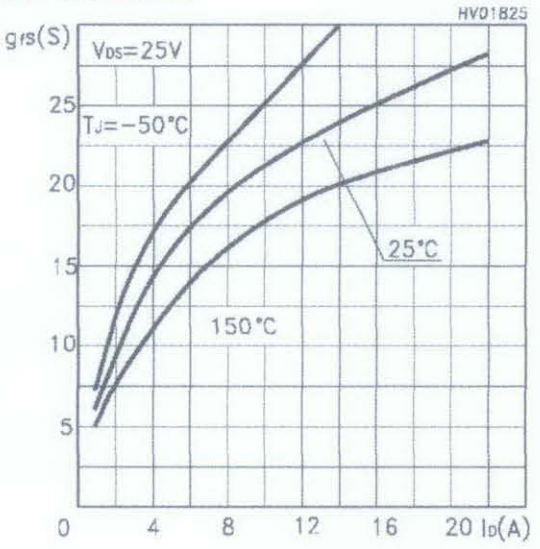
utput Characteristics



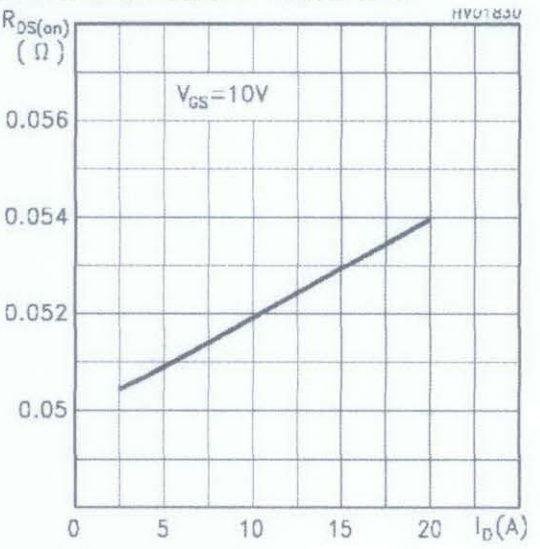
Tranfer Characteristics



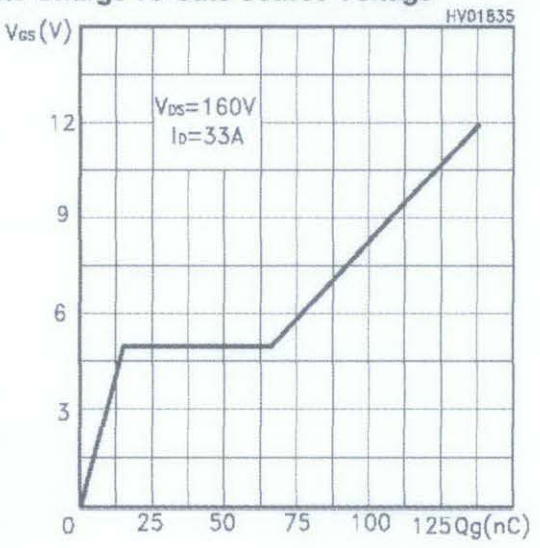
ranconductance



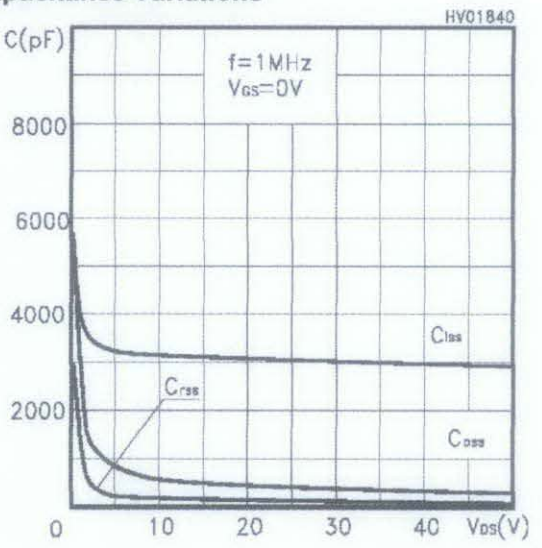
Static Drain-Source On Resistance



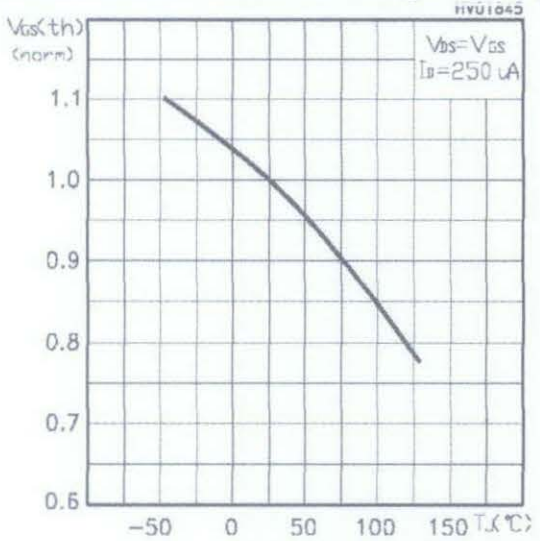
ate Charge vs Gate-source Voltage



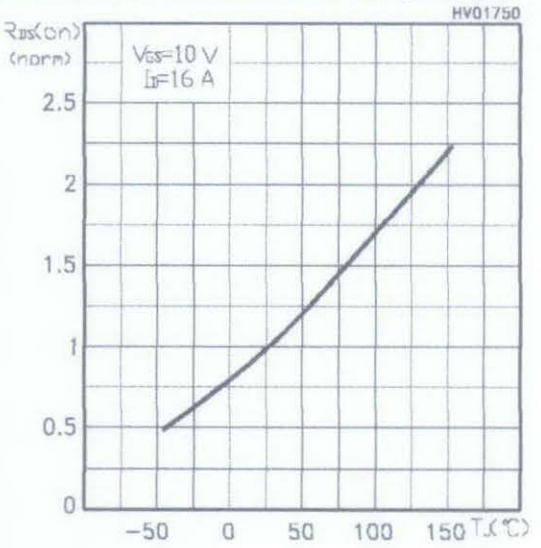
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

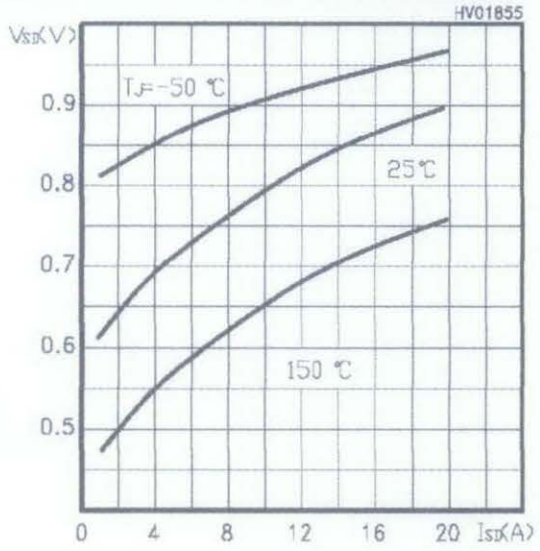


Fig. 1: Unclamped Inductive Load Test Circuit

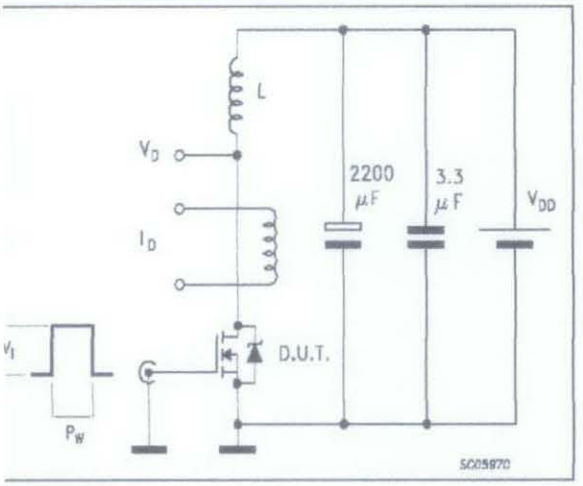


Fig. 2: Unclamped Inductive Waveform

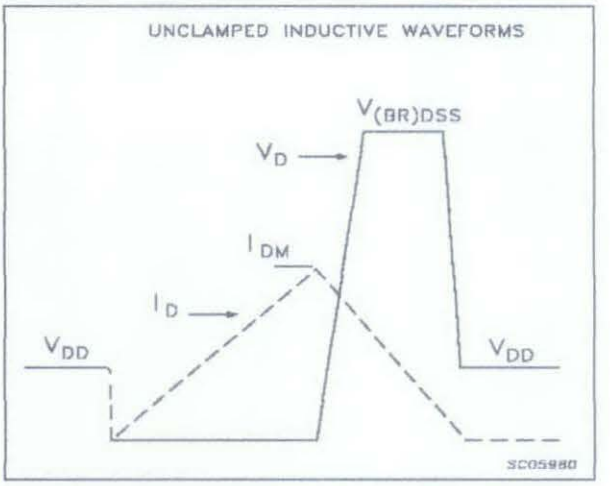


Fig. 3: Switching Times Test Circuit For Resistive Load

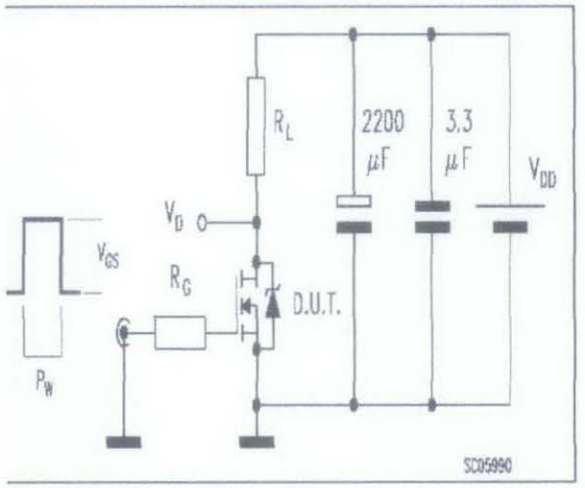


Fig. 4: Gate Charge test Circuit

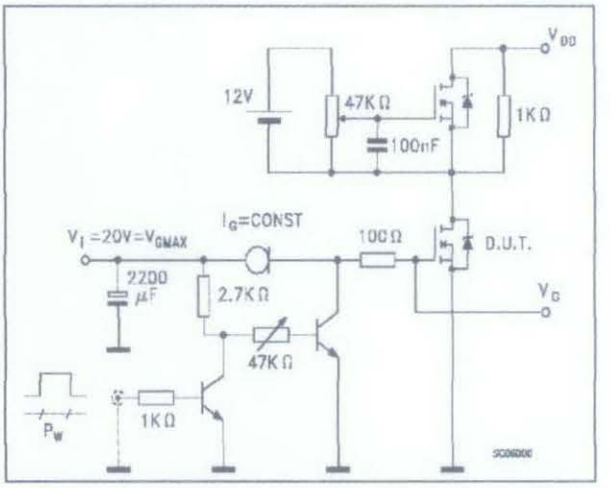
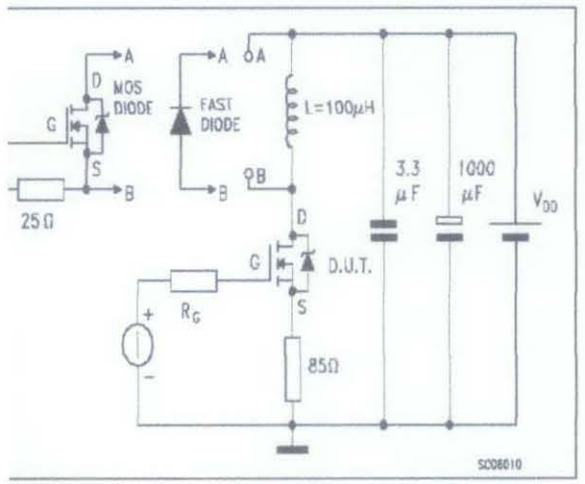


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118