THE STUDY OF MOSFETS PARALLELISM AND EFFECTS ON SRBC CIRCUIT

By

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FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
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CERTIFICATION OF APPROVAL

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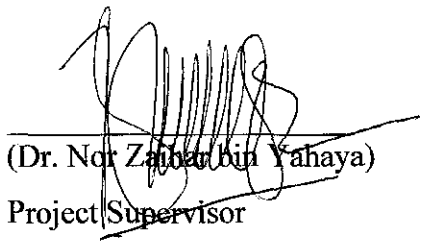
Approved by,



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TRONOH, PERAK

May 2011

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

NUR AMIZA MAKHTAR

ABSTRACT

This project is about the study of MOSFETs parallelism and its effects on SRBC circuit. Output current in the circuit will always be the main concern. Other main issue is high conduction loss. Hence, MOSFETs parallelism is used to produce high output current and reduce body diode conduction loss. The applied circuit is Synchronous Rectifier Buck Converter (SRBC). There are several configurations in paralleling the MOSFETs at both switches from 1×1 up to 4×4. The simulation work will be conducted into two modes which are in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). Analysis will be carried out in order to choose the optimized configuration that gives the best outcome based on design requirement such as produce high output current, minimal body diode conduction loss and 3V as output voltage. It is found that for CCM, the optimized configuration is (*S1*:4, *S2*:1). As for DCM, the optimized configuration is (*S1*:4, *S2*:3). Once the optimized configuration has been chosed, it will then compare to other SRBC circuits. They are SRBC with Conventional Gate Driver (CGD), Adaptive Gate Driver (AGD), compensator and AGD, and lastly SRBC with MPPT controller. For CCM, it is found that among all, MOSFETs parallelism can produce the second higher output current by 863.84 mA as SRBC with MPPT controller produces the highest output. Whilst for DCM, MOSFETs parallelism also produce second higher output current and successfully eliminate body diode conduction loss. Further details will be discussed in this report.

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TABLE OF CONTENTS

ABSTRACT . . . . . **iii**

ACKNOWLEDGEMENT . . . . . **iv**

LIST OF FIGURE . . . . . **viii**

LIST OF TABLES . . . . . **x**

LIST OF ABBREVIATIONS . . . . . **xi**

CHAPTER 1: INTRODUCTION **1**

1.1 Research Rationale . . . 1

1.2 Problem Statement . . . 1

1.3 Objective 2

1.4 Scope of Study . . . 2

CHAPTER 2: LITERATURE REVIEW/THEORY . **3**

2.1 Pulse Width Modulation . . 3

2.1.1 Types of PWM. . . *3*

2.2 MOSFET 6

2.2.1 Switching Characteristics of MOSFET *6*

2.2.2 Turn On and Off Characteristics *7*

2.2.3 MOSFET Conduction Loss . *8*

2.2.4 Body Diode Conduction Loss . *10*

2.3 MOSFETs Parallelism. . . 12

2.3.1 Parallel Operation of MOSFET *12*

2.3.2 Worst-Case of N Parallel MOSFET *14*

2.3.3 MOSFETs in Series . . *15*

2.3.4 Summary of Journals Related to MOSFETs Parallelism . *16*

2.4 Synchronous Rectifier Buck Converter. 17

2.4.1 Advantages of SRBC . . 18

2.4.2 Drawbacks of SRBC . . 18

2.5 Adaptive Gate Driver . . . 19

2.5.1 Advantages and Disadvantages of AGD 19

2.6 Compensator 20

CHAPTER 3: METHODOLOGY 21

3.1 Procedure Identification . . 21

3.2 Research 22

3.3 Circuit Design. . . . 22

3.3.1 Circuit Schematics . . 23

3.3.2 PWM Setting . . . 27

3.3.3 Value for Inductor, Capacitor, Resistor 28

3.4 PSPICE Simulation . . . 29

3.5 Analysis Performance. . . . 29

CHAPTER 4: RESULTS AND DISCUSSION . . 30

4.1 Chapter Overview . . . 30

4.2 Data Gathering and Analysis . 31

4.2.1 Pulse Width Modulator . 31

4.2.2 Voltage at PWM1. . . 32

4.3 Continuous Conduction Mode (CCM) Conventional SRBC Circuit 33

4.3.1 Output Current CCM . . 35

4.3.2 Body Diode Conduction loss CCM 37

4.3.3 Choosing Optimize Configuration for CCM 39

4.3.4 Optimized Configuration for CCM 41

4.4 Discontinuous Conduction Mode (DCM) Conventional SRBC Circuit 44

4.5 Comparison with Other Circuits for CCM 51
4.6 Comparison with Other Circuits for DCM 59

CHAPTER 5: CONCLUSION AND RECOMMENDATION 64
5.1 Conclusion 64
5.2 Recommendation . . . 65

REFERENCES 66

APPENDICES 69
APPENDIX A: Gantt Chart of the Project. . . . 69
APPENDIX B: SRBC Circuit with MOSFETs Parallelism Technique 70
APPENDIX C: Circuits for Comparison Part. . . . 102

LIST OF FIGURE

Figure 1	Analog PWM Generation	4
Figure 2	Pulse Modulator Circuit.	5
Figure 3	N-Channel Enhancement Type MOSFET. . .	6
Figure 4	Turn On and Off Characteristics of MOSFET . .	7
Figure 5	Equivalent Circuit of MOSFET. . . .	9
Figure 6	MOSFETs Switches in SRBC circuit . . .	9
Figure 7	Body Diode Conduction	10
Figure 8	Parallel Connected MOSFETs	13
Figure 9	MOSFETs Parallel	15
Figure 10	Conventional Synchronous Rectifier Buck Converter .	17
Figure 11	Adaptive Delay Control Scheme . . .	19
Figure 12	Project Activities Flow Chart	21
Figure 13	Conventional SRBC circuit using Direct PWM. .	23
Figure 14	Example of SRBC Circuit with MOSFETs Parallelism Technique (*S1*:4; *S2*:4).	25
Figure 15	Node Voltage, V_N graph.	26
Figure 16	Waveform of the Voltage Differential at PWM .	31
Figure 17	Node Voltage.	32
Figure 18	Graph of Output Current, I_o for CCM. . . .	36
Figure 19	Graph of Output Voltage, V_o and Output Current, I_o for CCM	37
Figure 20	Graph of Body Diode Conduction for CCM. . .	38
Figure 21	Node Voltage, V_N for CCM	39
Figure 22	Body diode conduction time for chosen configurations for CCM	40
Figure 23	Output Current Comparisons for CCM. . .	41
Figure 24	Node Voltage for optimize configuration for CCM. .	42

Figure 25 Graph of Output Current, I_o for DCM. . . . 46
Figure 26 Graph of Output Voltage, V_o and Output Current, I_o for DCM 47
Figure 27 Graph of Inductor Current for DCM.. . . . 48
Figure 28 Output Current Comparisons for DCM . . . 49
Figure 29 Inductor Current Comparisons for DCM. . . 50
Figure 30 Average Output Voltage Comparisons. . . . 54
Figure 31 Output Current Comparisons. 55
Figure 32 Output Voltage Ripple Comparisons. . . . 56
Figure 33 Output Current Ripple Comparisons. . . . 57
Figure 34 Body Diode Conduction Loss Comparisons. . . 58

LIST OF TABLES

Table 1.1	Summary of Related Journals	16
Table 3.1	Design Parameter.	22
Table 3.2	MOSFETs parallelism configurations . . .	24
Table 3.3	PWM Setting.	28
Table 4.1	Component Value for CCM Mode . . .	33
Table 4.2	CCM SRBC Circuit with MOSFETs Parallelism. .	34
Table 4.3	Configurations with Lowest Body Diode Conduction.	38
Table 4.4	Component Value for DCM Mode. . . .	44
Table 4.5	DCM SRBC Circuit with MOSFETs Parallelism. .	45
Table 4.6	Comparison SRBC circuit with controller for CCM..	52
Table 4.7	Improvement of CGD, AGD, Compensator-AGD, Parallelism and MPPT for CCM.	53
Table 4.8	Comparison SRBC circuit with controller for DCM..	60
Table 4.9	Improvement of CGD, AGD, Compensator-AGD, Parallelism and MPPT for CCM.	61

LIST OF ABBREVIATIONS

AGD	Adaptive Gate Drive
CCM	Continuous Conduction Mode
CGD	Conventional Gate Drive
DCM	Discontinuous Conduction Mode
MOSFET	Metal Oxide Field Effect Transistor
MPPT	Maximum Power Point Tracker
PWM	Pulse Width Modulation
SR	Synchronous Rectifier
SRBC	Synchronous Rectifier Buck Converter

CHAPTER 1
INTRODUCTION

1.1 Research Rationale

High output current is very important for every circuit. It has been identified that paralleling MOSFETs is one way to increase output current and also reduce body diode conduction loss. This work is to investigate the effect of MOSFETs parallelism. The applied circuit used in this project is Synchronous Rectifier Buck Converter (SRBC). Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) are included in this investigation. Optimized configuration will be chosen for both DCM and CCM.

1.2 Problem Statement

Output current in the circuit will always be the main concern. Other main issue is high conduction loss. It is known that by having several MOSFET switches connected in parallel, not only can help in increasing output current, but also able to reduce conduction loss. This work is to investigate the possible benefits and problems associated with MOSFETs paralleling operation. SRBC will be used as applied circuit. SRBC is widely used in low power DC-DC such as in mobile application, computer processor unit or part of the battery charging power module circuit. There are several configurations of MOSFETs paralleling at the switches that can be connected. Hence, the research is to find out the differences in the result and identify which configuration is the most effective and give best output outcomes.

1.4 Objective

Upon completing the project, few objectives will be achieved. They are:

- To understand concept of MOSFETs parallelism.
- To relate the effect of MOSFETs parallelism on the converter's performance (conventional SRBC circuit and SRBC circuit with controller).
- To compare several configurations of MOSFETs parallelism on other converters which are, SRBC with CGD, SRBC with AGD, SRBC with compensator and AGD and SRBC with MPPT controller.
- To identify optimized configuration of MOSFETs parallelism for CCM and DCM.
- To analyze the results for CCM (Continuous Conduction Mode) and DCM (Discontinuous Conduction Mode).

1.5 Scope Of Study

This project will be using PSPICE simulation to simulate few different configurations of MOSFET parallelisms in SRBC. The difference of each configuration will be the placement of multiple MOSFETs in parallel whether it is either connected to switch 1 or switch 2 or both. Study of the circuit and its component are very crucial to have better understanding throughout the research. Overall, the project scope can be divided into two stages. The first stage is to study the theories of MOSFETs parallelism in SRBC circuit and getting familiar with PSPICE simulation. The second stage is to model and simulate few configurations of MOSFETs parallelism using PSPICE. After that, analysis of the results will be concluded.

CHAPTER 2
LITERATURE REVIEW

2.1 Pulse Width Modulation (PWM)

PWM techniques are broadly utilized in digital-to-analog conversion, power conversion and also DC-DC voltage conversion. PWM creates analog outputs by using 'high' and 'low' signal of digital pulses. It adjusts the duty ratio; *D*. Duty Ratio refers to the amount of time in the period that the pulses are active or high. It is typically specified as a percentage of the full period to generate voltage in the range of 0 % to 100 % from the maximum supply voltage, depending on the PWM resolution. The PWM resolution is the maximum of pulses that can be packed into a PWM period. For higher switching frequency, f_s, the resolution will be lower. A PWM period is an arbitrary time given particularly to any switching circuit [1].

2.1.1 Types of PWM

PWM can be divided into two types which are digital and analog. Compared to the analog pulse width modulator, digital pulse width modulators are simpler. However their resolution is poor. This is because they control the duty-cycle by a binary increment fashion. As for the analog PWMs controllers, they are more complex than the digital ones, but, they are more efficient. This is due to the high resolution if operating at low speed. The operation of an analog pulse width modulator is mainly based on the comparison of a voltage proportional to the duty-cycle of the signal to be generated and a reference triangular-wave [2].

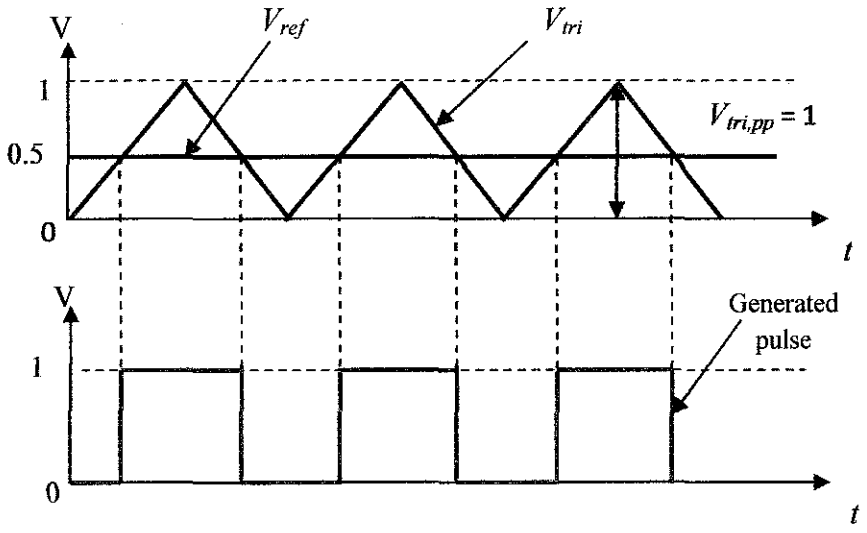

Figure 1 Analog PWM Generation

The common conventional analog PWM signal is generated by comparing the triangular waveform voltage, V_{tri} with constant reference voltage, V_{ref} using a ramp generator and a comparator block as shown in Figure 1. The comparator will produce an output each time V_{tri} goes above V_{ref}. For this type of pulse modulator, the width of the pulse can be adjusted by varying the V_{ref}. The output voltage generated by the comparator depends on the swing voltage applied to the comparator. The design is complex and sometimes is not suitable for high frequency operation due to noise [1,3].

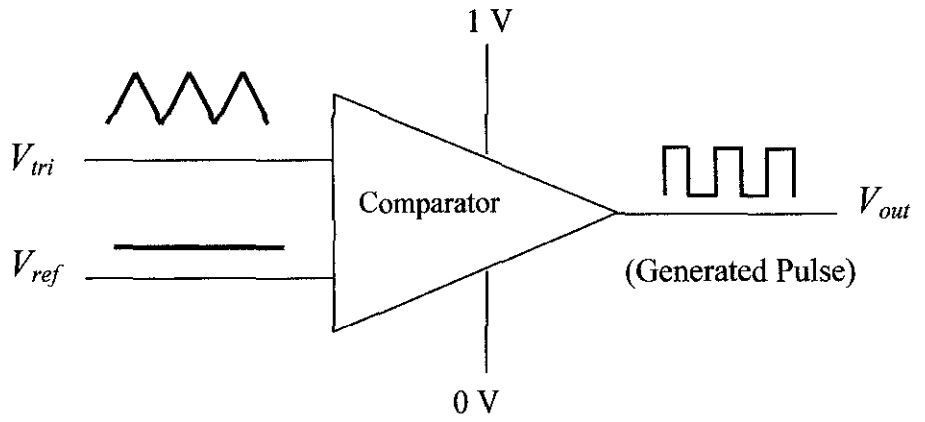

Figure 2 Pulse Modulator Circuit

Figure 2 shows the pulse modulator circuit. If the swing voltage is from 0 V to 1 V, the comparator will produce 1 V when V_{tri} is greater than V_{ref}. Whereas, 0 V will be produced when V_{tri} is less than V_{ref}.

An accurate design of PWM signal is crucial in driving the MOSFET switch especially for gate driver. The range of applied gate voltage must be given above its threshold voltage, V_{th} so that it can turn on with sufficient charge. In megahertz switching frequency, the PWM output normally contains high harmonic distortion and noise, which make the design complicated [1,3, 4].

2.2 MOSFET

2.2.1 Switching Characteristics of MOSFET

The most important parameters in MOSFET switching are gate-source voltage (v_{gs}), drain-source voltage (v_{ds}) and drain current (i_{ds}) as in the figure 3 below:

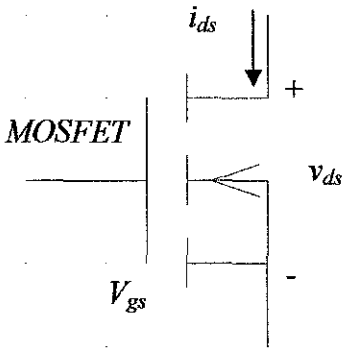

Figure 3 N-Channel Enhancement Type MOSFET

N-channel enhancement type MOSFETS are the most well-known for use in power switching circuits and applications. The drive voltage or voltage applied between gate and source to turn on the MOSFET must exceed a threshold value V_T 4 V although values of 10 V – 12 V are actually needed to ensure the MOSFET is fully conducting. Reducing the drive voltage to below V_T will cause the MOSFET to turn off. [5]

2.2.2 *Turn on and Off Characteristics*

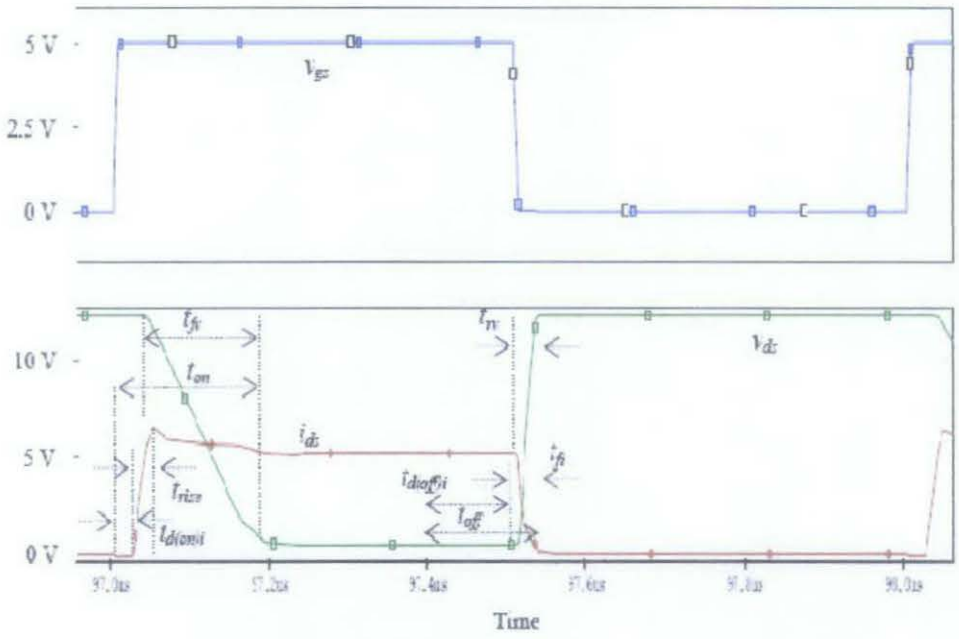

Figure 4 Turn On and Off Characteristics of MOSFET [1]

Turn-on time (t_{on}) and current turn-on delay time ($t_{d(on)i}$) indicate how fast MOSFET reacts during turn-on switching transient. This gives total turn-on time. Increased delay time will eventually limit the maximum switching frequency. The PWM signal received at the gate terminal of the MOSFET can be distorted by the longer turn-on delay. As current rise time (t_{rise}) on the other hand contributes to how fast drain current reaches the load indicating the speed of the circuit. Other parameters such as di/dt of turn-on current, voltage fall time (t_{fv}), dv/dt turn-off voltage, current overshoot and turn-on energy loss (E_{on}) are included in the total turn-on duration.

The turn-off characteristics exhibit the same functions as the turn-on except for the behavior of current, voltage and their related switching times and losses which depend on turn-off duration. Among the parameters are turn-off time (t_{off}), current turn-off delay time ($t_{f(off)}$), current fall time (t_{fi}), voltage rise time (t_{rv}), di/dt of turn-off current, dv/dt of turn-on voltage, voltage overshoot and its

respective turn-off energy loss. Because of the switching loss in MOSFET is critical in high frequency operation, these turn-on and turn-off characteristics must be understood as they contribute to switching losses in the MOSFET. [1,3,4,6]

2.2.2 MOSFET Selection

In most circumstances, MOSFET is preferred as a switching device for high switching frequency operation. In SRBC circuit operation, MOSFETs have to fulfill the system requirement in reducing loss and cost. The selection of MOSFET is based upon the following criteria:

a) Low power dissipation of switching device in megahertz range.

b) Figure of Merit of $R_{ds(on)}$ and gate charge.

c) Turn-on delay time ($t_{d(on)}$), rise time (t_{rise}), turn-off delay time ($t_{d(off)}$) and fall time (t_f) which have to be small for possible good switching performance.

2.2.3 MOSFET Conduction Loss

All components in a DC-DC converter, such as capacitors, inductors and switches are non-ideal. They have their own resistive components, R_{ESR}. Hence, the power dissipation due to the current that through them is unavoidable. When the device is in the on-state, almost all of them dissipate in a MOSFET. Equations (1) and Eq. (2) below show that conduction losses of S_1 and S_2 depend on their $R_{ds(on)}$ and D. [1,3,4,6,7]

$$P_{S1,COND} = (I_{RMS})^2 \times R_{ds\,(on)s1} \times D \quad (1)$$

$$P_{S2,COND} = (I_{RMS})^2 \times R_{ds\,(on)s2} \times (1 - D) \quad (2)$$

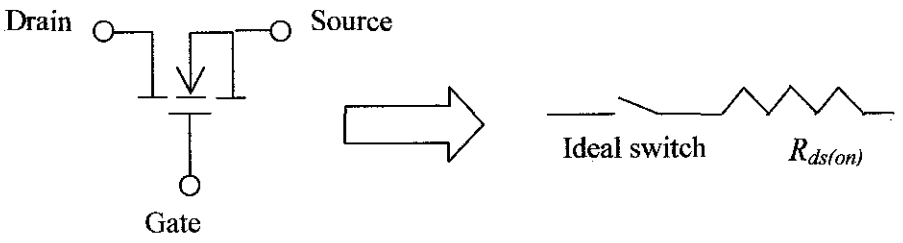

Figure 5 Equivalent circuit of MOSFET

Figure 5 shows the equivalent circuit of MOSFET. The on-resistance components, $R_{ds(on)}$ of MOSFET depends on the junction temperature of the MOSFET. If the temperature is higher, then the $R_{ds(on)}$ would be higher as well.

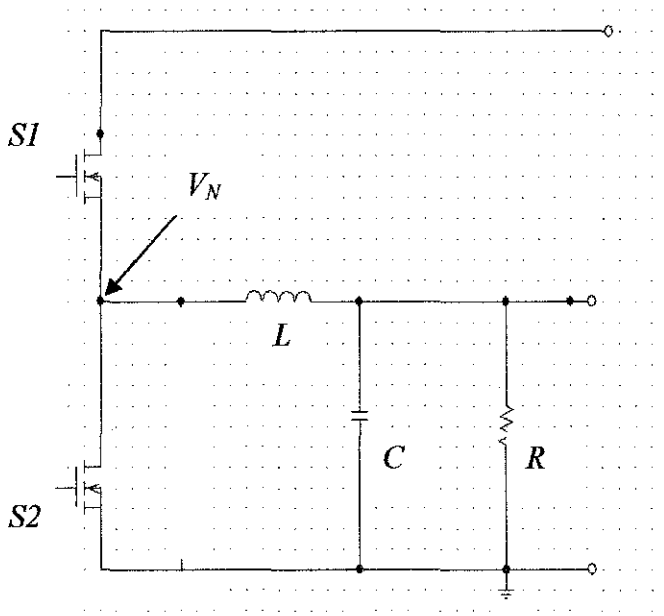

Figure 6 MOSFETs switches in SRBC circuit

The conduction loss can be reduced by minimizing this in both switches *S1* and *S2*. The other way to reduce conduction loss is via multiple paralleling of *S2* switch. This will lower effective $R_{ds(on)}$ since it reduces i2R loss but increase the gate drive loss [8].

2.2.4 Body Diode Conduction Loss

When *S1* and *S2* are off, parasitic body diode of *S2* is forward biased because of the continuity of i_{Lo}, and therefore generating an undershoot of approximately - 0.7 V at V_N [9]. This whole negative duration shows the duration of body diode conduction. *S2* body diode is turned on with ZVS by a circulating current that flows into *L* as soon as *S1* is turned off. Though, *S2* can concurrently conduct with its body diode, creating stored charge that must be removed before *S2* can support voltage. This leads to high switching loss in *S1* and an increase in reverse recovery loss in *S2* body diode. Thus, *S2* needs to be turned off completely before *S1* starts to conduct during T_d. After T_d delay ends, *S2* will start to conduct. As the forward voltage drop across *S2* is much lower than its body diode voltage drop, this will allow I_L to flow through *S2* instead [10]. Fig. 7 shows the effect of the body diode conduction.

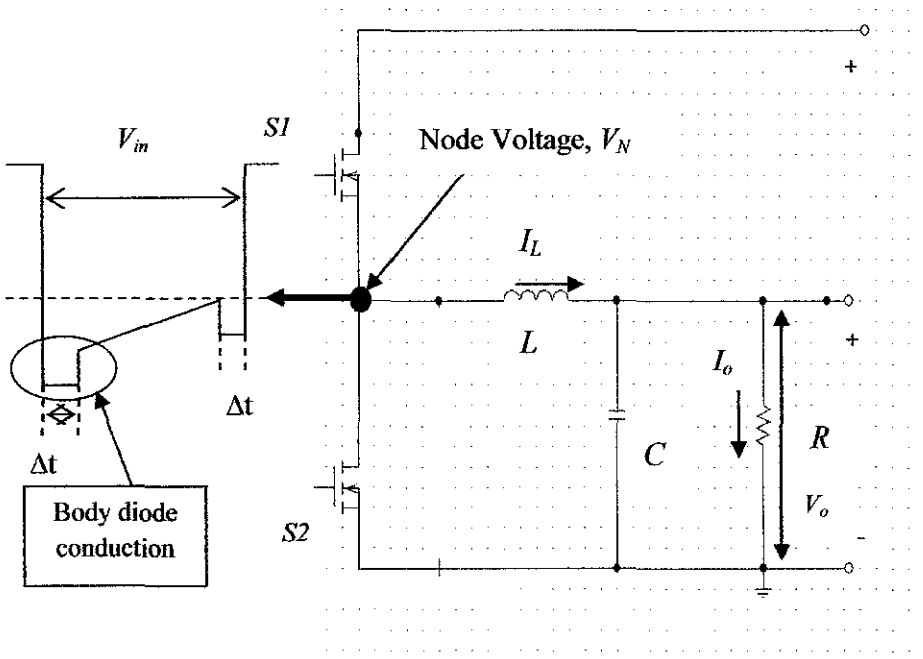

Figure 7 Body Diode Conduction

The effect of body diode is circled in the Figure 7. The period of the body diode conduction is related to T_d. Body diode conduction period will be longer if T_d is longer. Allowing the I_L to flow through the body diode of *S2* switch has a degrading effect on the overall converter's performance since it contributes to the losses. Note that the Δt increases with T_d and so does the body diode conduction loss. This shows that as T_d value increases, the power losses will increase thus affect the performance of the circuit. The equation is given by Eq. (3),

$$P_{bd} = 2 \times V_F \times I_o \times f_s \times \Delta t \quad (3)$$

where

V_F = body diode forward voltage drop

Δt = body diode conduction time

The losses are proportional to the body diode conduction time. A smaller body diode conduction time, Δt will have smaller conduction losses. Therefore, in order to have a low body diode loss, a shorter T_d delay is required. The additional loss due to body diode conduction can be as high as 6 % from overall loss in high frequency low output voltage power stage [11].

2.3 MOSFET Parallelism

A number of MOSFETs can be paralleled to handle higher output currents. Paralleling MOSFETs can also be used for further reduction in the on-resistance of the rectifying path. On the other hand, MOSFETs need to be paralleled to decrease the conduction loss.

2.3.1 Parallel Operation of MOSFETs

The parallel connection of MOSFETs allows higher load currents to be handled by sharing the current between the individual switches. Because MOSFETs have a positive temperature coefficient they can be paralled without the need for source resistors (BJTs need small emitter resistors that provide negative feedback). If one MOSFET starts to draw slightly more current than the others it heats up and its impedance increases which results in the current through it decreasing. Parallel MOSFETs should be mounted close together so that the gate drive impedances are the same and all transistors switch at the same time. [5,12].

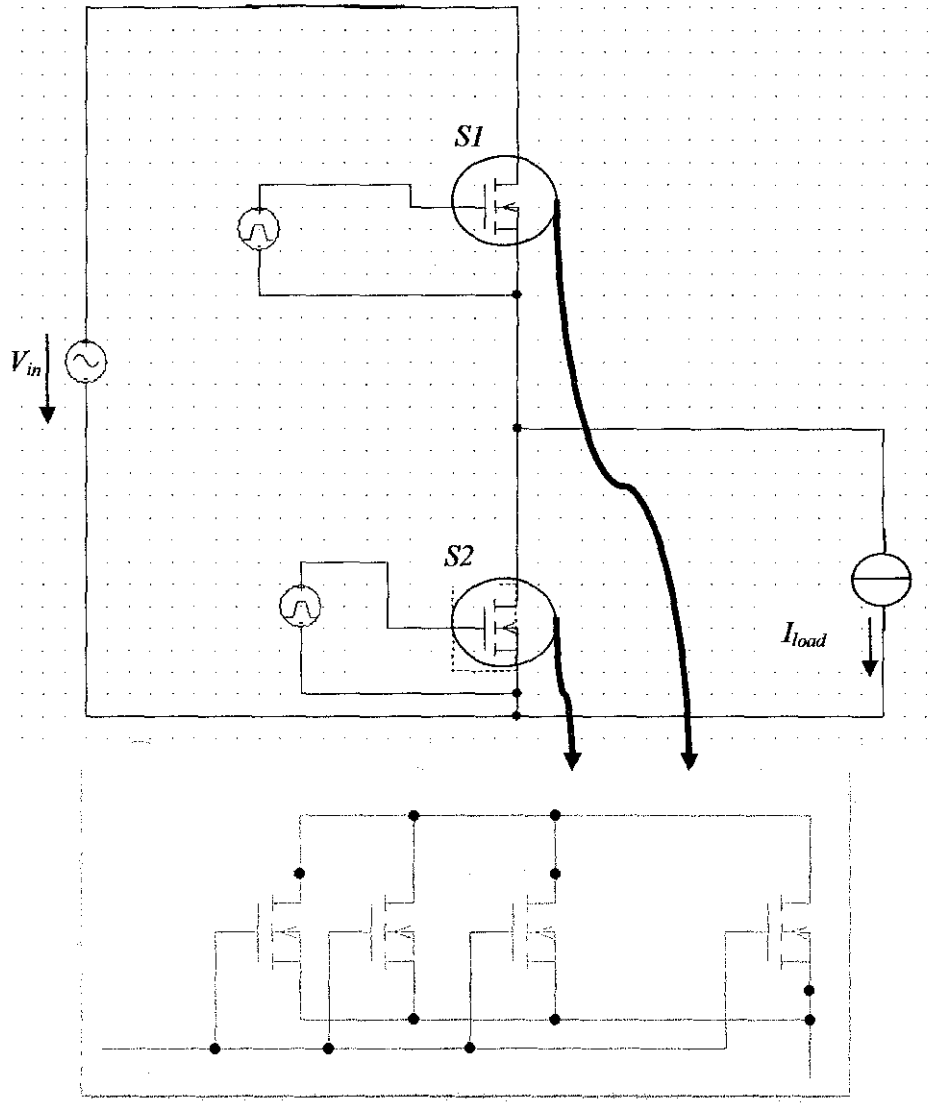

Figure 8 Parallel Connected MOSFETs

Paralleling MOSFETs might be used either for reduction of the on-resistance for efficiency considerations or for increasing the current handling capability of the converter.

Without the need of equalizing resistors, dynamic current balancing transformers, or active gate drive feedback, MOSFETs can operate in parallel. Nevertheless, current sharing must be assured between the devices to prevent current and thermal stresses on any of the devices. Transient current sharing turn out to be important at high switching frequencies. The transient current unbalance

can be limited by power circuit layout, device parameter watching and appropriate gate drive design. At lower switching frequencies the MOSFET on resistance strongly influences current sharing, but transient current sharing remains an important design factor [13].

2.3.2 Worst-Case for N Parallel MOSFETs

The worst-case analysis has to take the components' spread into consideration and requires specified ranges. Subjects to tolerances are the on-resistances at reference temperature, *R0i*, the thermal impedances, *Zthi*, and the branch inductances, *Li*. As for the on-resistances, usually only the maximum value is specified, which means that *R0i* lies between zero and *R0(Max)*.

Worst-Case Modelling

Increasing the path impedance of a first branch causes a temperature rise in the devices of the other branches. Hence, in worst-case, all but one branch must exhibit the maximum specified electric impedance, thereby worsening the device temperature of the lowest impedance branch, or also referred to as critical branch. Further, it is obvious that in worst-case, the thermal impedance of every branch must be at the maximum specified value, i.e. highest thermal resistance and lowest thermal capacitance.

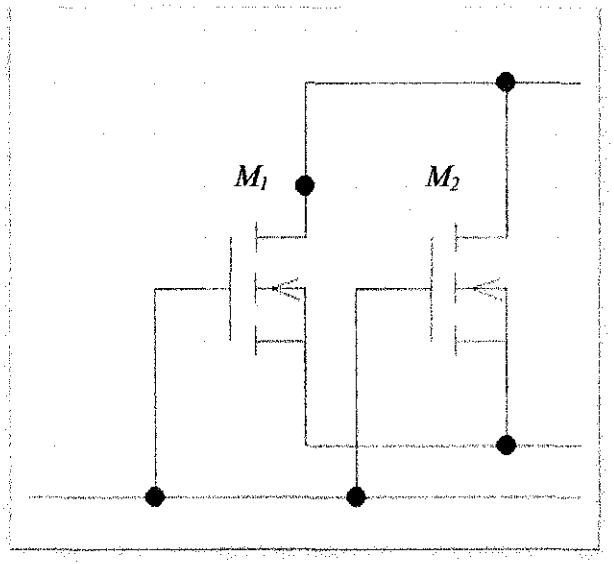

Figure 9 MOSFETs parallel

Therefore, the configuration of figure 9 with only two branches in parallel can be taken to model the general worst-case scenario. If M_1 represents the critical branch, worst case is given by Eq. (4) to Eq. (7);

$$R_{01} \equiv R_{0(Crit)} \quad (4) \qquad L_1 \equiv L_{min} \quad (5)$$

$$R_{00} \equiv \frac{R_{0(Max)}}{N-1} \quad (6) \qquad L_0 \equiv \frac{L_{max}}{N-1} \quad (7)$$

L_{max} and L_{min} are the maximum and minimum specified total branch inductances. $R_{0(Crit)}$ is the worst-case resistance (at reference temperature) of the critical branch, which still has to be determined. M_2 represents the remaining N-1 equal MOSFETs in parallel, each of them exhibits the maximum impedance. [14]

2.3.3 MOSFETs in Series

MOSFETs may be operated in series to increase their voltage-handling capability. It is very crucial that the series-connected MOSFETs are turned on and off simultaneously. Or else, the slowest device at turn-on and the fastest device at turn-off might be subjected to the full voltage of the collector-emitter (or drain-source) circuit and that particular device may be destroyed due to a high voltage [15].

2.3.4 *Summary of Journals Related to MOSFETs Parallelism*

Table 2.1 Summary of Related Journals

Paper	Circuit Applied	Advantage(s)	Issue(s)
a) Lopez, T.; Elferich, R.; , "Current Sharing of Paralleled Power MOSFETs at PWM Operation," *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE* , vol., no., pp.1-7, 18-22 June 2006	Half-bridge with constant input voltage and constant output current	-analysis of thermal aspects of paralleling MOSFETs	-in case of ideal switches, branch inductance can affect the worst-case temperature rise in parallel MOSFETs.
b) Hongfang Wang; Wang, F.; , "Power MOSFETs Paralleling Operation for High Power High Density Converters," *Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE* ,	Half-bridge three-level parallel resonant converter	- To achieve high switching frequency, low power loss and small package.	- power MOSFETs parameters may exhibit some discrepancies, which can be worse as temperature varies. - Directly paralleled power MOSFETs, without balancing switching transients current, leads to uneven power dissipation.
c) Lopez, T.; Elferich, R.; , "Static paralleling of power MOSFETs in thermal equilibrium," *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE* , vol., no., pp. 7 pp., 19-23 March 2006	Half-bridge	- investigation of static issues of paralleling MOFSETs, particularly the worst-case scenarios leading to the maximum temperature rise in the devices.	-Maximum operating temperature of each individual junction. - no electro thermal time constants are considered.
d) James B. Forsythe, "Paralleling of Power MOSFETs For Higher Power Output", *International rectifier technical paper*.	Clamped inductive load MOSFET power circuit	-MOSFET generated unbalance can be held to acceptable levels through appropriate driver design or power circuit design or parameter screening.	-parameter mismatched between parallel MOSFETs branches.

2.4 Synchronous Rectifier Buck Converter (SRBC)

Synchronous Rectifier Buck Converter (SRBC) circuit basically comes from the same family as Buck converter. The circuit is called as synchronous rectifier buck converter by replacing diode with another power MOSFET. The *S2* switch is synchronous rectifier since it only turns on after *S1* switch is off. Once the control switch *S1* is turned on, it transfers the energy and charges the inductor current to the load.

The load current will either be operating in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM) by having certain value of output inductance at the load. With respect to the variation of loads, this operating condition influences the SRBC circuit performance [8, 16].

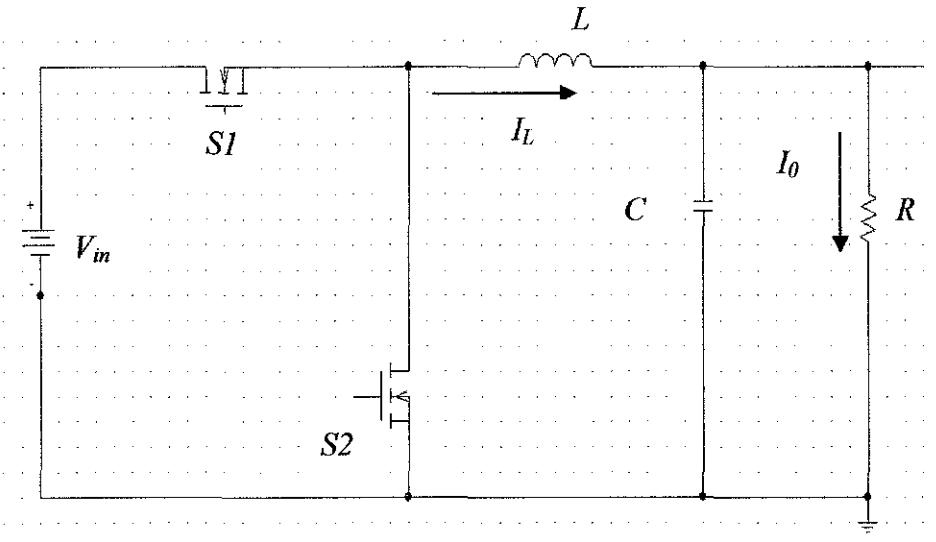

Figure 10 Conventional Synchronous Rectifier Buck Converter

2.4.1 Advantages of SRBC

The advantages of using SRBC in high performance, high-power converters include better efficiency, better thermal performance, lower profile, lower power dissipation, increased quality and improved manufacturing yields though automated assembly processes (higher reliability).

2.4.2 Drawbacks of SRBC

In addition, there are also other issues regarding the design of SRBC circuit which are explained as follows:

1) DCM and CCM operation

   Normally, switch *S1* will experience switching loss and reverse recovery loss in *S2* body diode in any load conditions. But, by allowing I_L to operate in Discontinuous Conduction Mode (DCM), these losses can be minimized. A high output inductance (L) value can be used so that I_L flow will allow *S1* body diode to turn on before *S1* conducts during T_d. This ensures that the current is mostly DC, with the cost of low regulated I_L. On the other hand, switch *S1* will experience hard switching in Continuous Conduction Mode (CCM) since I_L never touches zero. This is opposite to the operation of *S2* where in CCM; current can easily reverse and reduce the body diode recovery loss. Different load currents (varying load resistances) definitely will influence the total loss in the SRBC circuit [1, 17].

2.5 Adaptive Gate Driver (AGD)

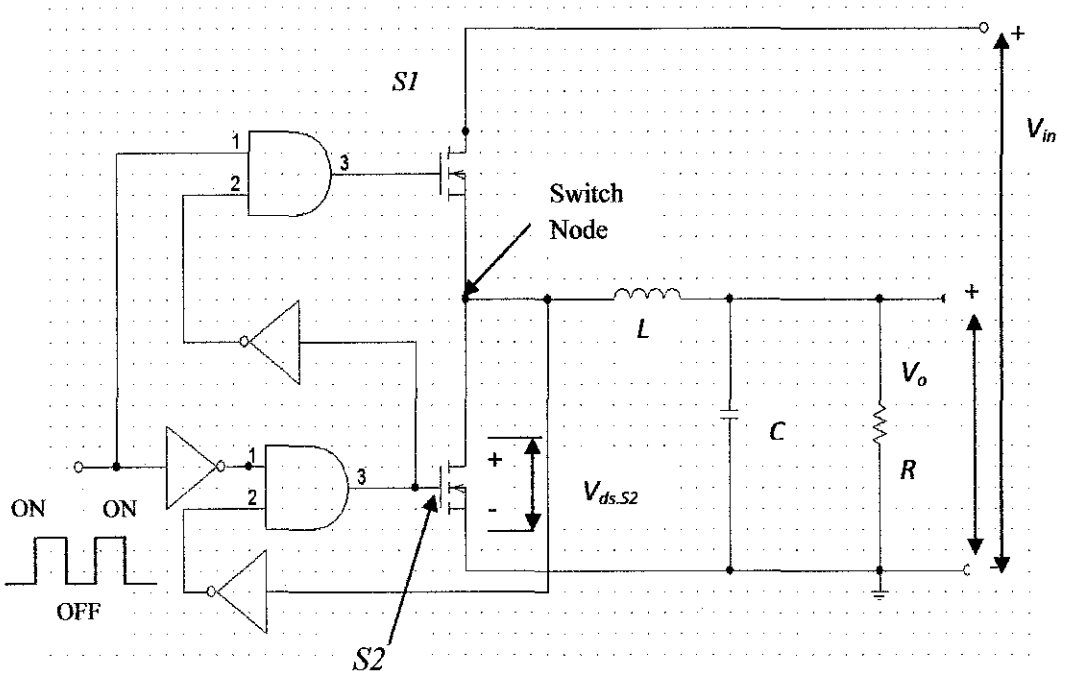

Figure 11 Adaptive Delay Control Scheme

Figure 11 shows the Adaptive Gate Delay Control (AGD) scheme. It uses a control loop that includes a digital delay line where it senses the drain to source voltage, *vds* of the *S2*. Then, it will adjust the digital delay line according to the amount of delay that should be applied to turn on *S2*. Therefore, *S2* is turned on only when the switch node voltage equals to zero.

2.5.1 Advantages and Disadvantages of AGD

The advantage of AGD is that the adjustment of the delay can be made adaptively according to the type of MOSFET used. While the disadvantages of AGD is the variation of body diode conduction time interval may not easy to predict. This is because of the logic components used as the feedback circuit. Each of the components has its own propagation delay that may indirectly increase the T_d between the pulses.

The ideal adaptive gate driver should be able to:

- Minimize the reverse recovery body diode conduction period.
- Avoiding shoot through and cross conduction problems.

The adaptive gate driver should be designed to be as fast as possible to eliminate the diode conduction periods and this includes the delay through the gate driver itself. To do so, a simple and fast detection method has been used to equalize the delay time needed to turn on the power FETs before the diode conducts. This method is based on detecting the voltage changes on V_{DS} of the S_2 and comparing it with a programmable threshold voltage using controlled threshold digital inverter [18].

2.6 Compensator

The compensation circuit design is a very important point for system performance. Furthermore, it is important to note that one of the challenges is to choose low values of compensation capacitors to stabilize the system with a very limited available space.

The advantage of design good compensator is the ability to achieve high switching frequency which provides the opportunity to design high bandwidth loop compensation. The accepted feedback design should have the following characteristics:

a) *DC gain* should be high for better system regulation.
b) System Unity-Gain Bandwidth (UGB) should be as high as possible to decrease overshoot and undershoot.
c) Phase margin is preferred being more than 45 degree.
d) Error amplifier gain at switching frequency should be designed with appropriate enough value to prevent jitter of the switching waveform [18].

CHAPTER 3
METHODOLOGY

3.1 Procedure Identification

The project activities flow is shown in Figure 12.

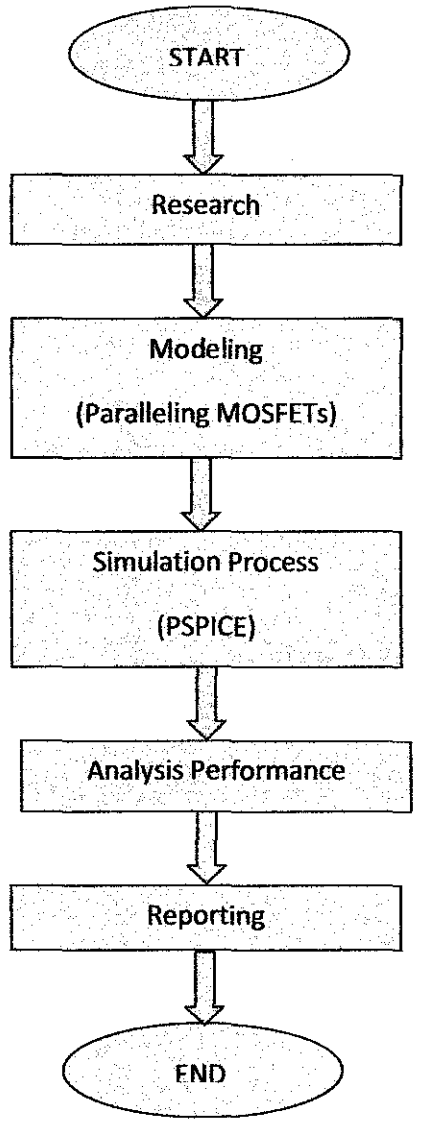

Figure 12 Project Activities Flow Chart

Figure 12 shows the flow of activities during Final Year Project 1 and 2. The project starts with research findings followed by modeling the circuits. After that, simulation of all circuits will be done using PSPICE. The results will then be analyzed.

3.2 Research

The first step of this project is by doing research findings on topics that are related to MOSFETs parallelism, SRBC circuit, PWM techniques and issues raised. The information is gathered from books, technical papers, journals, thesis and internet searches. The purpose of this step is to understand the basic concept.

3.3 Circuit Design

In this project, the applied circuit chosen is Synchronous Rectifier Buck Converter (SRBC). This is because; this circuit is broadly used in the industry and many electronic appliances. This project is divided into two parts; SRBC in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). Basically the circuit used will be the same. Only the parameter of resistor, inductor and capacitor are different. Below is the design specification in the design of SRBC circuit for both modes (DCM and CCM);

Table 3.1 Design Requirement

Input voltage, V_{in}	12 V
Output voltage ,V_o	3 V
Switching Frequency ,f_s	1 MHz
Duty ratio, D	0.25

Table 3.1 shows the design requirement for this project. As this is buck converter, basically the circuit will produce smaller voltage compared to input voltage. The input voltage, V_{in} is 12 V whereas the output voltage, V_o is 3 V. The frequency for this project has been set to 1 MHz and the duty ratio is 0.25.

3.3.1 Circuit Schematics

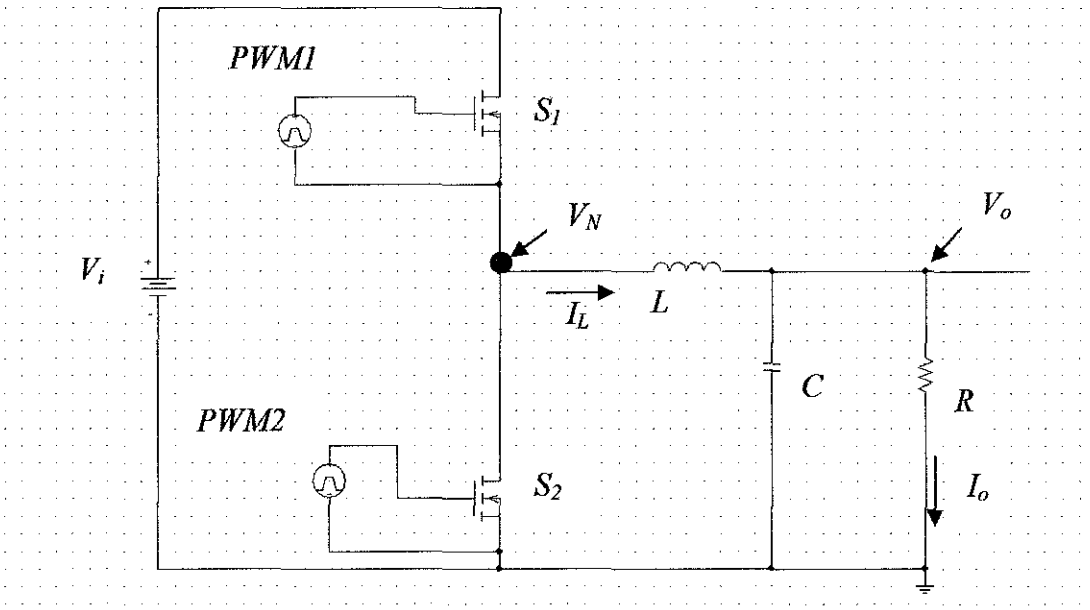

Figure 13 Conventional SRBC circuit using Direct PWM

Figure 13 shows the basic circuit of SRBC using direct Pulse Width Modulation (PWM) technique. The parameter value for each component will be calculated and will be shown in section 3.3.3. PWM technique used at the beginning of this project is to get better understanding on the circuit.

The function of the inductor is to limit the current slew rate (limit the current in rush) through the power switch when the circuit is on and to reduce the ripple in current. The current through the inductor cannot change suddenly. When the current through an inductor tends to fall, the inductor tends to maintain the current by acting as a source. This limits the otherwise high-peak current that would be limited by the switch resistance alone. Also the inductor controls the percent of the ripple [5].

Capacitor provides the filtering action by providing a path for the harmonic currents away from the load. Output capacitance (across the load) is required to minimize the voltage overshoot and ripple present at the output of a step-down converter [5].

The purpose of high frequency of 1 MHz is to reduce the size and component value of inductor and capacitor.

Table 3.2 MOSFETs parallelism configurations

S_1	S_2		S_1	S_2
1	1		3	1
1	2		3	2
1	3		3	3
1	4		3	4
2	1		4	1
2	2		4	2
2	3		4	3
2	4		4	4

Table 3.2 shows the configurations of MOSFETs parallelism used in this project. There are in total of 16 configurations to be simulated. Throughout the project, configurations of MOSFETs parallelism will be mentioned as (*S1*:1; *S2*:1) for example. That means, only one MOSFET at *S1* and *S2*. If it is mentioned as (*S1*:3; *S2*:4), three MOSFETs are paralleled at *S1* and four MOSFETs are paralleled at *S2*. The maximum MOSFETs that are paralleled for this project has been fixed which is up to four for each *S1* and *S2*.

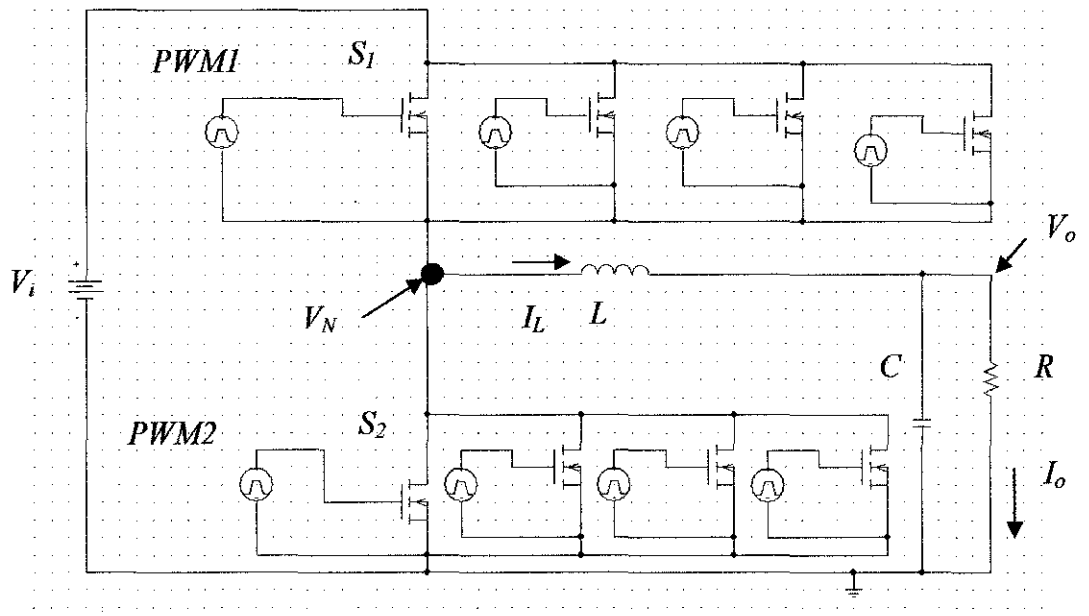

Figure 14 Example of SRBC Circuit with MOSFETs Parallelism Technique

(*S1*:4; *S2*:4)

In Figure 14, it shows one of the MOSFETs parallelism, (*S1*:4; *S2*:4). *PWM1* and *PWM2* settings are fixed for all configurations. Other circuits can be seen in Appendix (B).

Firstly, the circuits are simulated. After that, to ensure that the settings of *PWM1* and *PWM2* are correct, voltage differential at both *PWM* are taken. If the setting is correct, it will give the correct waveform. The voltage consumption at the PWM is 5 V. Then, node voltage, V_N will be observed as the voltage value. At this point, V_N should be the same as voltage input. On the other hand, this point is also important to observe body diode conduction time.

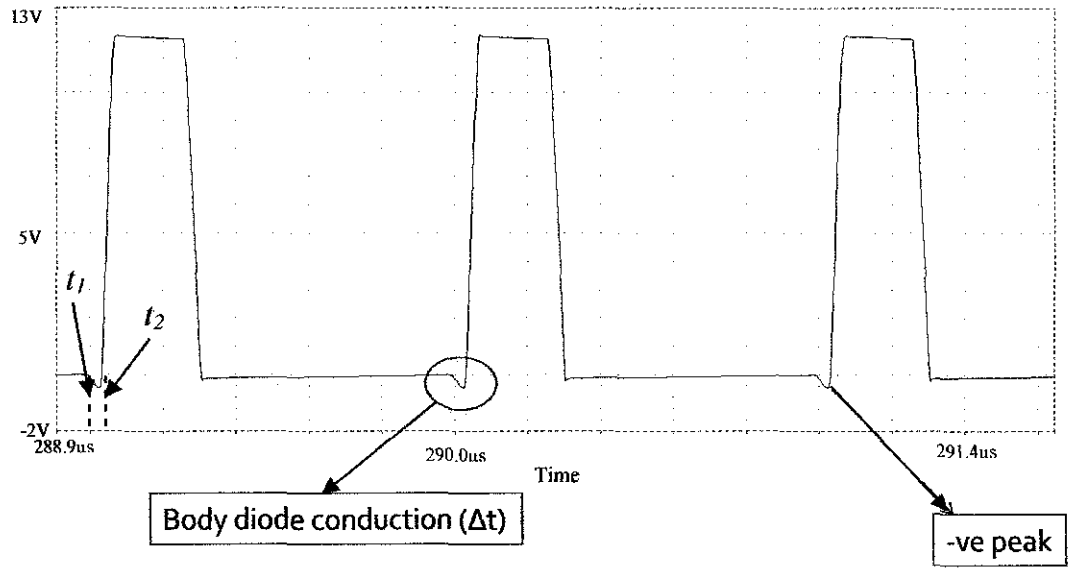

Figure 15 Node Voltage, V_N graph

By putting voltage marker at node voltage, this graph will be obtained as shown in Figure 15. At node voltage, V_N graph, body diode conduction time (Δt) and –ve peak will be observed. The formula for calculating body diode conduction time is given in Eq. (8);

$$\Delta t = t_2 - t_1 \tag{8}$$

After obtaining body diode conduction time, body diode conduction loss, P_{bd} can be calculated using Eq. (9);

$$P_{bd} = V_F \times I_o \times f_s \times \Delta t \tag{9}$$

Next, current marker will be placed at inductor to obtained inductor current, I_L. Here, the value of negative peak and positive peak of the waveform will be taken. Average of the current will also be observed. The importance of monitoring inductor current is to check whether the circuit is operating under CCM or DCM.

After that, the average of output voltage and output current will be observed by placing voltage marker and current marker at resistor, R. Once all the important points have been observed, they will be analyzed. Then, the best configuration for CCM and DCM will be chosen. After that, the best

configuration of MOSFETs parallelism will be compared to other SRBC circuit. They are SRBC with Conventional Gate Driver (CGD), Adaptive Gate Driver (AGD), compensator and AGD, and lastly SRBC with MPPT controller. Again, analysis will be done to compare which have the best output.

3.3.2 PWM Setting

Below is calculation to determine T_s, D, T_{on}, and T_{off} {Eq. (10) to Eq. (13)}

1. To calculate T_s:

$$f_s = \frac{1}{T_s} \tag{10}$$

$$T_s = \frac{1}{f_s} = \frac{1}{1\,MHz} = 1 \times 10^{-6} = 1\mu s$$

$$T_s = T_{on} + T_{off}$$

2. To calculate duty cycle, D:

$$D = \frac{T_{on}}{T_s} = \frac{T_{on}}{T_{on} + T_{off}} \tag{11}$$

$$D = \frac{V_o}{V_i} = \frac{3}{12} = 0.25$$

3. To calculate T_{on}:

$$D = \frac{T_{on}}{T_s} \tag{12}$$

$$T_{on} = D.T_s$$

$$= (0.25) \times (1\mu s)$$

$$= 2.5 \times 10^{-7}$$

$$= 0.25\,\mu s$$

4. To calculate T_{off}:

$$T_s = T_{on} + T_{off} \tag{13}$$

$$T_{off} = T_s - T_{on}$$

$$= 1\mu s - 0.25\mu s = 0.75\mu s$$

Table 3.3 *PWM* Setting

	PWM 1	***PWM 2***
V1	0V	0V
V2	5V	5V
TD	5n	255n
TR	5n	5n
TF	5n	5n
PW	240n	735n
PER	1000n	1000n

Table 3.3 shows PWM settings used throughout the project.

3.3.3 Value for Inductor, Capacitor and Resistor

The value for inductor, capacitor and resistor will be taken from [19]

3.4 PSPICE simulation

This project is mainly based on research and simulation work. The simulation will be done using PSPICE. The type of PSPICE used throughout the project is Microsim Design Manager, version 8.0.

3.5 Analysis Performance

Initially, the circuits that have been modeled from 1×1 to 4×4 for both DCM and CCM will be simulated using PSPICE software. From PSPICE, all data will be obtained. The data acquired from the simulation of each configuration are; node voltage (V_N), inductor current (I_L), output voltage (V_o) and output current (I_o). The entire data obtained will be tabulated in a table. Then, it will be analyzed to determine the optimized configuration. The criteria in deciding the best configuration is; produce high output current, minimal body diode conduction loss and maintaining 3 V as output voltage.

After obtaining the optimized configuration for both CCM and DCM, then it comes to the second stage of this work which is comparing my work with others that are;

- SRBC with CGD,
- SRBC with AGD,
- SRBC with AGD and compensator,
- SRBC with MPPT controller.

The parameter of the circuit is the same, only the method to get the best result is different. The rationale of comparing the result is to find out which technique can give the best result. The factors that will be evaluated are; output voltage ($V_{o(avg),}$), output current (I_{oavg}), output voltage ripple ($\Delta V_{op\text{-}p}$), output current ripple ($\Delta I_{op\text{-}p}$) and body diode conduction loss (P_{BD}). The formula for calculating the ripple is given in Eq. (14);

$$ripple = \frac{peak-avrg}{avrg} \times 100\% \qquad (14)$$

CHAPTER 4
RESULT AND DISCUSSION

4.1 Chapter Overview

This chapter will discuss on results obtained from the simulations of conventional SRBC circuits. The result will be divided into two sections which are Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). Several configurations of MOSFET parallelism at switch, *S1* and switch, *S2* from 1×1 up to 4×4 have been analyzed to determine the best option that can produce the highest output current as well as low body diode conduction and other losses. In order to get the best conventional SRBC circuit performance, PWM setting must be correct so that the signal can be correctly supplied to the switches. Other than that, few points at the circuit have been taken i.e. node voltage (V_L), inductor current (I_L), output voltage (V_o) and output current (I_o). After that, the best option for conventional SRBC circuit's result will be compared to SRBC using controller.

4.2 Data Gathering and Analysis

4.2.1 Pulse Width Modulator

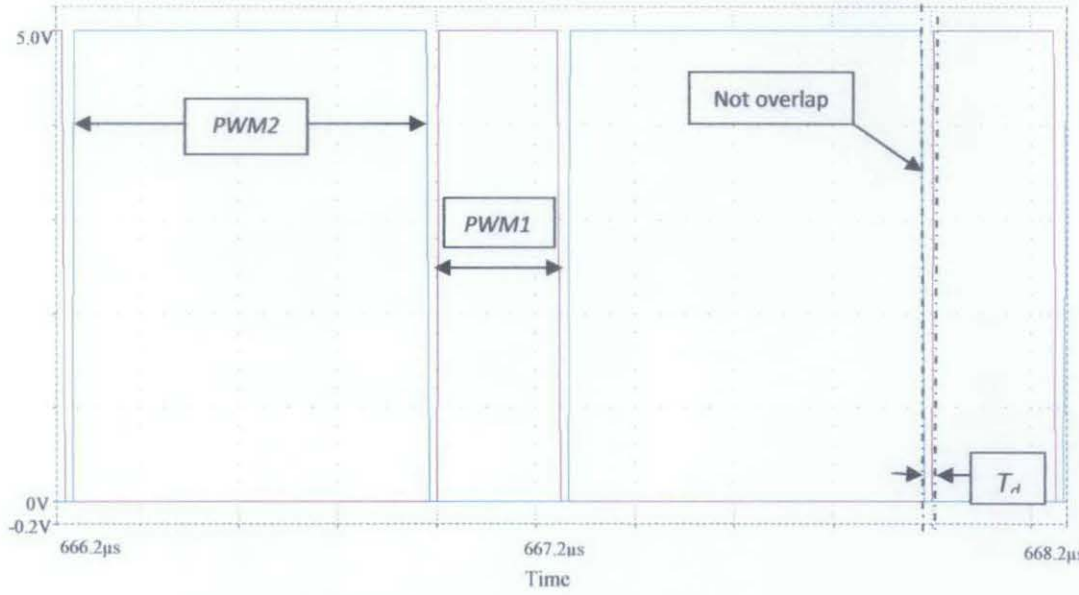

Figure 16 Waveform of the Voltage Differential at PWM

In this project, there are two PWM used. Referring to Figure 16 there are *PWM1* and *PWM2*. For *PWM1*, it is the pulse width for MOSFET *S1*. Whereas for *PWM2* represents pulse width of MOSFET *S2*. It is a square-wave pulse signals.

S1 and *S2* MOSFETs will conduct complementarily i.e. will not conduct at the same time. As shown in the Figure 16, there is no overlapping between *PWM1* and *PWM2*. This is very important in order to have correct switching time. With that, *S1* and *S2* MOSFETs will not turn on at the same time.

T_d is dead time of when the both *S1* and *S2* are not conducting. The dead time for this circuit is 15 ns. It is preferred to keep the dead time as short as possible as this may reduce body diode conduction loss. Other than that, when making T_d too long, this may result in increasing overshoot voltage at the gate terminal S_1 which can damage the switch.

4.2.2 Voltage at PWM1

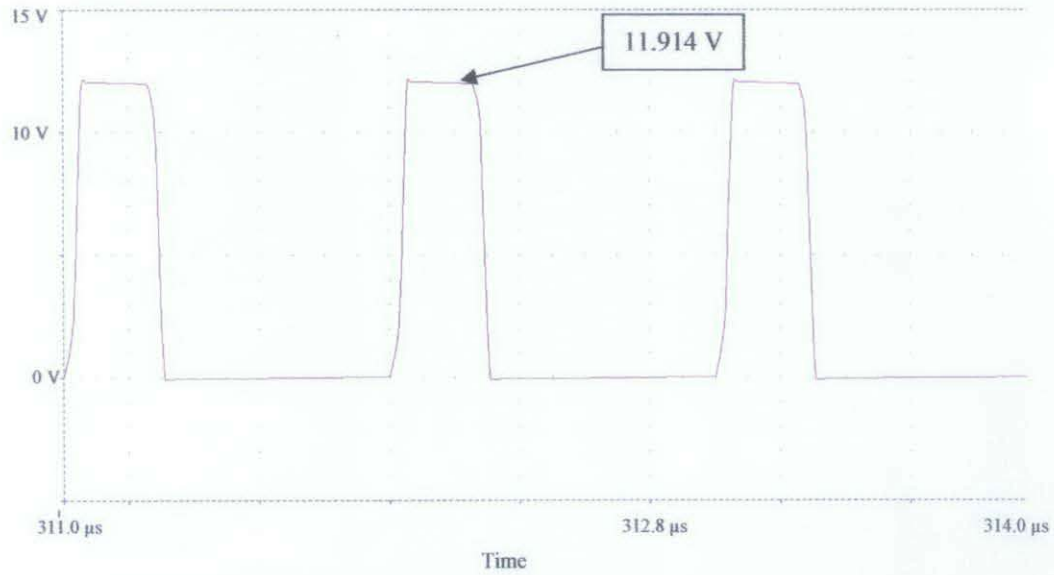

Figure 17 Node Voltage

Figure 17 shows node voltage taken between *PWM1* and *PWM2* point. This is important to check whether the switching of MOSFETs *S1* and *S2* are correct or not. According to theory, node voltage must be the same as voltage input which is for this case the input voltage is 12 V. From the graph in Figure 17, the peak voltage for node voltage is 11.914 V. The difference between theoretical and practical value is 0.716 % $=\left(\left(\frac{12-11.914}{12}\right) \times 100\ \%\right)$. As long as the difference is only ±5 % it is acceptable. Hence, the setting for PWM is correct.

4.3 Continuous Conduction Mode (CCM) Conventional SRBC Circuit

Continuous Conduction Mode (CCM) is when the current in the energy transfer inductor never goes to zero between switching cycles. That means the inductor current; I_L will always be above 0 A. The CCM optimum parameter value taken from [19] is as in Table 4.1 below;

Table 4.1 Component Value for CCM Mode

Component	**Value**
Inductor, *L*	15 μH
Capacitor, *C*	0.625 μF
Resistor, *R*	3.5 Ω

Using the CCM parameter value, the MOSFETs at both *S1* and *S2* switches have been paralleled. For CCM the inductor current will always be above 0 A. Overall, there are 16 configurations consisting of 1×1 up to 4×4 switches. Below are the results of all the configuration of parallelism for CCM Conventional SRBC circuit.

Table 4.2 CCM SRBC Circuit with MOSFETs Parallelism

Case	Node Voltage, V_N			Inductor Current, I_L			Output	Output
S1,S2	Δt (ns)	Negative Peak (mV)	Body diode Conduction Loss, P_{bd} (mW)	Negative Peak (mA)	Positive Peak (mA)	Current, $I_{L,avg}$ (mA)	Voltage, V_o (V)	Current, I_o (mA)
1,1	53	-606.525	16.870	706.167	844.824	775.287	2.6959	770.260
1,2	54	-567.683	24.250	721.908	860.762	791.245	2.6954	791.097
1,3	55	-549.083	23.880	729.943	866.174	794.263	2.6954	790.675
1,4	55	-535.383	23.250	725.827	863.605	793.058	2.6955	789.732
2,1	49	-612.941	24.677	752.679	897.967	825.234	2.6945	821.652
2,2	50	-573.637	23.928	763.531	908.661	831.915	2.6943	834.623
2,3	49	-553.659	22.576	765.412	909.775	834.765	2.6944	832.167
2,4	60	-540.892	27.065	765.926	909.962	837.000	2.6943	833.955
3,1	50	-621.820	26.387	778.224	926.767	852.677	2.6936	848.696
3,2	30	-576.119	14.739	784.551	932.432	855.589	2.6932	852.801
3,3	30	-555.733	14.232	783.947	931.151	855.429	2.6929	853.662
3,4	50	-542.813	23.089	784.271	930.668	855.671	2.6930	850.716
4,1	20	-620.474	10.720	793.868	944.155	865.984	2.6919	863.835
4,2	49	-581.881	24.700	796.231	945.411	868.952	2.6914	865.975
4,3	48	-561.913	23.281	797.248	945.970	868.211	2.6916	863.175
4,4	30	-545.211	14.111	794.391	942.298	866.219	2.6917	862.737

Table 4.2 is the summary of simulation result of CCM SRBC circuit with MOSFETs parallelism. There are four main criteria to choose the best configuration for CCM. They are node voltage (V_N), inductor current (I_L), output voltage (V_o) and output current (I_o). It can be noted that the body diode conduction time, Δt is fluctuating. The value is taken from node voltage, V_N. The inductor current I_L is continuously increasing as the parallelism method applied to the switch. Comparing to inductor current, output current has slightly smaller value. This is because some current is fed into capacitor. However, further discussion on each point can be seen in section 4.3.1.

4.3.1 Output Current CCM

It is crucial to observe the output current. This is because to make sure to achieve the aim of the project which is to obtain highest output current possible. However, other points also require consideration in search for the optimized configuration.

Referring to the Table 4.2, output current, I_o increases as the configuration of 1×1 to 4×4 that is from 769.684 mA to 862.737 mA (862.737 mA - 769.684 mA = 93.053 mA). The pattern of output current, I_o can be seen in Figure 18 below;

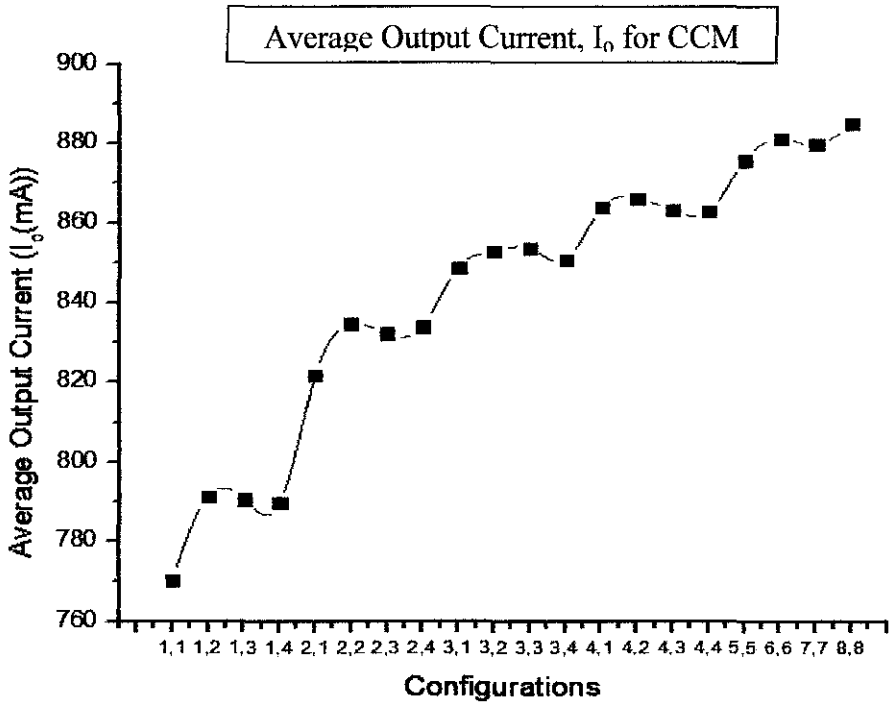

Figure 18 Graph of Output Current, I_o for CCM

Figure 18 shows graph of output current, I_o for all configurations for CCM. A few extra configurations are added to prove the pattern of output current which are (*S1*:5; *S2*:5), (*S1*:6; *S2*:6), (*S1*:7; *S2*:7) and (*S1*:8; *S2*:8). It is proven that by paralleling the switches, the output current keeps on increasing.

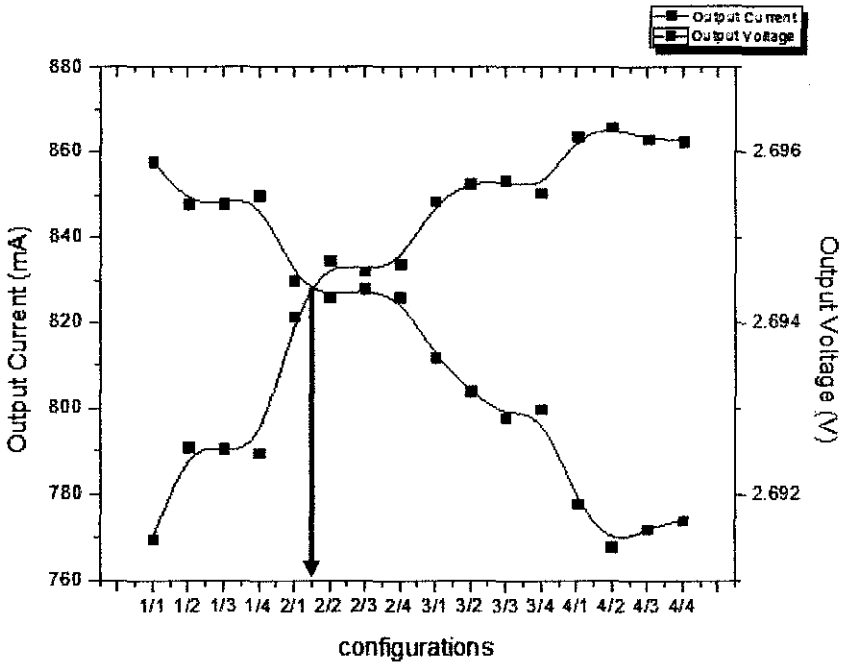

Figure 19 Graph of Output Voltage, V_o and Output Current, I_o for CCM

Figure 19 shows graph of Output Voltage, V_o and Output Current, I_o for CCM. From this figure, the cross between output voltage and output current is at configuration of (*S1*:2; *S2*:1) but we cannot easily assume that this is the optimized configuration because other factors need to take into consideration too which are body diode conduction loss (P_{bd}), and inductor current, (I_L).

4.3.2 Body diode conduction loss for CCM

Even though the aim of this project is to get highest output current, other criteria need to be considered to get the optimum result out of 16 configurations. Body diode conduction loss is another crucial point. In the Table 4.2, body diode conduction (Δt) can be seen at node voltage column. The value is fluctuating as in Figure 20;

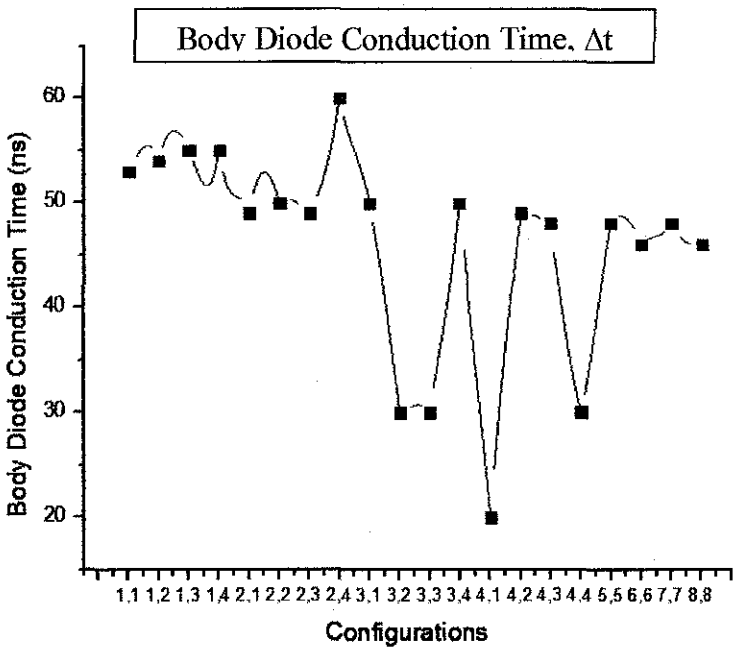

Figure 20 Graph of Body Diode Conduction for CCM

Body diode conduction time can be observed at node voltage. It is preferred to have the smallest body diode conduction because the losses are proportional to body diode conduction time. A smaller body diode conduction time will have smaller conduction loss. Referring to Figure 20, there are few configurations that have lowest body diode conduction which is shown in Table 4.3 below;

Table 4.3 Configurations with Lowest Body Diode Conduction

S1	*S2*
3	3
4	1
4	4

4.3.3 Choosing optimized configuration for CCM

Table 4.3 shows configurations of MOSFETs parallelism that has lowest body diode conduction time among 16 configurations. All four configurations are increasing in output current. These configurations will be compared and discussed to determine the optimized setting.

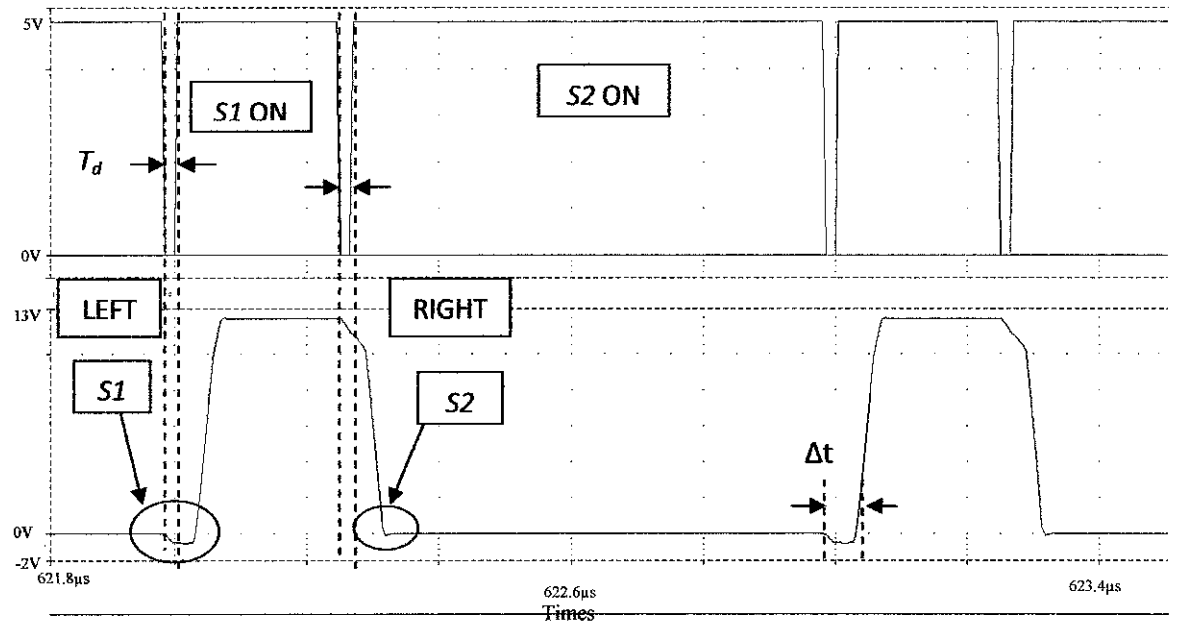

Figure 21 Node Voltage, V_N for CCM

Figure 21 shows that body diode conduction time that was obtained from node voltage, V_N and above node voltage waveform is from the switching of *S1* and *S2*. In Figure 21, the left-hand side shows the body diode conduction loss for *S1*. This is because it is only happens when *S1* is turned on. Whilst the right-hand side is body diode conduction is for *S2* as *S2* turns on. *S2* body diode is turned on with ZVS by circulating current that flows into L_o as soon as *S1* turned off. For *S2*, it is assumed that there is no body diode conduction loss since it is conducting below 0.3 V. It is the same for all configurations in CCM. The only thing that differ in the configurations is that the value of body diode conduction loss.

From the results obtained, the configuration which has the smallest body diode conduction loss can be seen in the waveform below.

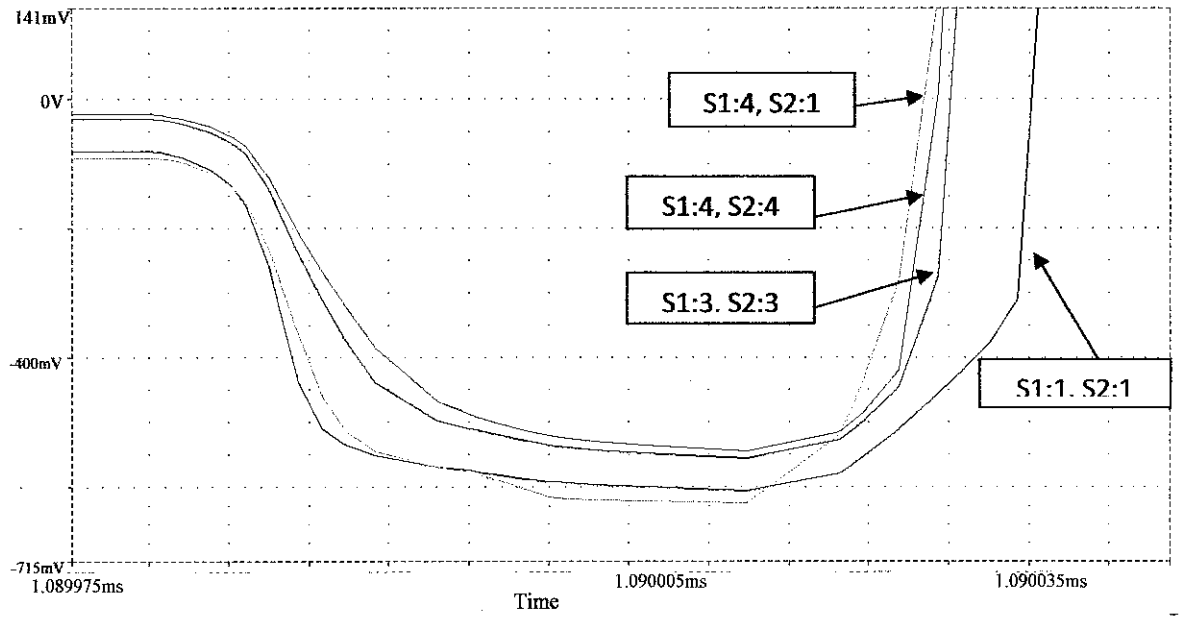

Figure 22 Body diode conduction time for chosen configurations for CCM

Figure 22 shows the enlarged waveform of node voltage, V_N of body diode conduction time, Δt. There are three configurations that have smallest body diode conduction time that is first, 20 ns for configuration of (*S1*:4, *S2*:1). 30 ns for both configurations of (*S1*:3, *S2*:3) and (*S1*:4, *S2*:4). In the Figure 22, those three configurations are compared to the original configuration, (*S1*:1, *S2*:1). It is found that body diode conduction exists when it is conducting with more than -0.3 V. Hence, it is an advantage to choose body diode conduction with the lowest value of negative peak that is closest to -0.3 V. Referring to Figure 22, a pattern of body diode conduction is shown. If the body diode conduction time is smaller, it will result in increasing negative peak value. This can be seen in configuration of (*S1*:4, *S2*:1) having the negative peak of -620.474 mV (refer to Table 4.2).

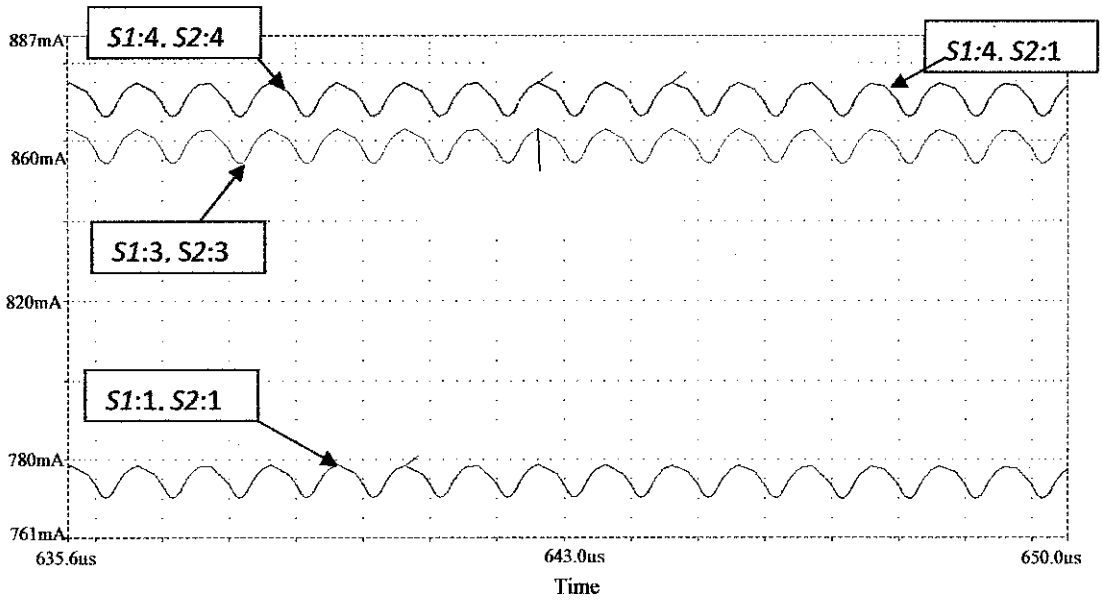

Figure 23 Output Current Comparisons for CCM

Figure 23 shows the output current for the several configurations having the lowest body diode conduction time. It is clear that the value of output current increases. It is clear that paralleling MOSFETs can increase the output current compared to the original configuration (*S1*:1, *S2*:1). The output current for configuration in (*S1*:3, *S2*:3) is 853.662 mA. However, in configurations of (*S1*:4, *S2*:1) and (*S1*:4, *S2*:4), there is not much different in output currents having 863.83 5mA and 862.737 mA respectively.

4.3.4 Optimized configuration for CCM

In choosing the best configuration of MOSFET parallelism, all factors need to be put into considerations which are;

- high output current,
- low body diode conduction loss,
- output voltage ≈ 3V

As for CCM, output current and inductor current values will increase as numbers of parallel switches are added. The only difference is body diode

conduction loss. So, in order to choose the best configuration for CCM conventional SRBC, it is not only to look at the highest output current but also to consider the body diode conduction loss as it minimizes the loss.

In order to get the best result, configuration (*S1*:4, *S2*:1) is chosen to be the optimized configuration. This is because it has highest output current, lowest body diode conduction loss, and also third highest of inductor current. Below are the waveforms comparing the optimized configuration with (*S1*:1, *S2*:1);

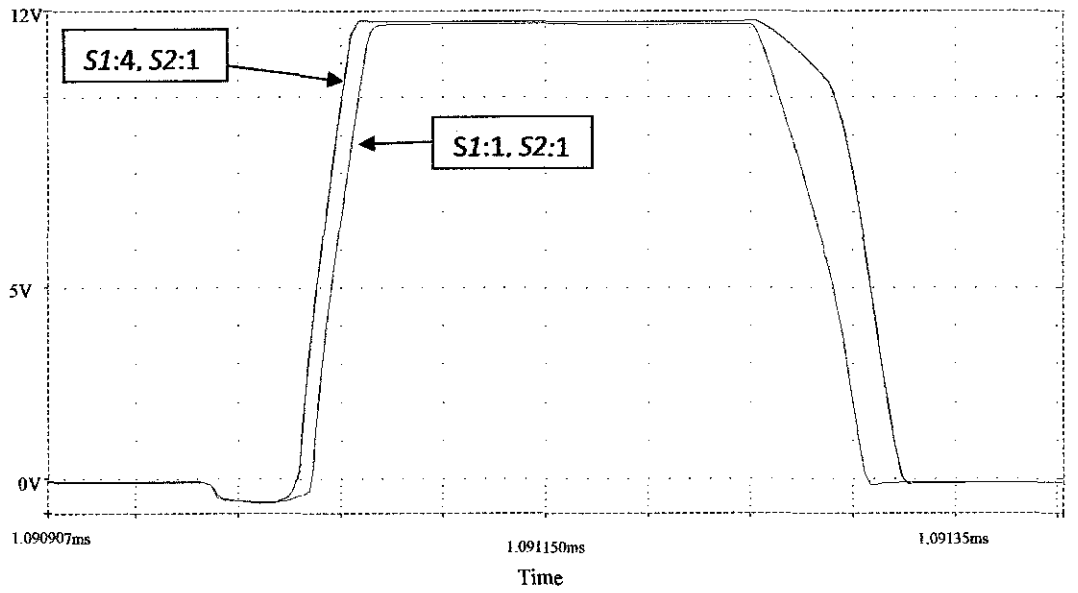

Figure 24 Node Voltage for optimized configuration for CCM

Referring to Figure 24 and Table 4.2, this configuration (*S1*:4, *S2*:1) has the shortest body diode conduction time which is 20 ns only. However, the drawback of having short body diode conduction time is that, it is resulting in increasing negative node voltage peak value which is -620.474 mV. In spite of this, body diode conduction loss decreases by 36.45 % $\left(\frac{16.87mW-10.72mW}{16.87mW} \times 100\ \%\right)$ from 16.87 mW to 10.72 mW.

Referring to Figure 23, output current increases by 8.27 % $\left(\left|\frac{770.26mA-833.955mA}{770.26mA} \times 100\ \%\right|\right)$ compared to the configuration of (*S1*:1, *S2*:1). As long the output current increases, it is acceptable since the aim of this project is to increase the output current of original configuration.

However, the drawback of this configuration is the output voltage. According to Ohm's Law, V=IR, when resistor is fixed, if the current value increases, thus the voltage value will drop. Same goes to this case, when the output current increases, and hence it results in lower voltage. The output voltage decreases from 2.6959 V to 2.6919 V. That would be 0.148 % $\left(\frac{2.6959-2.6919}{2.6959} \times 100\ \%\right)$ in voltage drop.

4.4 **Discontinuous Conduction Mode (DCM) Conventional SRBC Circuit**

Discontinuous Conduction Mode (DCM) is when the current goes to zero during part of the switching cycle. For DCM conventional SRBC circuit, parameter for DCM are used. The DCM optimum parameter values are taken from [19] as shown in Table 4.4 below;

Table 4.4 Component Value for DCM Mode

Component	**Value**
Inductor, *L*	1 μH
Capacitor, *C*	9.375 μF
Resistor, *R*	4 Ω

For DCM the inductor current will be slightly below negative. Again using the same configuration as CCM conventional SRBC circuit, the switches will be parallel up to 16 configurations which is from 1×1 to 4×4. Below are the results of PSPICE simulation:

Table 4.5 DCM SRBC Circuit with MOSFETs Parallelism

Case	Node Voltage, V_N			Inductor Current, I_L			Output Voltage, V_o (V)	Output Current, I_o (mA)
S1,S2	Δt (ns)	Negative Peak (mV)	Body diode Conduction Loss, P_{bd} (mW)	Negative Peak (mA)	Positive Peak (mA)	Current, $I_{L,avg}$ (mA)		
1,1	3.148	-617.568	6.29	-335.993	1.7193	707.294	2.7405	674.382
1,2	-	-	-	-334.012	1.7115	765.446	2.7402	685.793
1,3	-	-	-	-335.765	1.7264	775.502	2.7400	695.418
1,4	-	-	-	-332.028	1.7266	779.564	2.7397	698.681
2,1	-	-	-	-342.276	1.7726	788.309	2.7395	705.668
2,2	-	-	-	-342.110	1.7820	805.839	2.7390	721.264
2,3	-	-	-	-336.342	1.7916	812.049	2.7388	726.872
2,4	-	-	-	-338.433	1.7965	815.141	2.7385	729.978
3,1	-	-	-	-348.524	1.8182	816.081	2.7387	728.091
3,2	-	-	-	-338.478	1.8310	796.589	2.7382	740.202
3,3	-	-	-	-334.968	1.8326	792.591	2.7375	746.027
3,4	-	-	-	-343.216	1.8349	798.901	2.7373	747.479
4,1	-	-	-	-352.9115	1.8514	766.489	2.7372	748.604
4,2	-	-	-	-342.651	1.8598	805.910	2.7369	755.595
4,3	-	-	-	-347.338	1.8506	827.023	2.7362	758.520
4,4	-	-	-	-345.955	1.8555	787.474	2.7365	757.760

Table 4.5 is the summary of the result of DCM for all 16 circuits' configurations from 1×1 up to 4×4. There are four main criteria in the table: Node voltage (V_N), inductor current (I_L), output voltage (V_o) and output current (I_o). The body diode conduction can be seen at the node voltage. Inductor current is an important point to check because it is to ensure that the circuit is working in DCM mode. By checking the positive peak of the inductor current, current ripple can be calculated too. As for output voltage and output current, it is crucial to observe the value.

Referring to Table 4.5, there is no body diode conduction except for (*S1*:1, *S2*:1) configuration. Hence, paralleling the MOSFETs has helped reduce the body diode conduction to zero. With no current flowing during the turn off time, this can increase the output current. This is shown in the graph below.

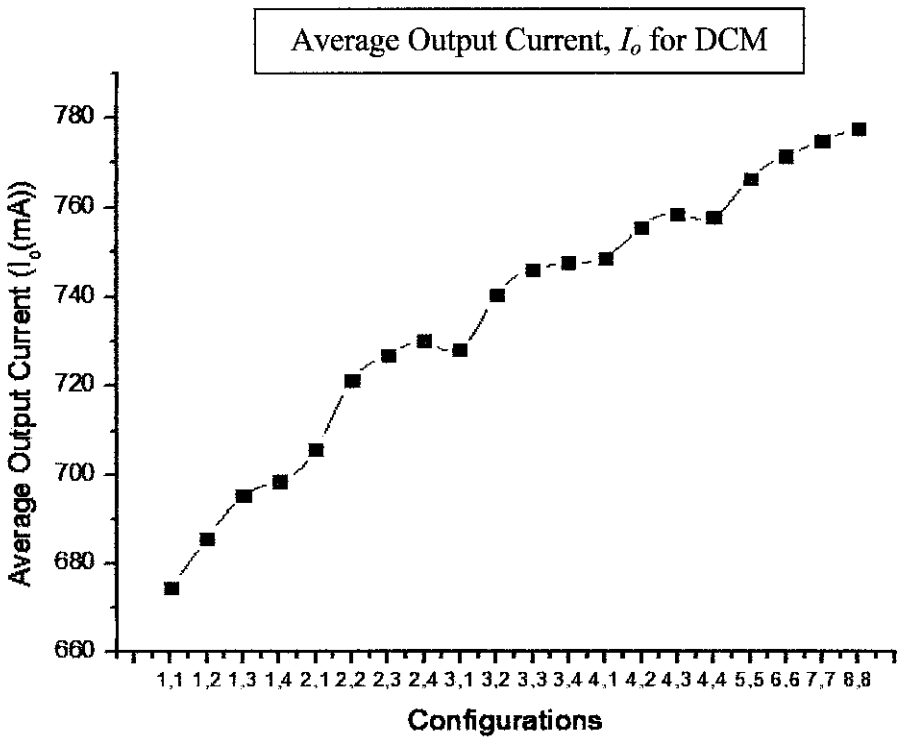

Figure 25 Graph of Output Current, I_o for DCM

In Figure 25, the output current keeps on increasing from the first configuration until the last configuration. Overall, the output current increases by 12.36 % from 674.382 mA to 757.76 mA$\left(\left|\frac{674.382mA-757.76mA}{674.382mA} \times 100\,\%\right|\right)$. However, to choose the optimized configuration for DCM, apart from producing high output current, other parameters also need to be taken into consideration.

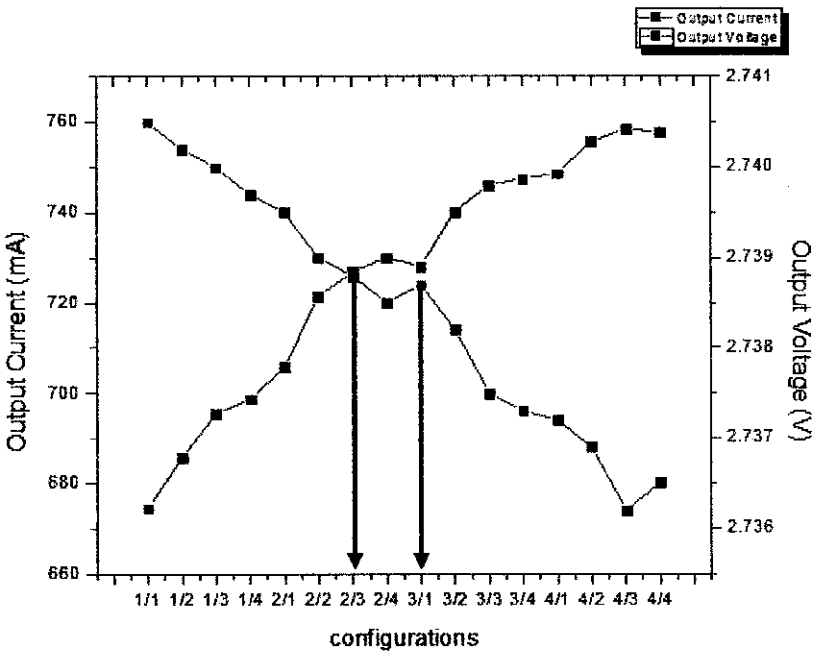

Figure 26 Graph of Output Voltage, V_o and Output Current, I_o for DCM

Figure 26 shows graph of output voltage, V_o and output current, I_o for DCM. The intersection point in the waveform are at ($S1$:2; $S2$:3) and ($S1$:3; $S2$:1). However, we cannot easily assumed that these two configurations are optimized. This is because we also have to take other factors into considerations which are body diode conduction loss (P_{bd}), inductor current, (I_L) and also output voltage (V_o).

The drawback for paralleling the MOSFETs is it generates a low output voltage. In this case, the output voltage should be 3 V. The output voltage is acceptable if the difference is ±10 %. So the acceptable range is 2.7 V (-10 %×3) to 3.3 V (+10 %×3). Therefore, it can be seen in Table 4.5 that the output voltage

is decreasing as the output current increases. The output voltage decreases from 2.7405 V to 2.7365 V.

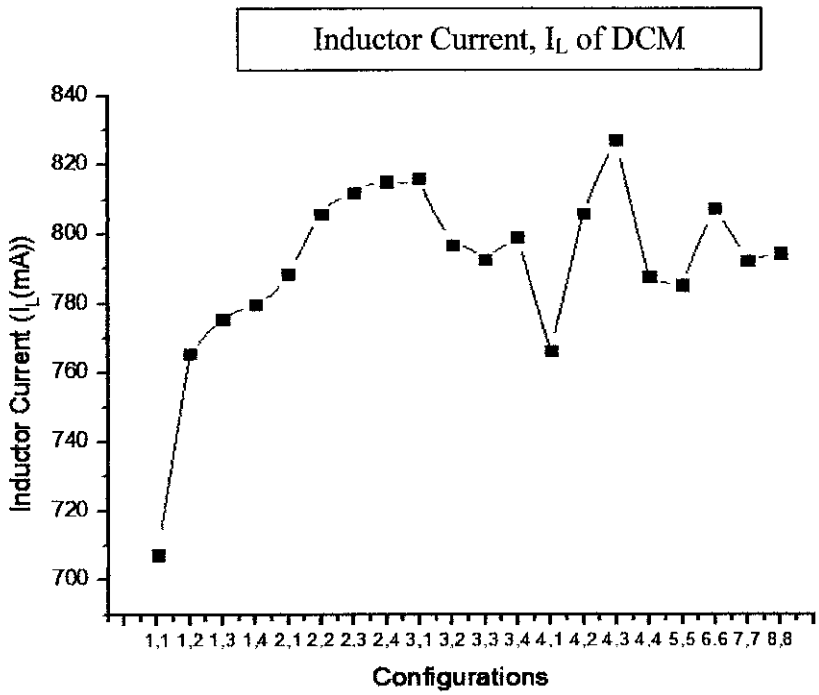

Figure 27 Graph of Inductor Current for DCM.

Figure 27 shows inductor current for DCM. From the graph it shows that the value is fluctuating. The lowest inductor current value for (*S1*:1, *S2*:1) configuration that is 707.294 mA. While the highest value is 827.023 mA at (*S1*:4, *S2*:3). Overall the inductor current increases by 16.93 %$\left(\left|\frac{707.294mA-827.023mA}{707.294mA}\times 100\ \%\right|\right)$. It is important to keep the inductor current high as this current that will be fed into the resistor which is the output current. However, if the peak current value is high, it will contribute to high ripple current.

After analyzing all the parameters, it is proven that (*S1*:4, *S2*:3) configuration is the optimized configuration. First of all, this configuration produces high output current compared to conventional (*S1*:1, *S2*:1) configuration.

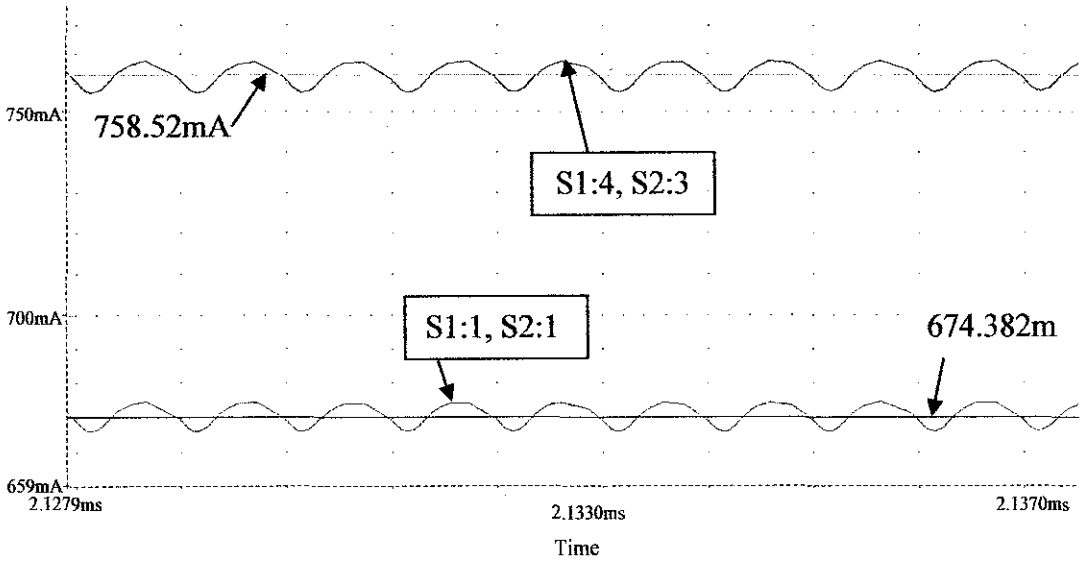

Figure 28 Output Current Comparisons for DCM

Figure 28 shows the comparison between configurations of (*S1*:4, *S2*:3) and (*S1*:1, *S2*:1). The average output voltage increases by 12.48 % $\left(\left|\frac{758.52mA-674.382mA}{758.52mA} \times 100\ \%\right|\right)$. Thus the aim of increasing higher output current is successful by paralleling the MOSFETs.

The average output voltage for configuration (*S1*:4, *S2*:3) is 2.7362 V. Even though the voltage is not close to 3 V, it is still acceptable because the difference is 8.79 % $\left(\frac{3V-2.7362V}{3V} \times 100\ \%\right)$ which is not more than ±10 %.

Another drawback for DCM optimized configuration (*S1*:4, *S2*:3) is the inductor current value. The waveform of inductor current can be seen in Figure 29.

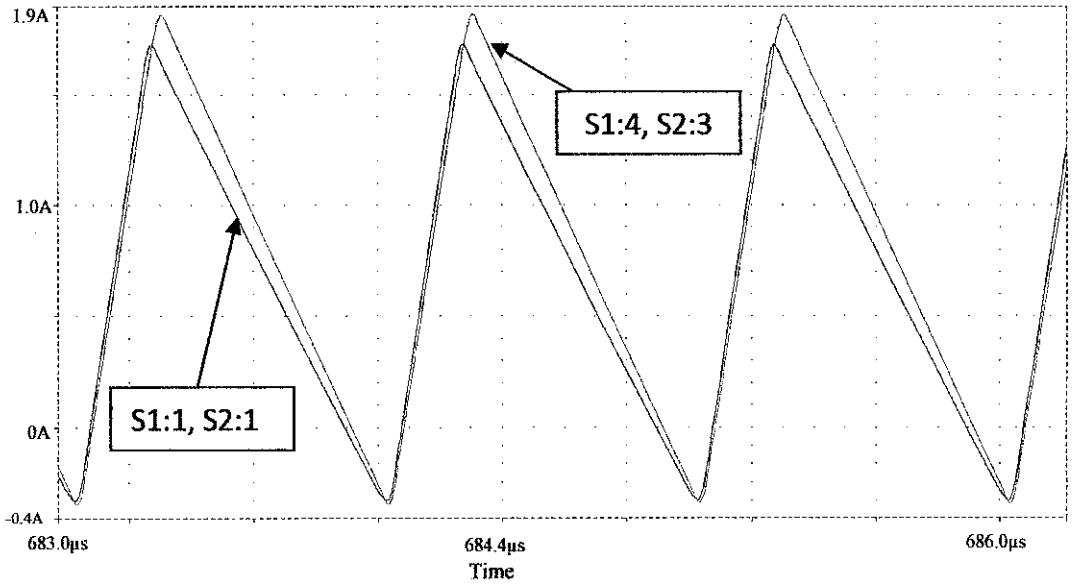

Figure 29 Inductor Current Comparisons for DCM

Figure 29 shows comparison between configurations (*S1*:4, *S2*:3) and (*S1*:1, *S2*:1) for inductor current. Supposedly, the value for inductor current should be low in order to keep the current ripple value lower. However, in order to get high output current, the current at inductor should also be high because this current will be fed into two different junctions which are capacitor and resistor (output current). Hence, the inductor current increases by 16.93 % $\left(\left|\frac{707.294mA-827.023mA}{707.294mA} \times 100\right|\right)$.

4.5 **Comparison with Other Circuits for CCM**

The results are then compared with other SRBC circuits having the same parameter values but with different type of controllers. The results are shown in Table 4.6 and Table 4.7 respectively;

According to table 4.6, there are 4 types of SRBC circuit used to compare in this project. They are, conventional SRBC circuit; an original circuit that only uses optimum parameter values for resistor, inductor and capacitor to get the best result. Secondly, the SRBC circuit with AGD controller. Thirdly, SRBC circuit with compensator and AGD. Lastly, it is SRBC circuit with MPPT controller. In order to compare those SRBC circuits, there are few parameters evaluated: output voltage ($V_{o(avg),}$), output current (I_{oavg}), output voltage ripple ($\Delta V_{op\text{-}p}$), output current ripple ($\Delta I_{op\text{-}p}$) and the lastly, body diode conduction loss (P_{BD}).

Table 4.6 Comparison SRBC circuit with controller for CCM

	CCM				
	CGD [19]	**AGD [20]**	**Compensator and AGD [20]**	**Parallelism- M_1:4, M_2:1**	**MPPT- V_{pulse} [21]**
$V_{o(avg)}$, **(V)**	2.70	2.68	2.99	2.69	3.09
I_{oavg}, **(mA)**	770.26	765.76	853.77	863.84	882.27
$\Delta V_{o\ p\text{-}p}$ **(%)**	1.66	2.23	2.10	1.86	0.95
$\Delta I_{o\ p\text{-}p}$ **(%)**	1.62	2.21	2.08	2.36	0.95
P_{BD} **(mW)**	16.87	20.79	None	10.70	None

Table 4.7 Improvement of CGD, AGD, Compensator-AGD, Parallelism and MPPT for CCM

	CCM			
	Improvement of Parallelism to CGD (%)	**Improvement of Parallelism to AGD (%)**	**Improvement of Parallelism to Compensator-AGD (%)**	**Improvement of Parallelism to MPPT- V_{pulse} (%)**
$V_{o(avg)}$, (V)	-0.37	+0.38	-11.15	-14.87
I_{oavg}, (mA)	+10.83	+11.33	+1.165	-2.13
$\Delta V_{o\ p\text{-}p}$ (%)	-10.75	+19.89	-12.90	-48.92
$\Delta I_{o\ p\text{-}p}$ (%)	-31.35	-6.35	-11.86	-59.74
P_{BD} (mW)	+61.68	+94.29	-100	-100

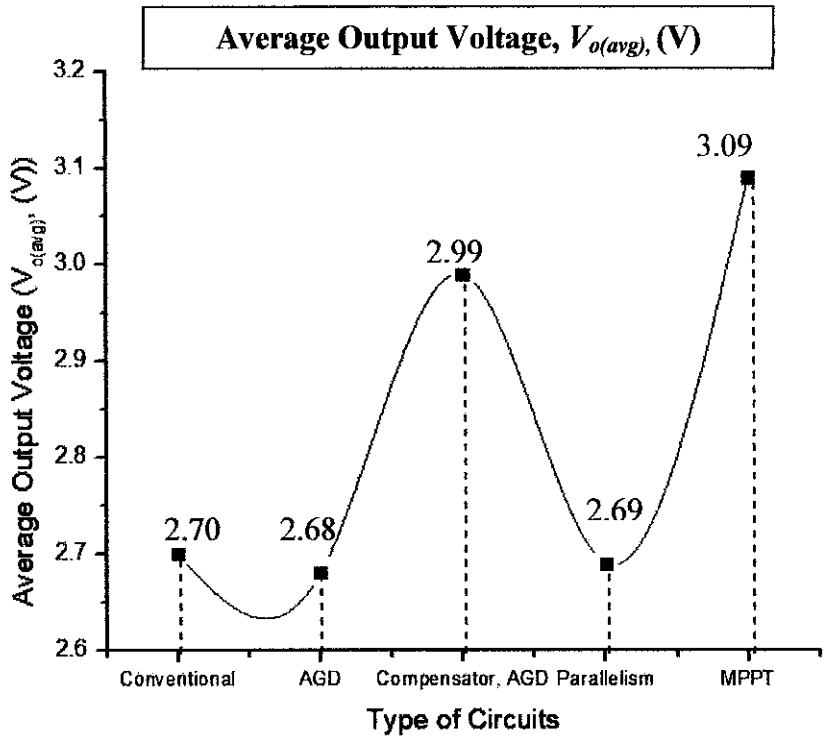

Figure 30 Average Output Voltage Comparison

Figure 30 shows the comparison among the circuits on average output voltage. The output voltage is preferred to be close to 3 V. This is because the circuit is buck converter that converts 12 V to be 3 V. By comparing with MOSFETs parallelism, MPPT controller increases the output voltage by 14.87 % $\left(\left|\frac{2.69-3.09}{2.69}\right| \times 100\ \%\right)$. SRBC circuit with compensator and AGD also increases by 11.15 % $\left(\left|\frac{2.69-2.99}{2.69}\right| \times 100\ \%\right)$. Whilst for conventional SRBC and AGD, the value for output voltage is not much different compared to my optimized configuration work. They are 2.7 V and 2.68 V, respectively.

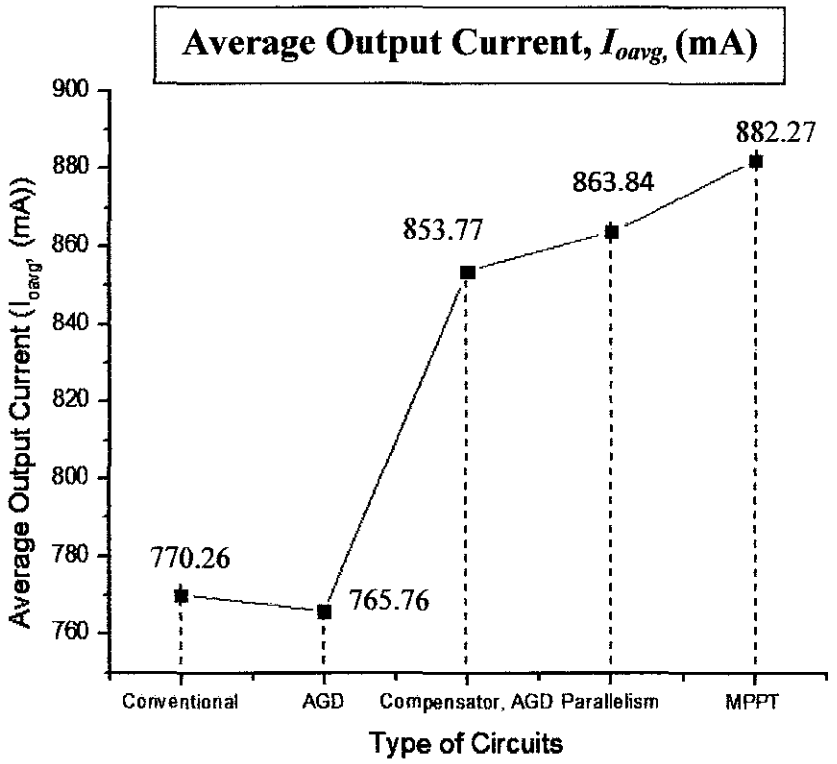

Figure 31 Output Current Comparison

Referring to Figure 31, it is clearly seen that MOSFETs parallelism is producing quite high output current compared to other technique. For AGD technique, MOSFETs parallelism increases output current by 11.33 % $\left(\left|\frac{863.84-765.76}{863.84}\right| \times 100\ \%\right)$. It is obvious that the technique of compensator and AGD is better than AGD alone. But still, MOSFETs parallelism gives slightly better output current that is an increase of 1.165 % $\left(\left|\frac{863.84-853.77}{863.84}\right| \times 100\ \%\right)$. On the other hand, MPPT controller technique is better than MOSFETs parallelism by 2.13 % $\left(\left|\frac{863.835-882.266}{863.835}\right| \times 100\ \%\right)$.

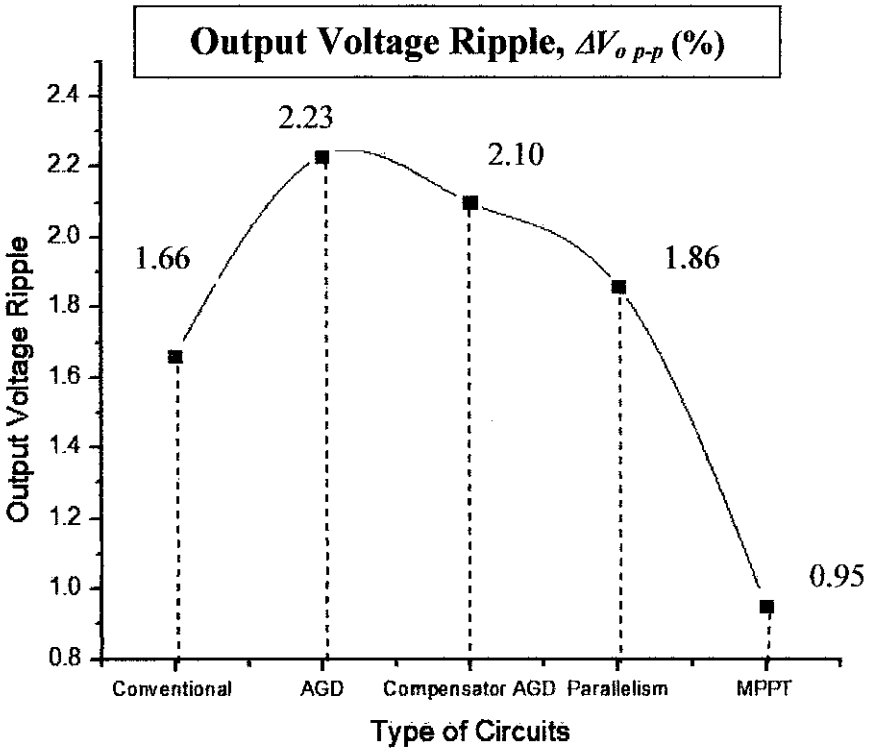

Figure 32 Output Voltage Ripple Comparison

Figure 32 shows the comparison of output voltage ripple. It is important to keep the output voltage ripple as small as possible. From Figure 32, MPPT controller gives the smallest output voltage ripple that is 0.9124 % (1.86 % - 0.9476 %) compared to MOSFETs parallelism.

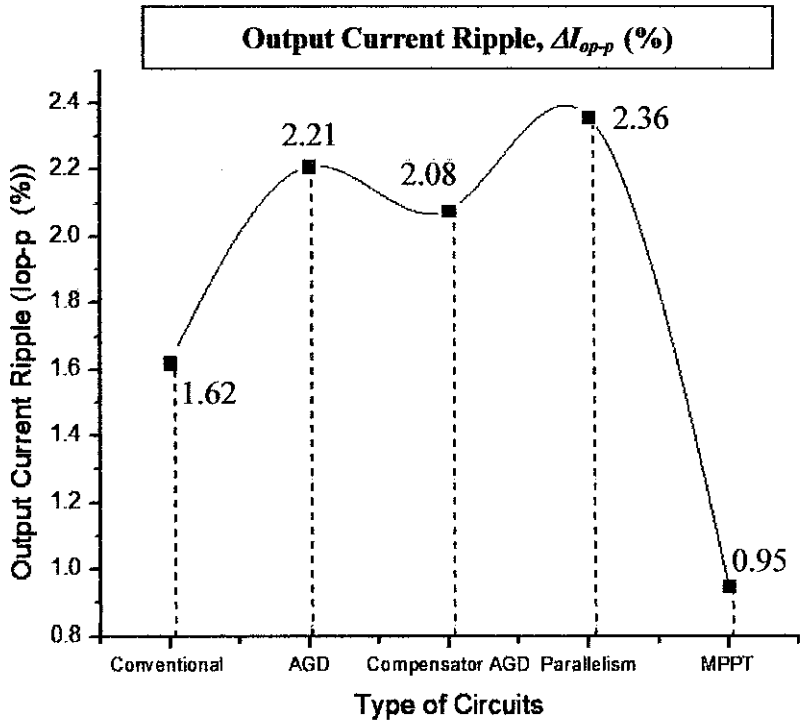

Figure 33 Output Current Ripple Comparison

The comparison of output current ripple is shown in Figure 33. Obviously, MOSFETs parallelism is not able to produce small ripple value. Compared to MPPT controller, it is better than MOSFETs parallelism by 1.4126 % (2.36 % - 0.9474 %). Conventional SRBC circuit also gives smaller output current ripple with only 1.20 % (2.36 % - 1.16 %).

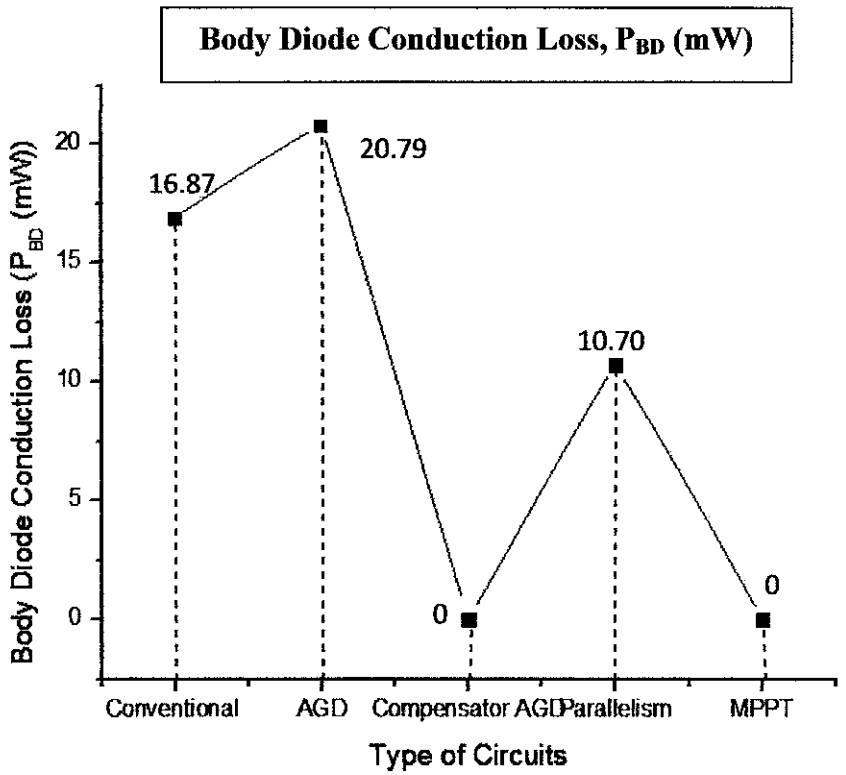

Figure 34 Body Diode Conduction Loss Comparison

Figure 34 shows the comparison of body diode conduction loss between all the techniques applied. Compared to MOSFETs parallelism techniques, AGD and MPPT controller are better because they have reduced body diode conduction loss to zero.

4.6 **Comparison with Other Circuits for DCM**

According to table 4.8, there 4 types of SRBC circuits used to compare in this project. There are, conventional SRBC circuit; an original circuit that only used optimum parameter value for resistor, inductor and capacitor to get the best result. Secondly, would be SRBC circuit with AGD controller. The next circuit is SRBC circuit with compensator and AGD. Lastly, it is SRBC circuit with MPPT controller. In order to compare those SRBC circuits, there are few parameters that have been taken which is output voltage ($V_{o(avg),}$), output current (I_{oavg}), output voltage ripple ($\Delta V_{op\text{-}p}$), output current ripple ($\Delta I_{op\text{-}p}$) and the last one is body diode conduction loss (P_{BD}).

Table 4.8 Comparison SRBC circuit with controller for DCM

	DCM				
	CGD [19]	**AGD [20]**	**Compensator and AGD [20]**	**Parallelism- M_1:4, M_2: 3**	**MPPT- V_{pulse} [21]**
$V_{o(avg)}$, **(V)**	2.70	2.68	2.99	2.74	3.11
I_{oavg}, **(mA)**	676.13	670.60	748.86	758.52	777.81
$V_{o\ p\text{-}p}$ **(%)**	1.02	1.65	3.48	1.34	1.35
$I_{o\ p\text{-}p}$ **(%)**	1.06	1.62	3.41	1.00	1.35
P_{BD} **(mW)**	6.29	4.63	None	None	None

Table 4.9 Improvement of CGD, AGD, Compensator-AGD, Parallelism and MPPT for CCM

	CCM			
	Improvement of Parallelism to CGD (%)	**Improvement of Parallelism to AGD (%)**	**Improvement of Parallelism to Compensator-AGD (%)**	**Improvement of Parallelism to MPPT- V_{pulse} (%)**
$V_{o(avg)}$, (V)	+1.46	+2.19	-9.12	-13.50
I_{oavg}, (mA)	+10.86	+11.59	+1.27	-2.54
$\Delta V_{o\ p\text{-}p}$ (%)	-23.88	+23.13	+159.70	+0.75
$\Delta I_{o\ p\text{-}p}$ (%)	+6.00	+62.00	+241.00	+35.00
P_{BD} (mW)	+100	+100	-	-

Table 4.9 shows the improvement of other circuits (conventional SRBC, AGD, Compensator-AGD and MPPT controller) compared to my work (MOSFETs parallelism). For DCM mode, after paralleling the MOSFETs with (*S1*:4, *S2*:3) configuration, body diode conduction loss has been reduced to zero compared to CGD, which is 6.29 mW. SRBC circuit with compensator-AGD and MPPT also successfully eliminates body diode conduction loss to zero as well.

For average output voltage, MOSFETs parallelism produces better output voltage by 1.46 % ($\frac{2.74-2.7}{2.74} \times 100\ \%$) compared to the conventional SRBC circuit (CGD). However, when SRBC circuit is applied with controller that is compensator-AGD and MPPT, they give better average output voltage. Both of the controller increases by 9.12 % ($\frac{2.74-2.99}{2.74} \times 100\ \%$) and 13.50 % ($\frac{2.74-3.11}{2.74} \times 100\ \%$) respectively compared to MOSFETs parallelism.

In term of average output current, MOSFETs parallelism produces higher average output current better than CGD, AGD and compensator-AGD. It is improved by 10.86% ($\frac{758.52-676.13}{758.52} \times 100\ \%$), 11.59 % ($\frac{758.52-670.60}{758.52} \times 100\ \%$) and 1.27 % ($\frac{758.52-748.86}{758.52} \times 100\ \%$) respectively. Nevertheless, MPPT controller gives 2.54 % ($\frac{758.52-777.81}{758.52} \times 100\ \%$) higher output current compared to MOSFETs parallelism.

As for output voltage ripple, MOSFETs parallelism is not able to provide the best result. CGD gives the smallest value for voltage ripple, 1.02 %. Here MOSFETs parallelism is 23.88 % ($\frac{1.34-1.02}{1.34} \times 100\ \%$) higher than CGD. Comparing with compensator-AGD, MOSFETs parallelism gives lower output current ripple. For output current ripple, MOSFETs parallelism produces the smallest value compared to CGD (1.06 %), AGD (1.62 %), compensator-AGD (3.41 %) and MPPT controller (1.35 %) which is only 1.00 %.

Only SRBC with CGD and SRBC with AGD have body diode conduction loss, P_{BD}. They are 6.29 mW and 4.63 mW respectively. However, when SRBC circuit is applied with MOSFETs parallelism technique, the body diode conduction loss has totally gone. That means, by using this method, it can improve 100 %. On the other hand, using the method of SRBC with compensator-AGD and SRBC with MPPT, this can also successfully eliminate body diode conduction loss.

CHAPTER 5
CONCLUSION AND RECOMMENDATION

5.1 Conclusion

Using SRBC as applied circuit, the MOSFETs have been paralleled at both switches and simulated using PSPICE. The configurations are from 1×1 up to 4×4. The simulation is divided into two sections which are CCM and DCM mode. Among the 16 configurations, there is one optimized configuration that gives the best result. The optimized configuration is chosen based on few factors; node voltage (V_N), inductor current (I_L), output voltage (V_o) and output current (I_o).

The optimized configuration for CCM is (*S1*:4, *S2*:1). Theoretically MOSFETs parallelism is able to increase output current and also reduce body diode conduction loss. In the simulation, it is found that by paralleling MOSFETs, it can increase output current. However, it increases only by few percents which is 8.27 $\%\left(\left|\frac{770.26mA-833.955mA}{770.26mA} \times 100\ \%\right|\right)$. Nevertheless, body diode conduction has been successfully reduced by paralleling the MOSFETs which is 36.45 $\%\left(\frac{16.87mW-10.72mW}{16.87mW} \times 100\ \%\right)$. However, the drawback of this method (MOSFETs parallelism) is the reduction in output voltage, 0.148 % $\left(\frac{2.6959-2.6919}{2.6959} \times 100\ \%\right)$ as the output current increases.

As for DCM, the optimized configuration is (*S1*:4, *S2*:3). The output current increases by only 12.48 $\%\left(\left|\frac{758.52mA-674.382mA}{758.52mA} \times 100\ \%\right|\right)$. Since output current increases, inductor current also increases by 16.93 % $\left(\left|\frac{707.294mA-827.023mA}{707.294mA} \times 100\ \%\right|\right)$. Similar to CCM, the drawback of this

technique is that value of output voltage decreases as the output current increases which is 8.79 % $\left(\frac{3V-2.7362V}{3V} \times 100\ \%\right)$.

5.2 Recommendation

There are several recommendations for future work:

- Adding more configuration of MOSFETs parallelism in conventional SRBC circuit.
- Using another type of applied circuit to see how much paralleling of the MOSFETs can influent the results.

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APPENDIX A

GANTT CHART OF THE PROJECT

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	Selection of Project Topic	■														
2	Preliminary Research/Design Work		■	■												
3	Submission of Preliminary Report (Initial Proposal)				✱											
4	Project Work i.e. modeling and simulation of converters				■	■	■	■								
5	Submission of Progress Report								✱							
6	Seminar								■	■	■	■				
6	Project work continue i.e. modeling and simulation of converters and analysis of results								■	■	■	■				
7	Submission of Dissertation Final Draft												✱			
8	Oral Presentation															✱
9	Submission of Project Dissertation														✱	

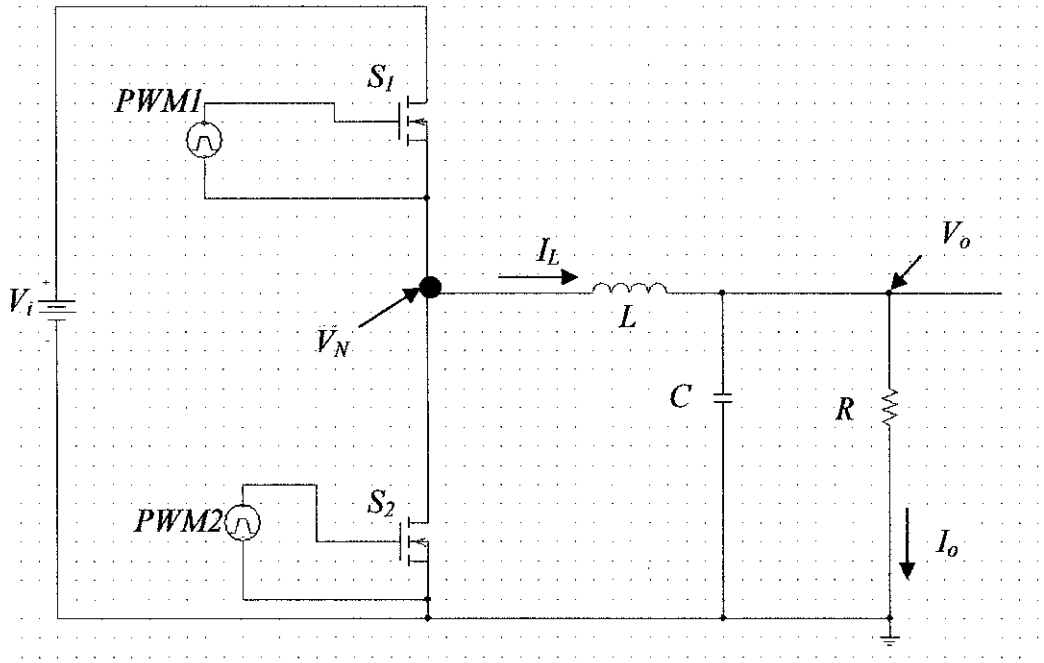
✱ Suggested milestone

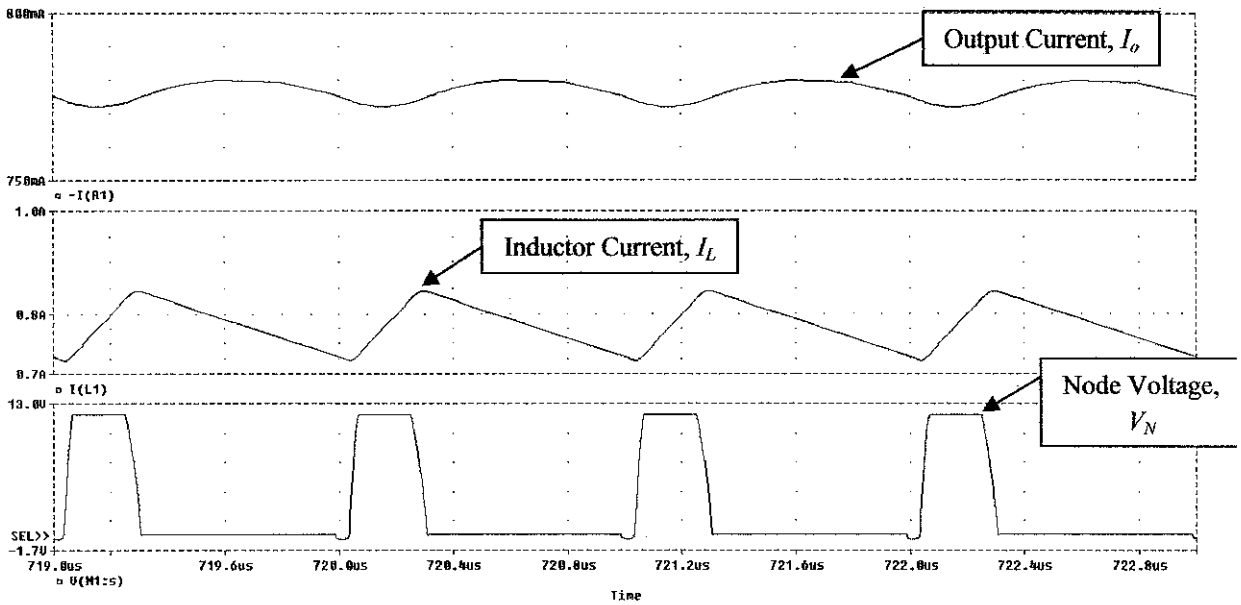
■ Process

APPENDIX B

SRBC circuit with MOSFETs parallelism technique for CCM

1) Configuration of (*S1*:1; *S2*:1)





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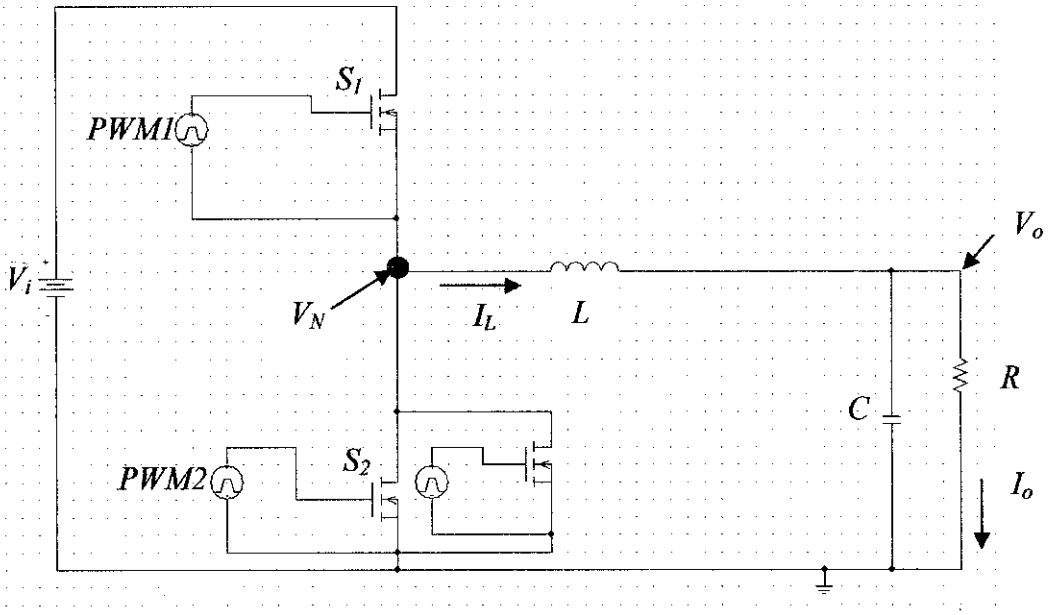

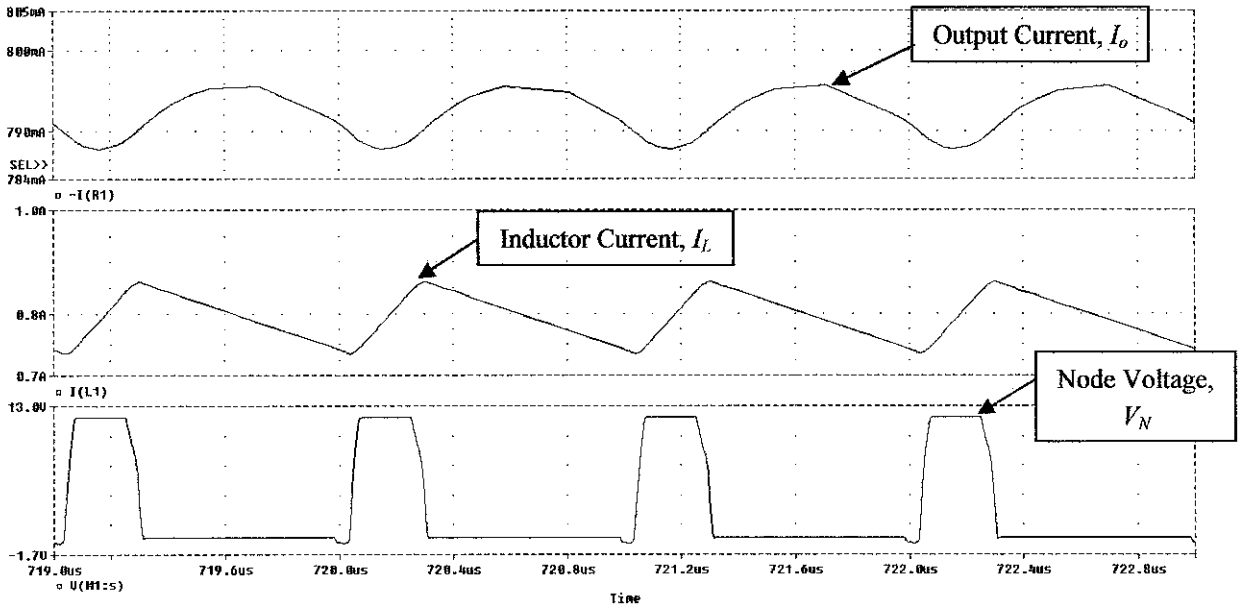

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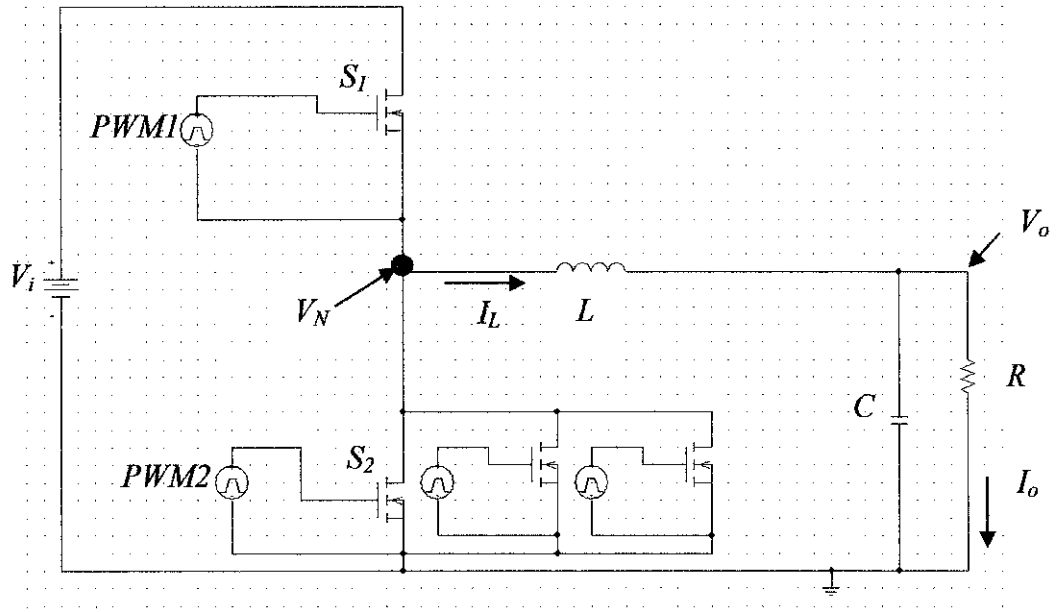

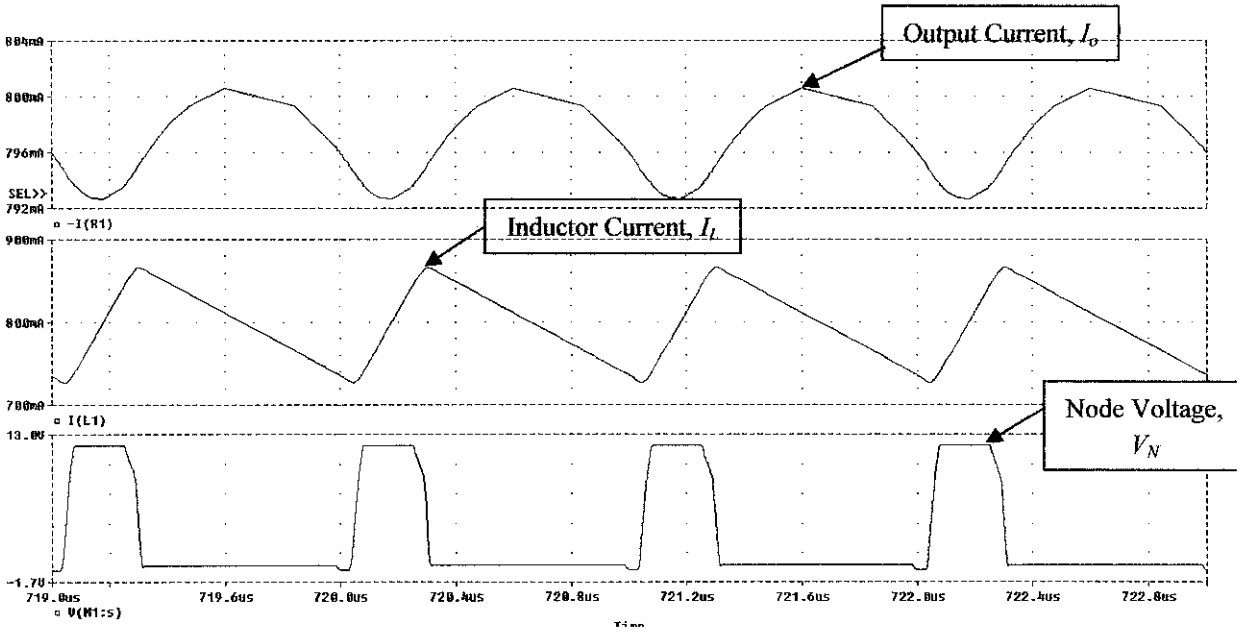

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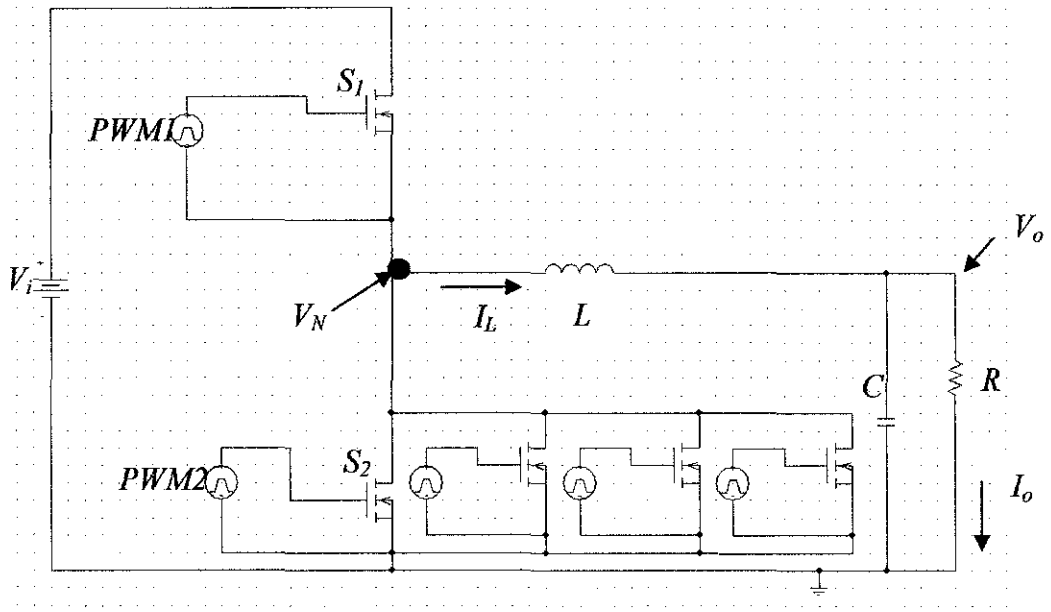

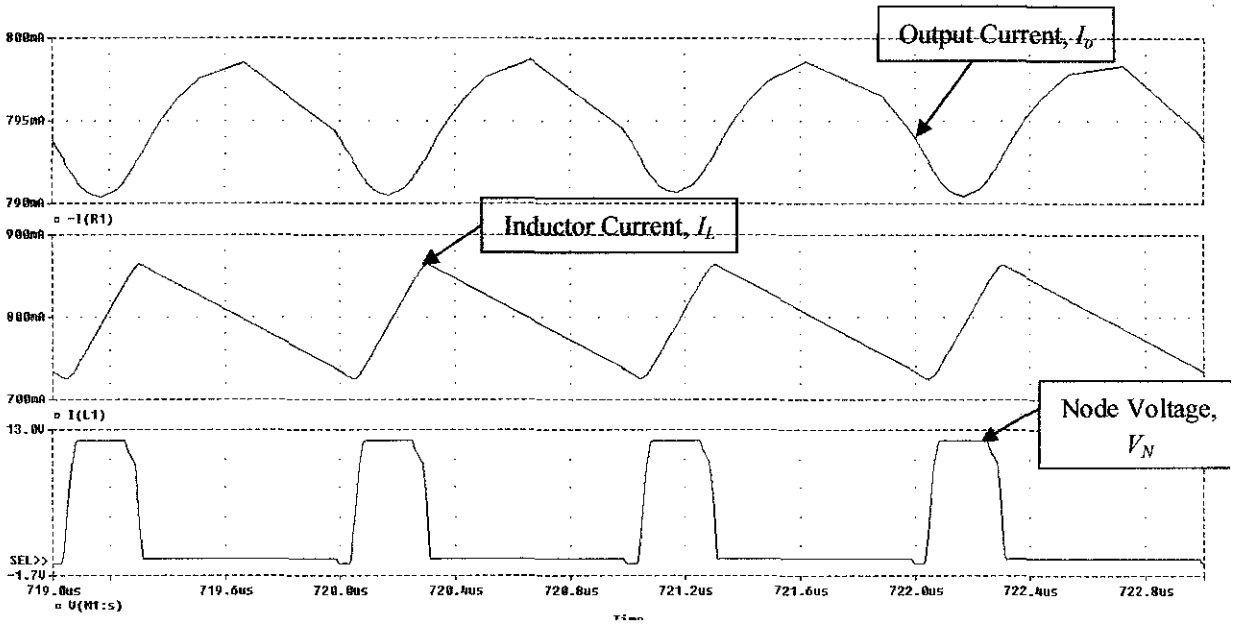

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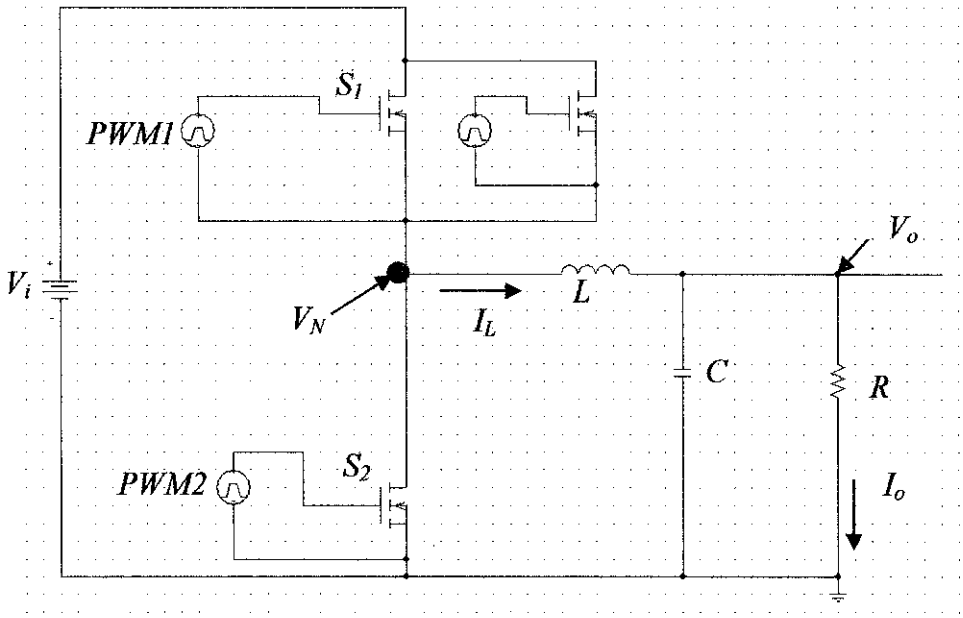

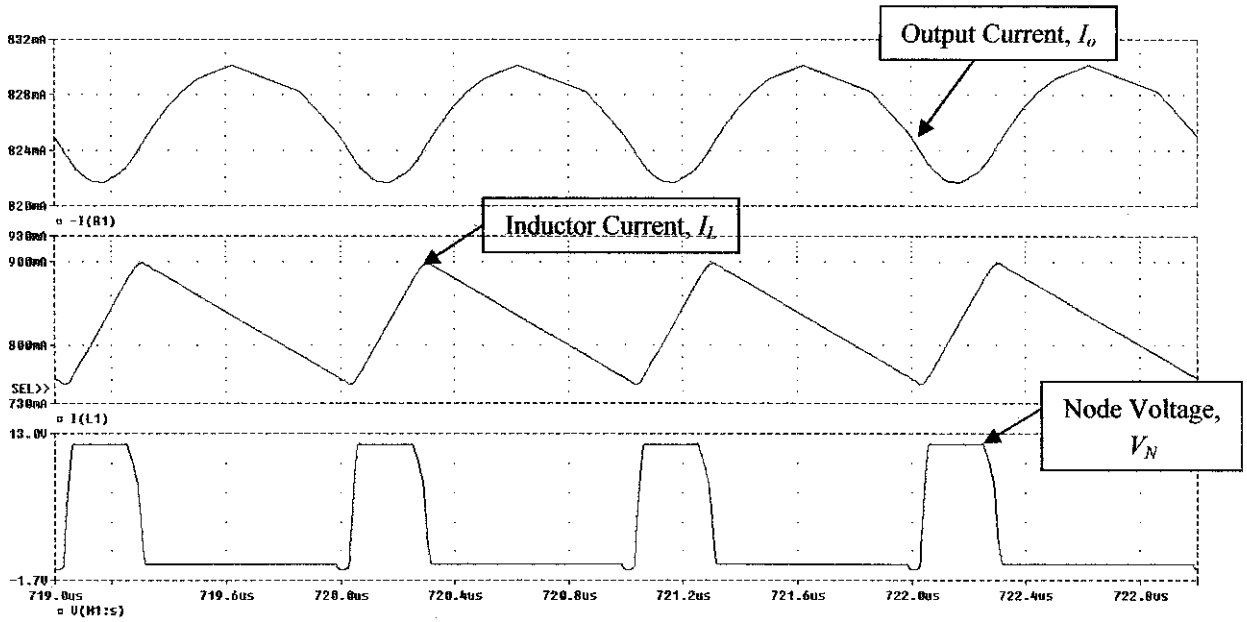

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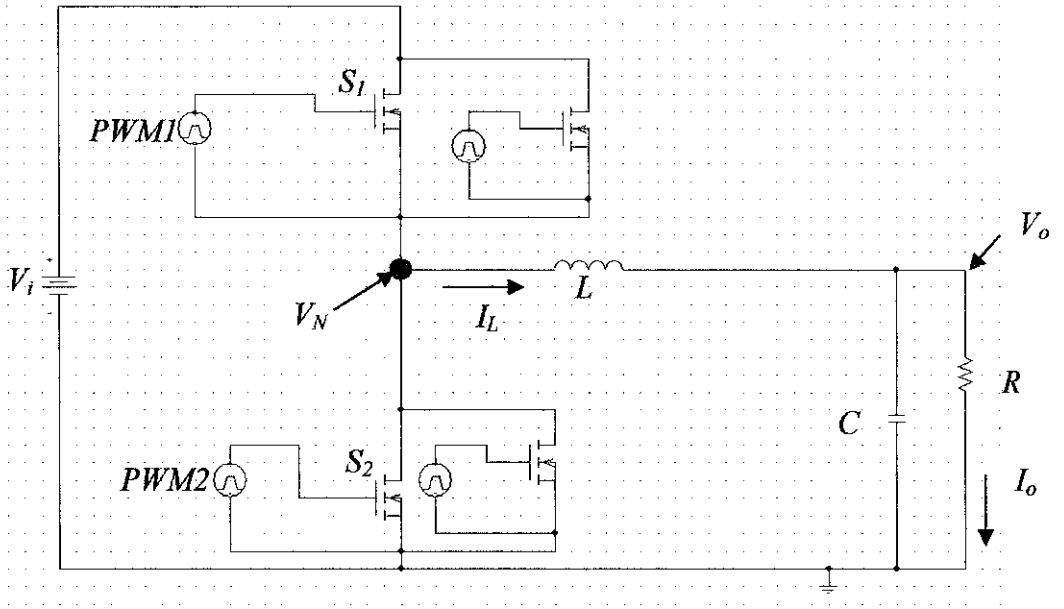

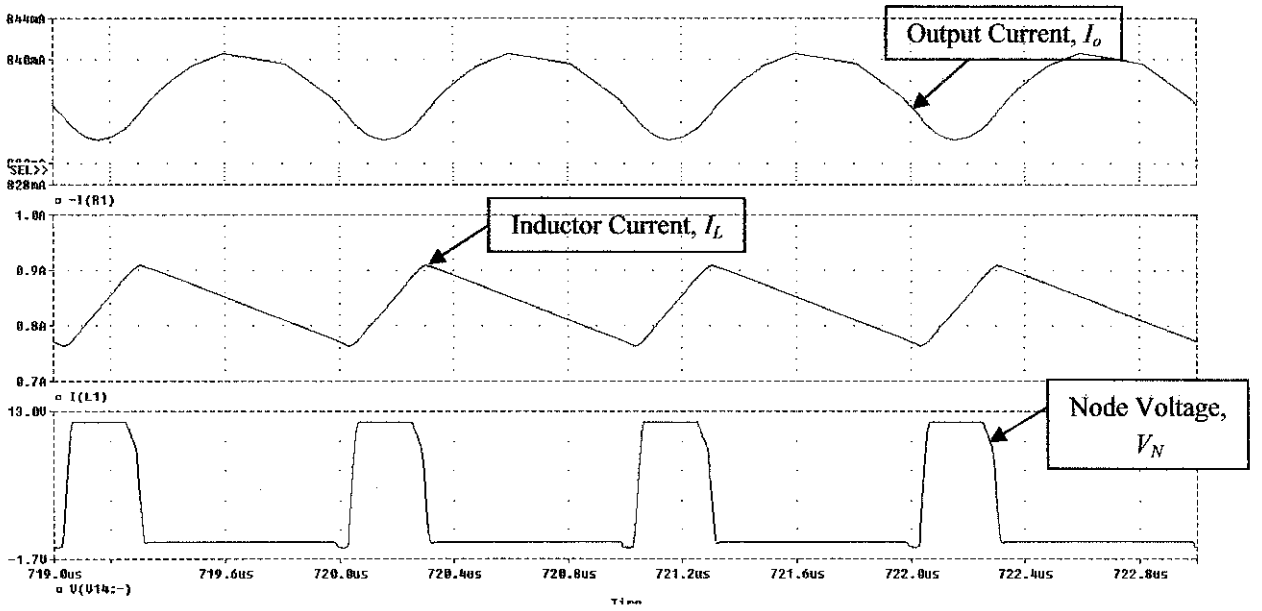

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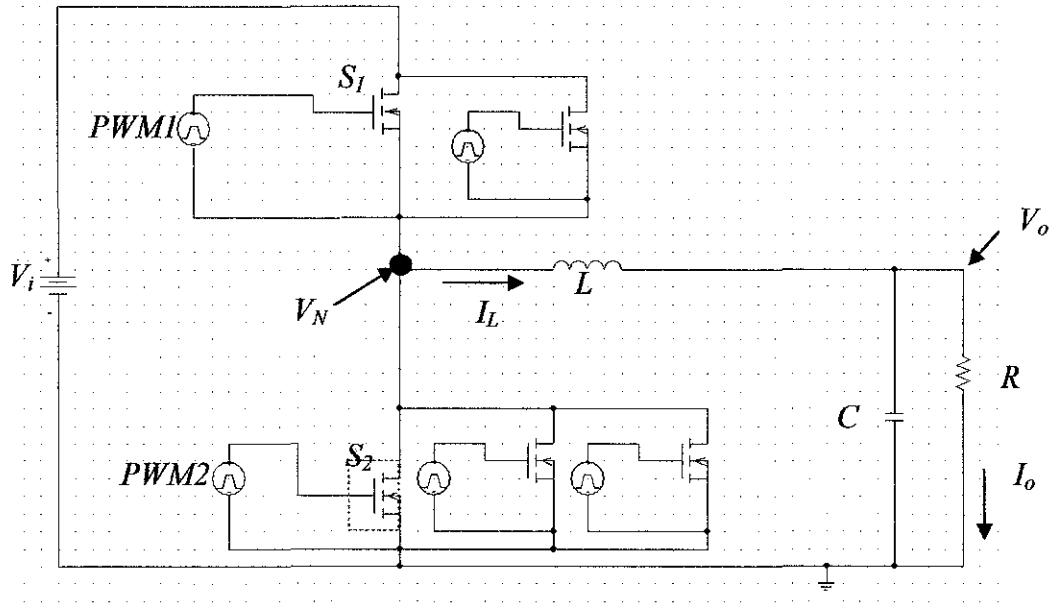

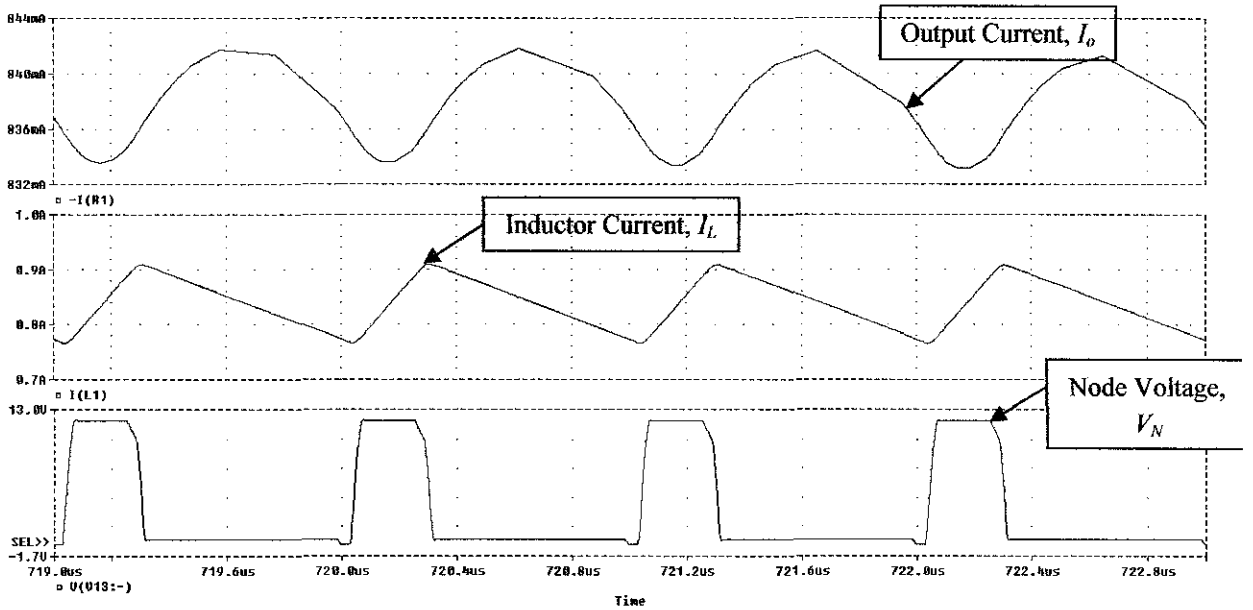

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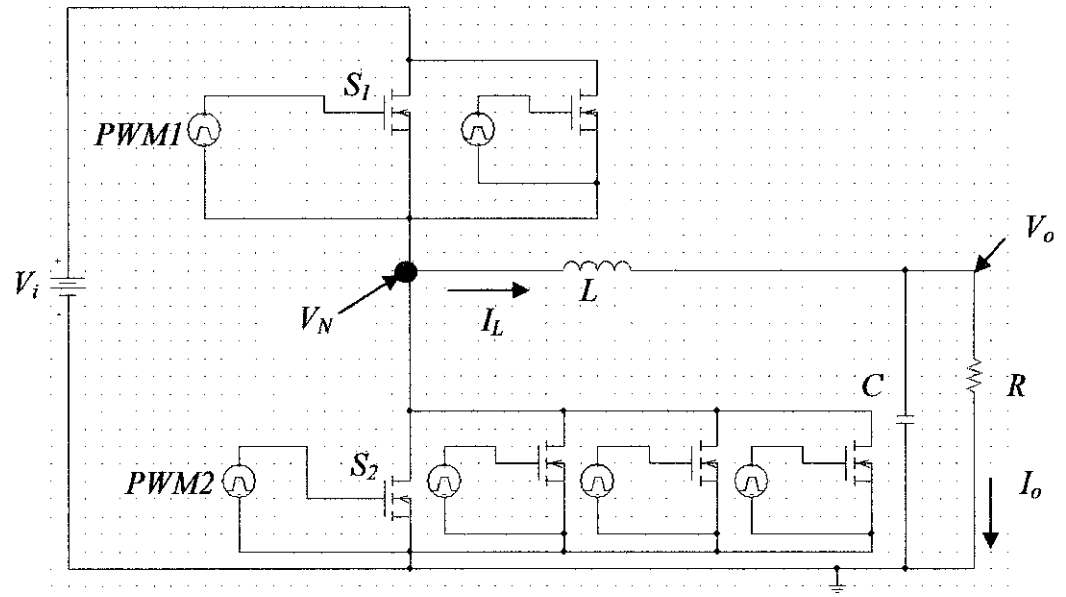

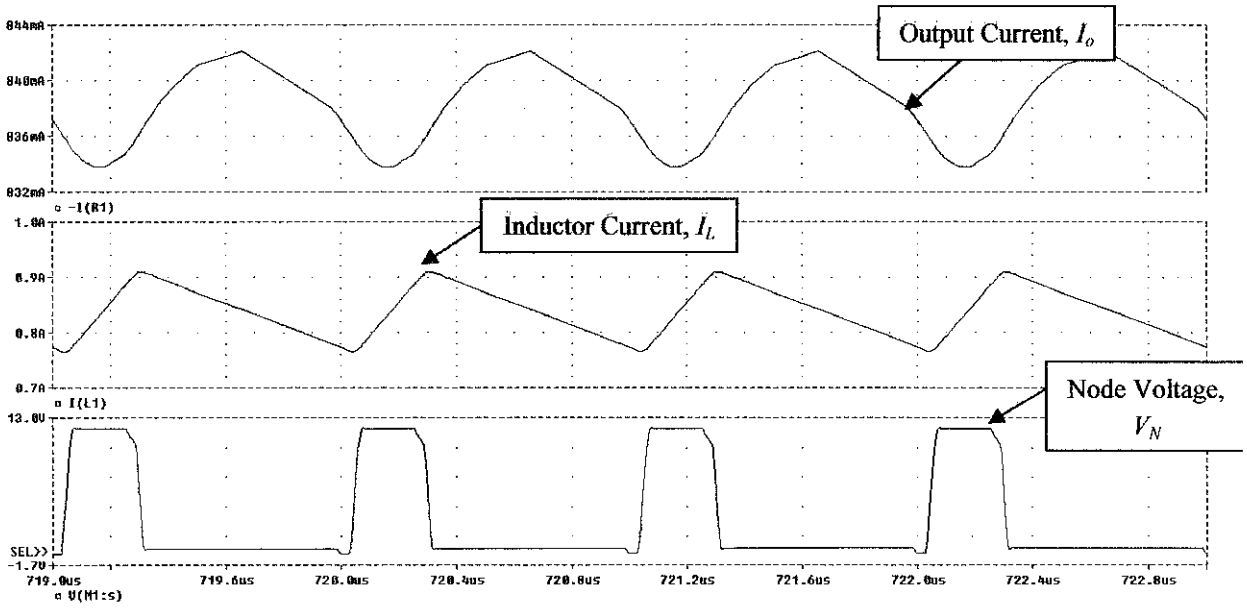

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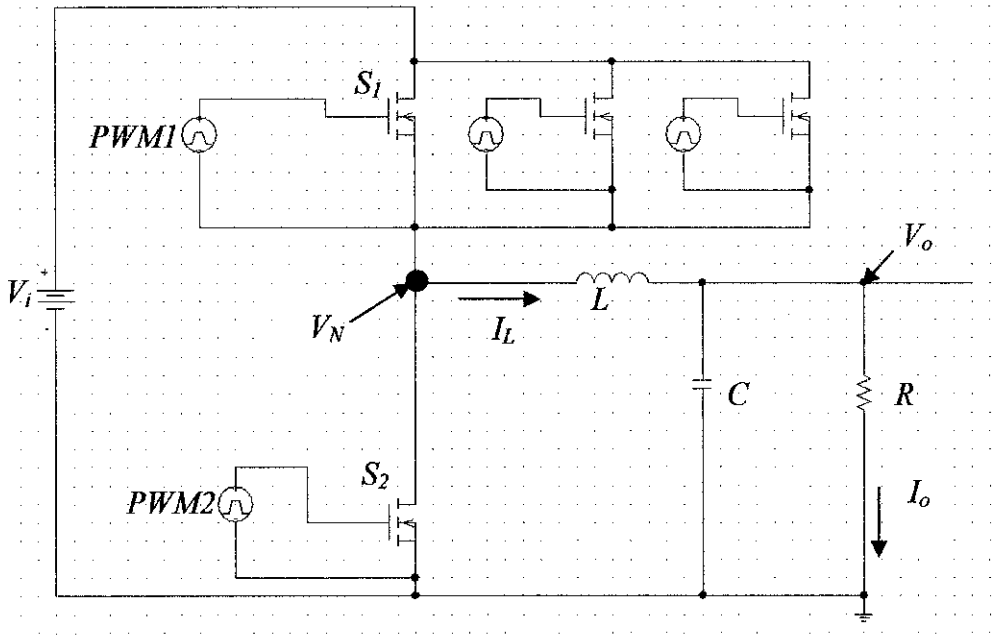

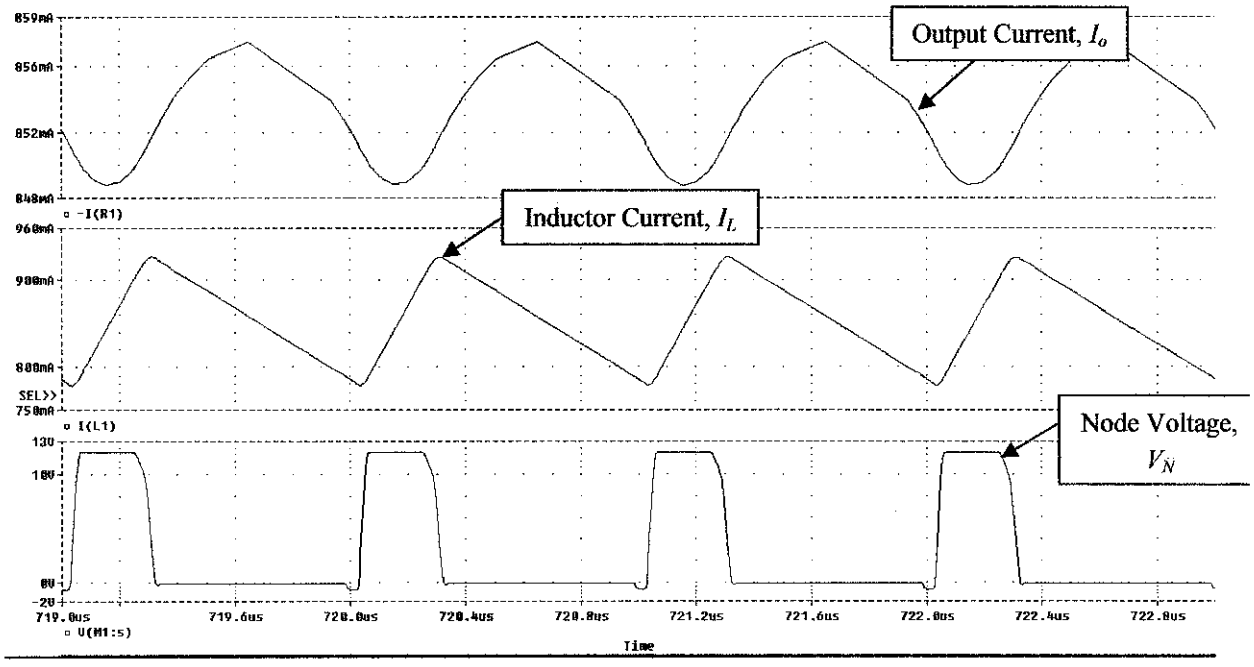

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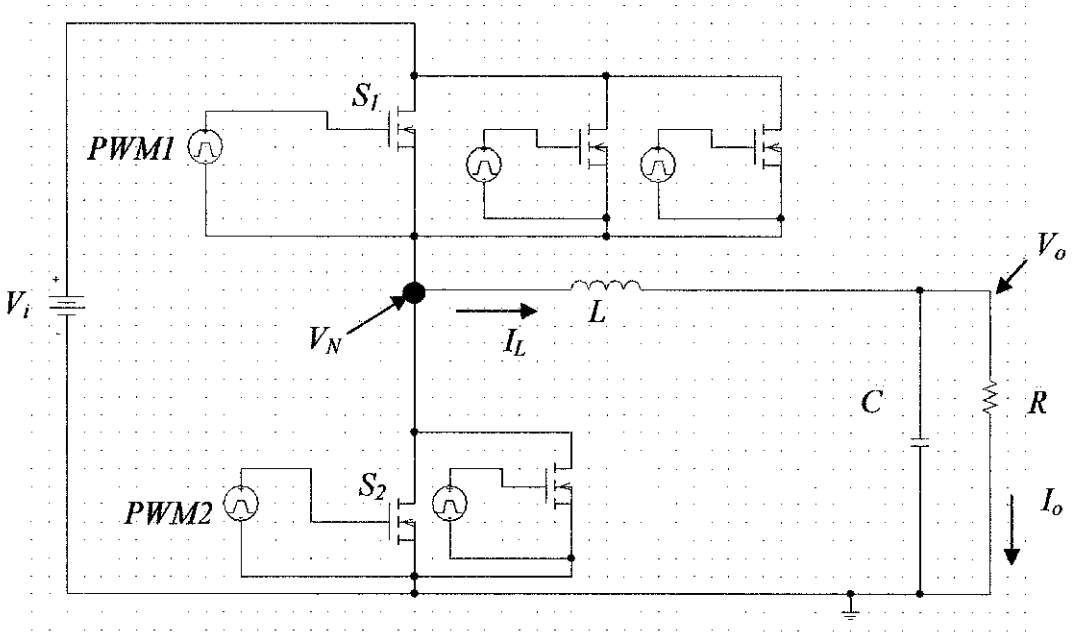

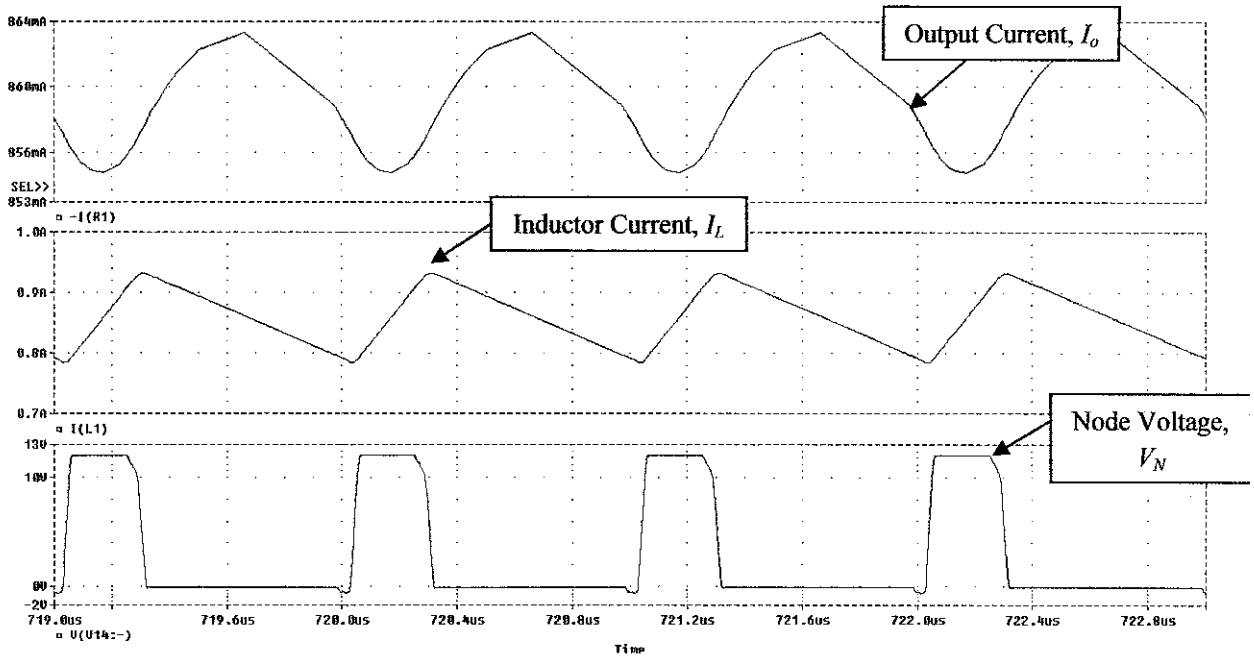

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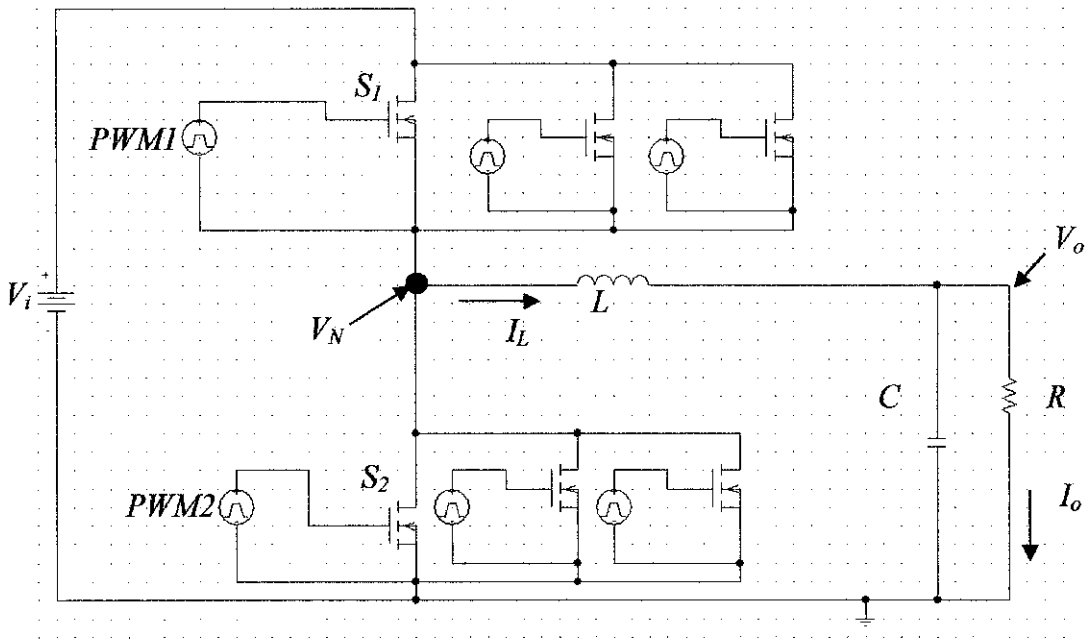

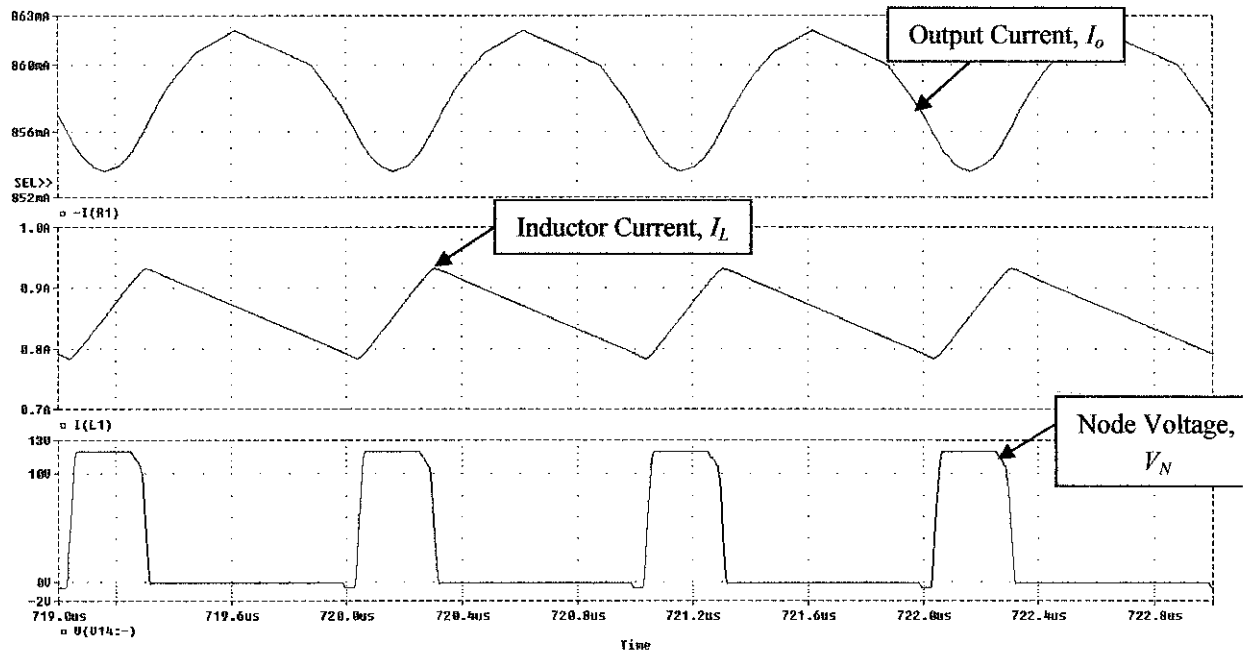

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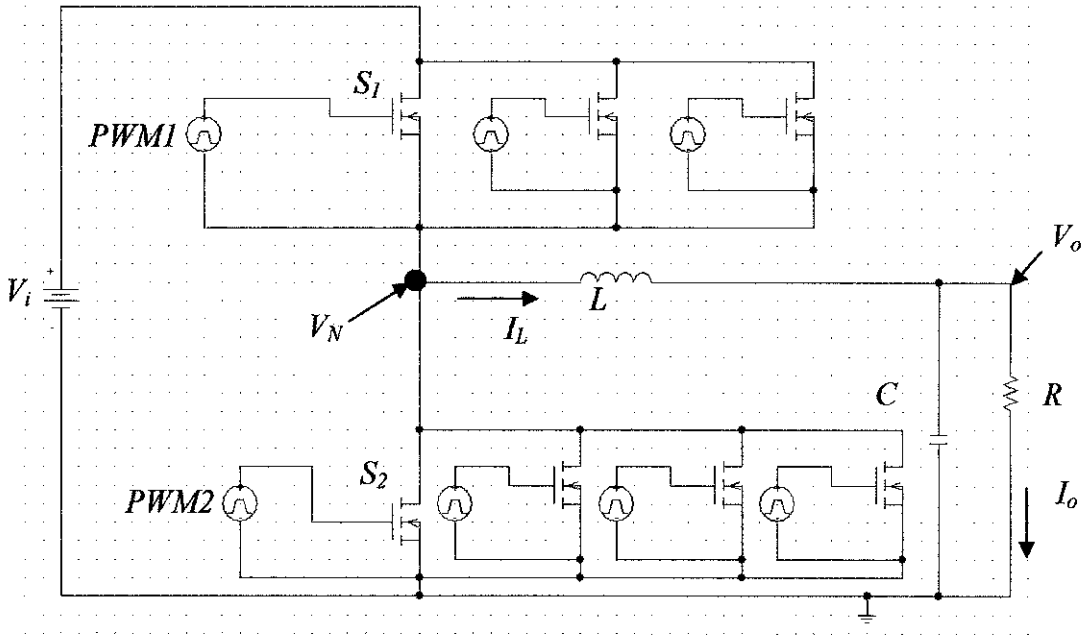

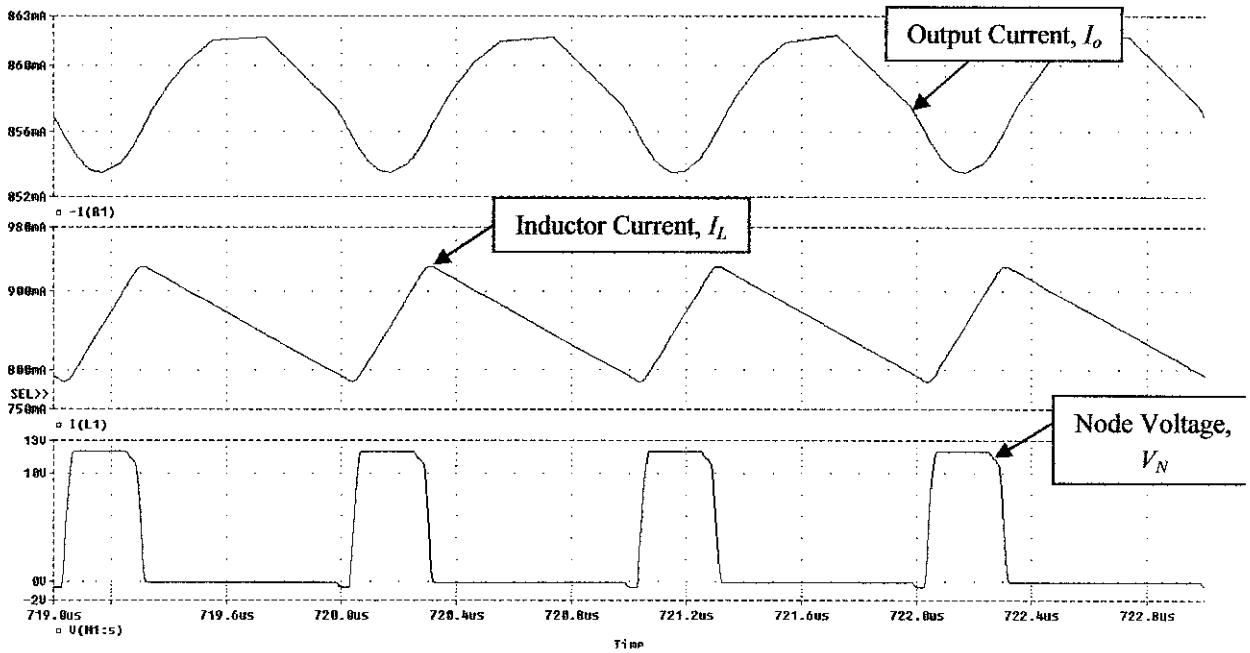

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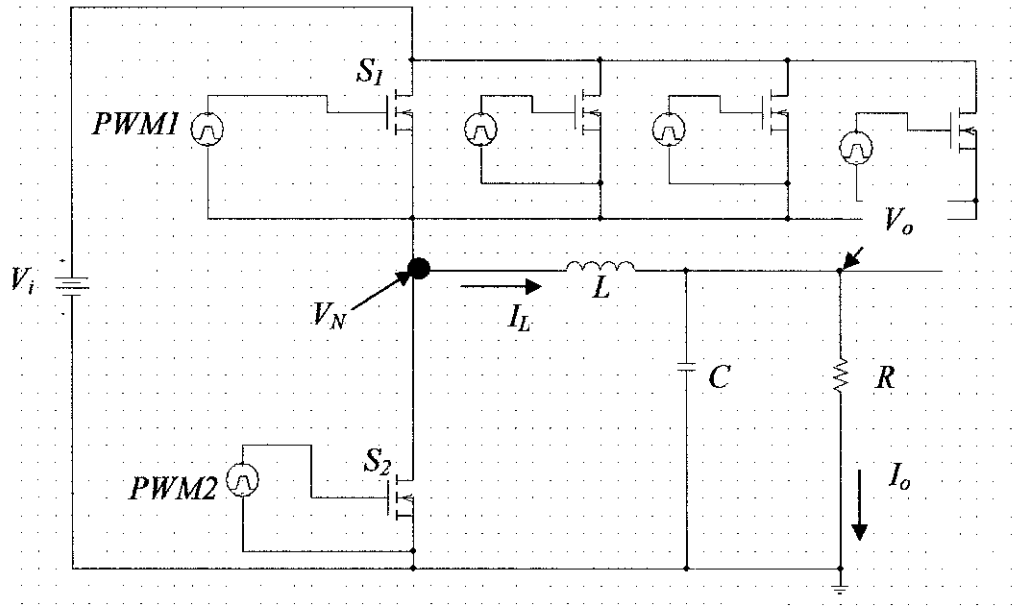

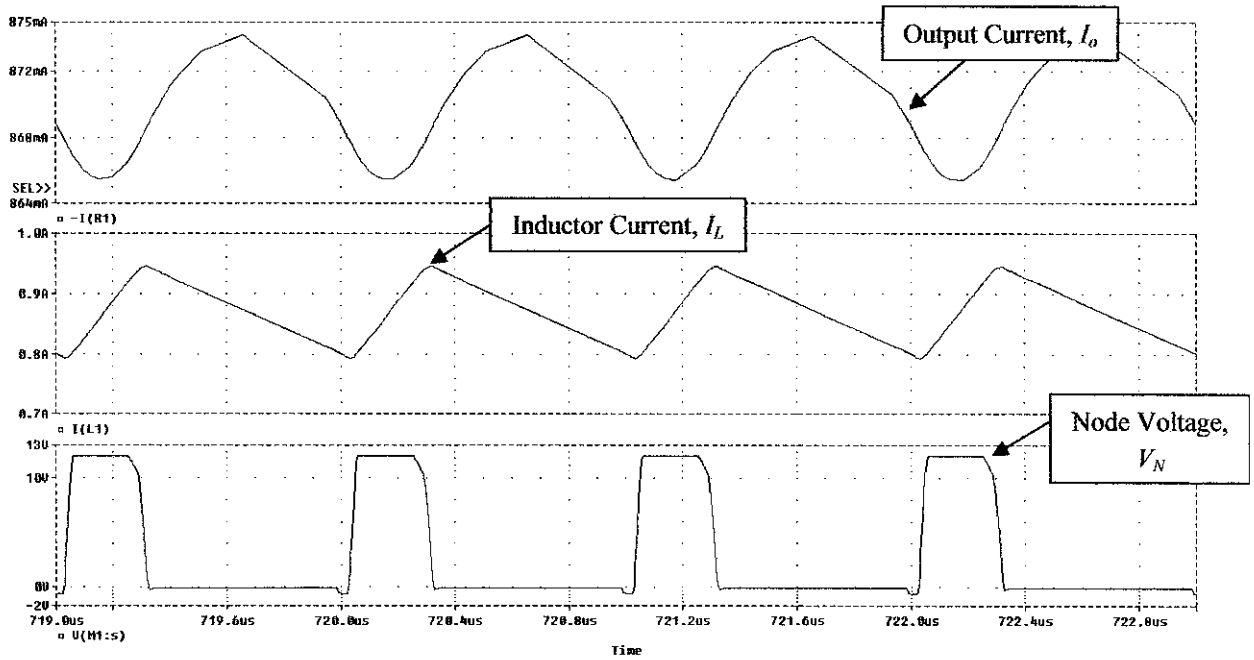

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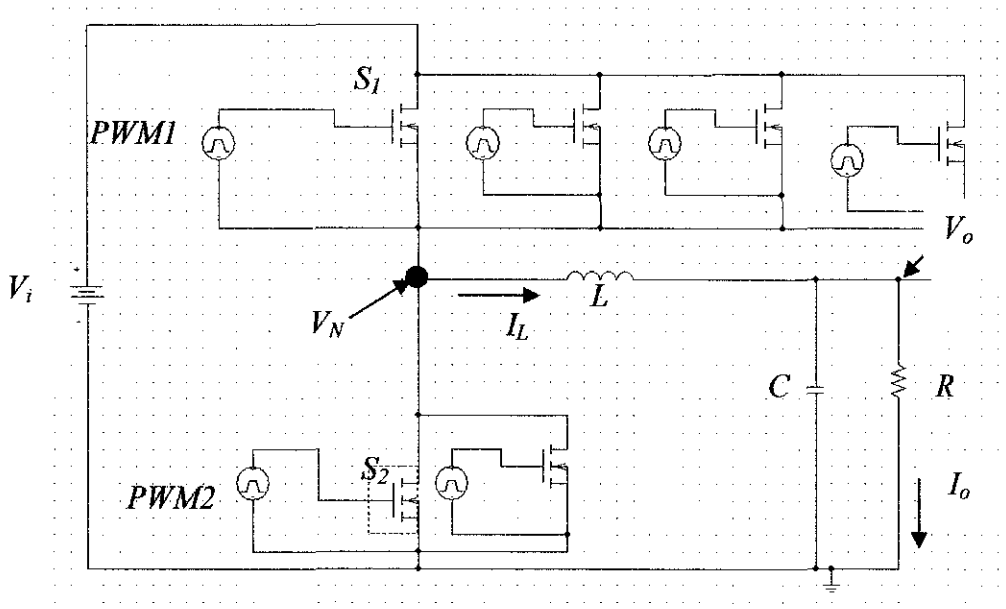

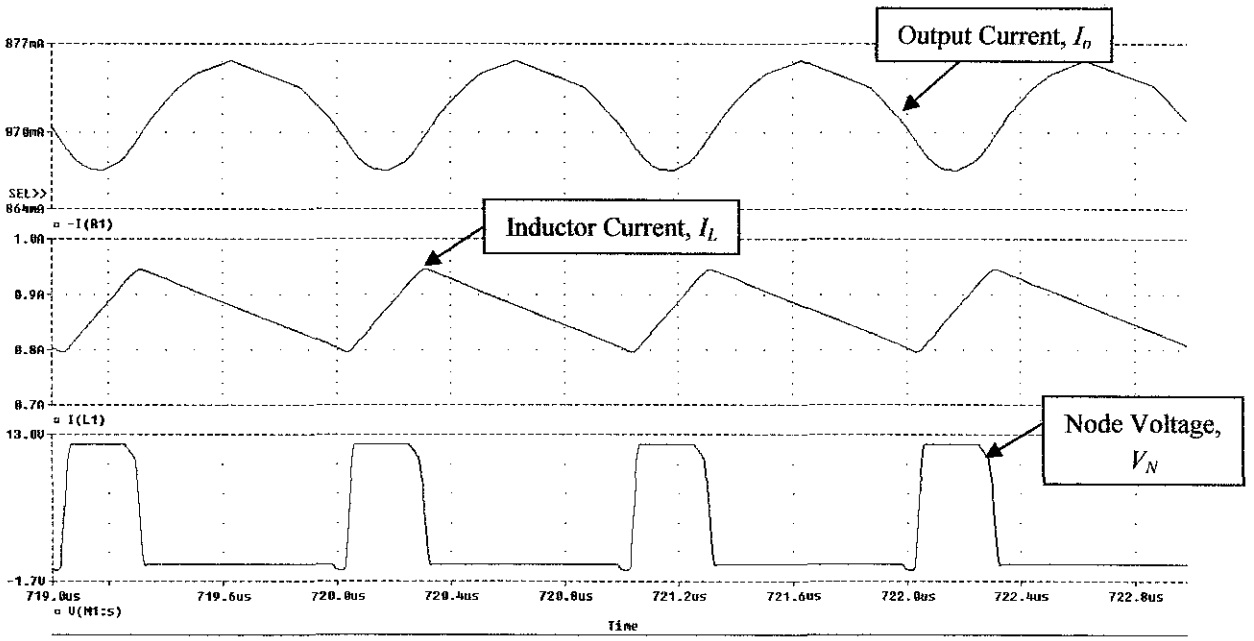

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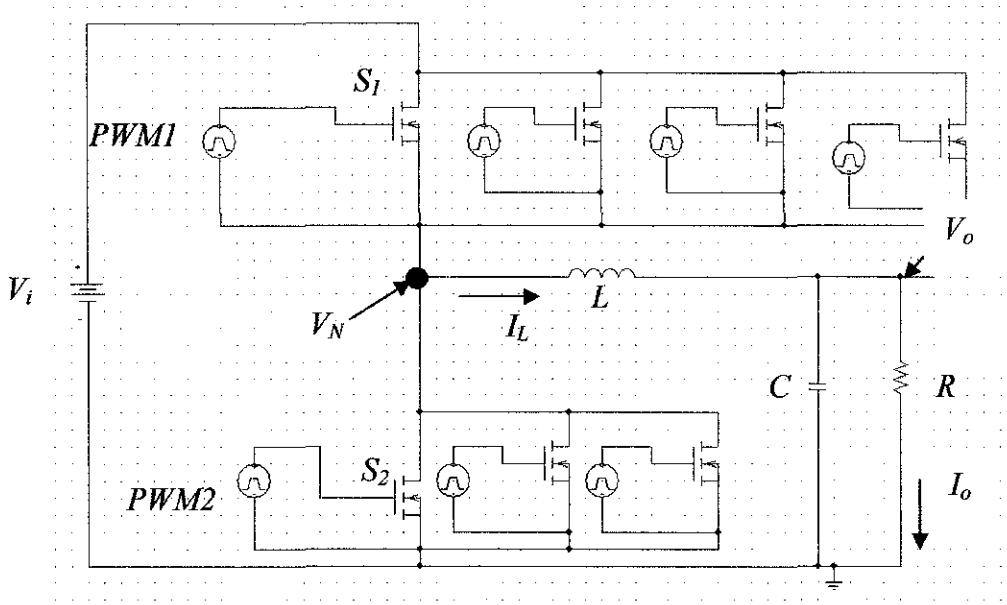

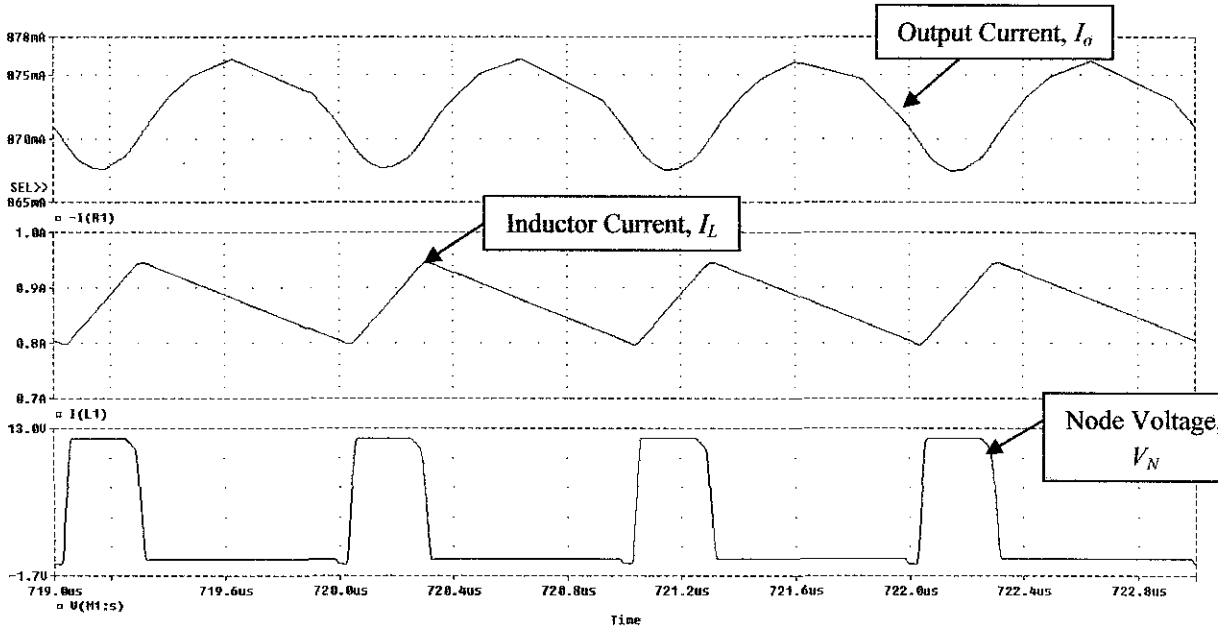

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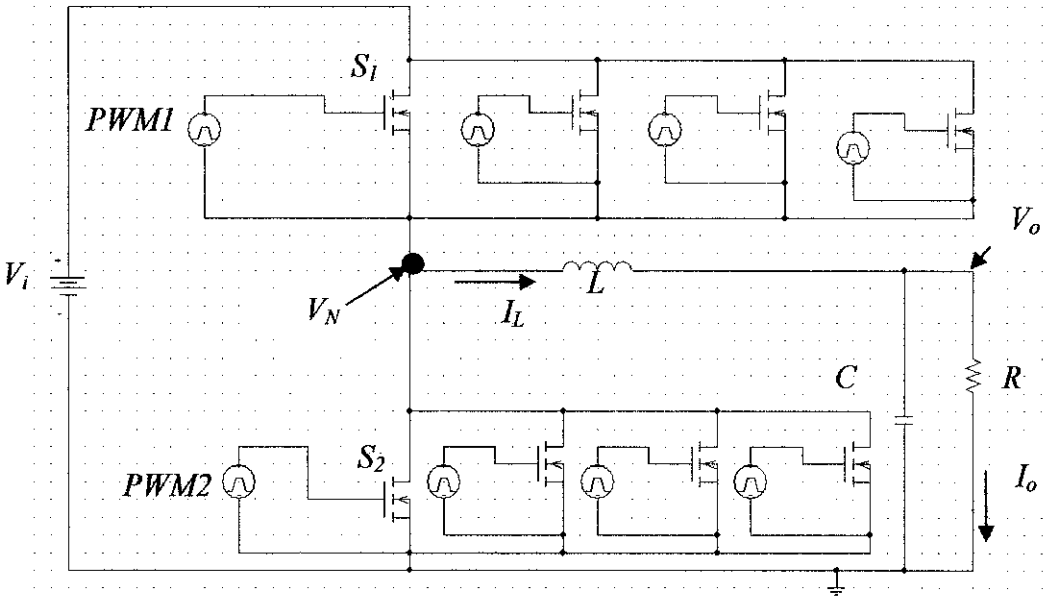
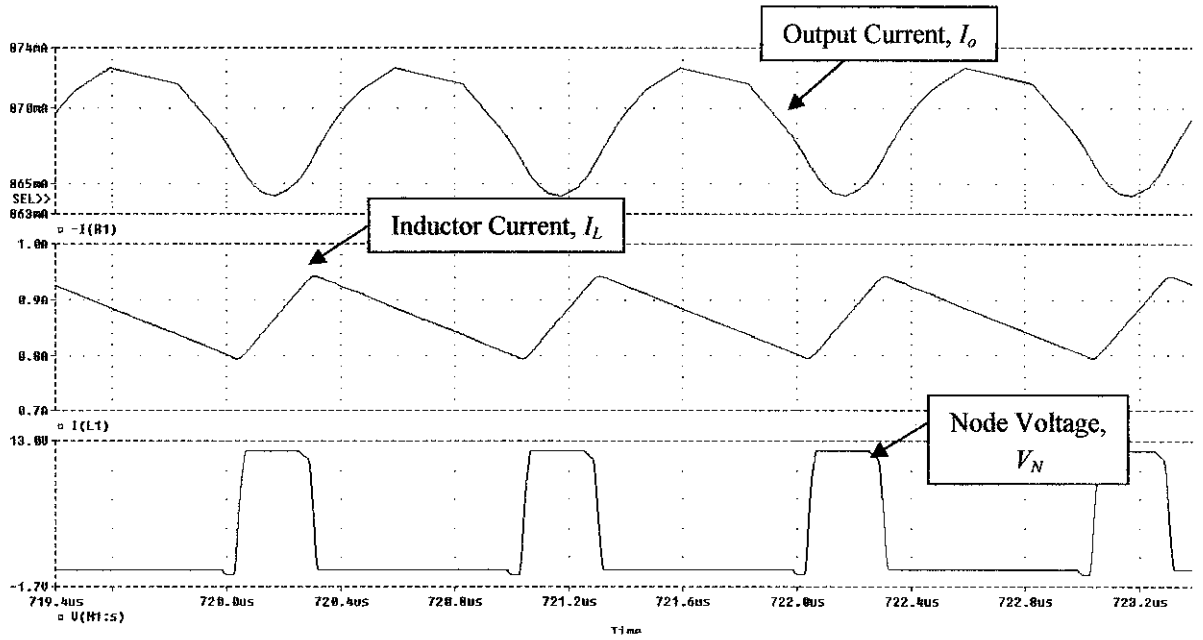
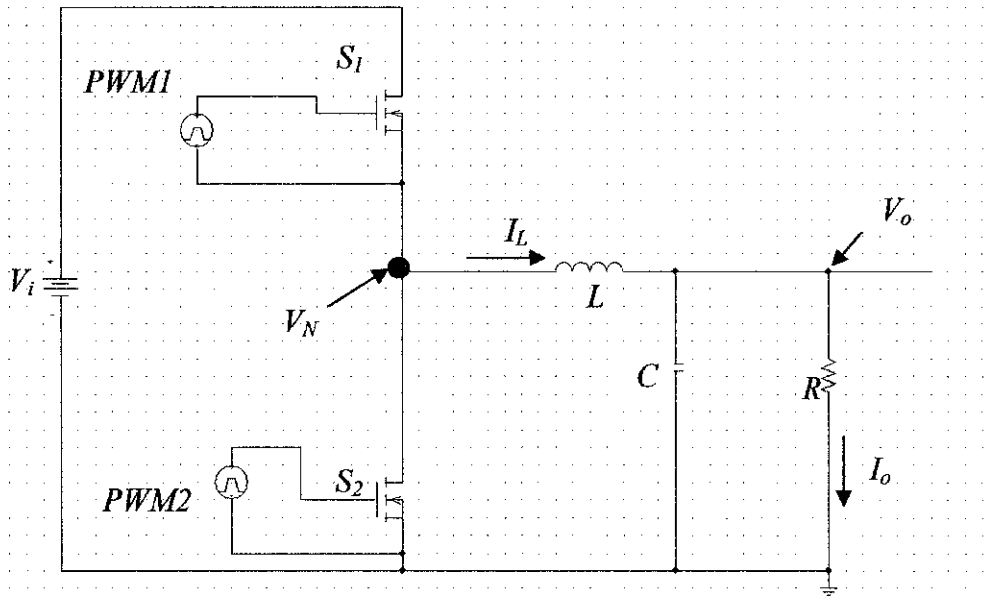
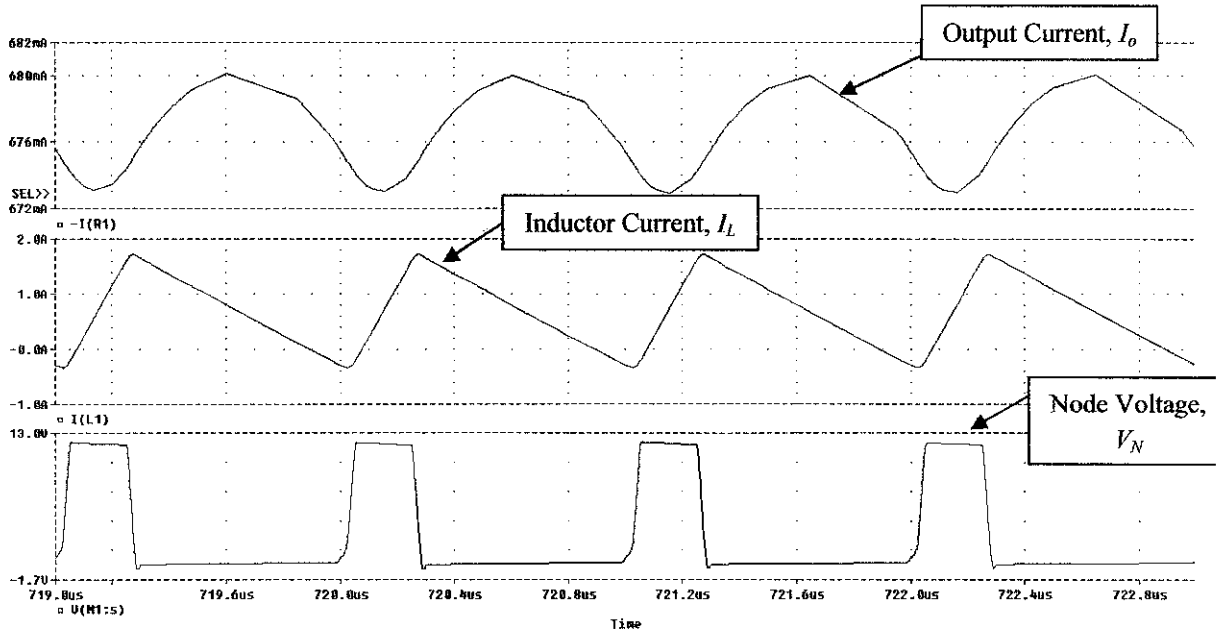




SRBC circuit with MOSFETs parallelism technique for DCM

1) Configuration of (*S1*:1; *S2*:1)





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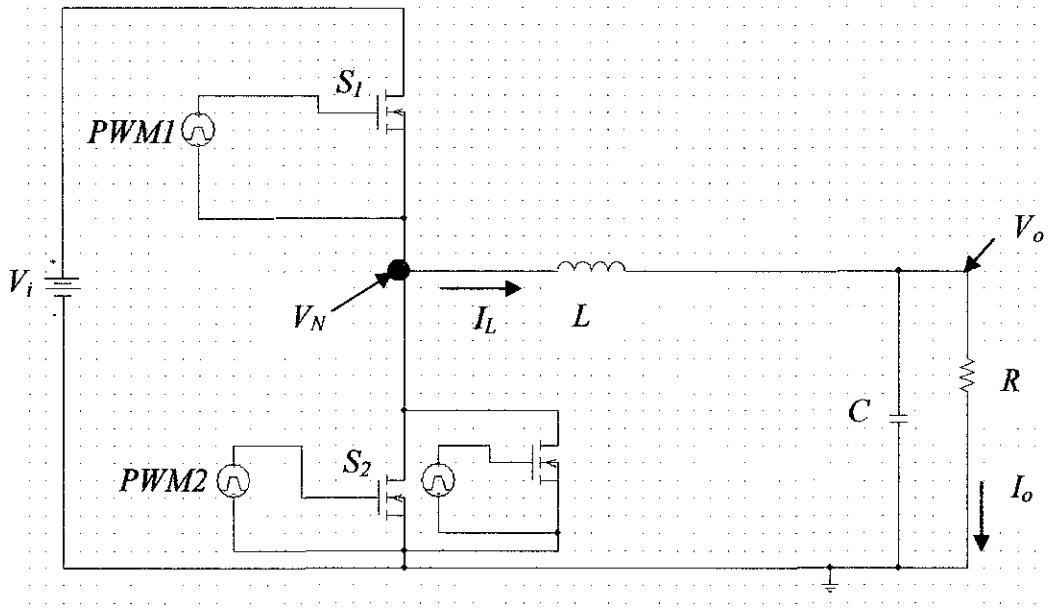

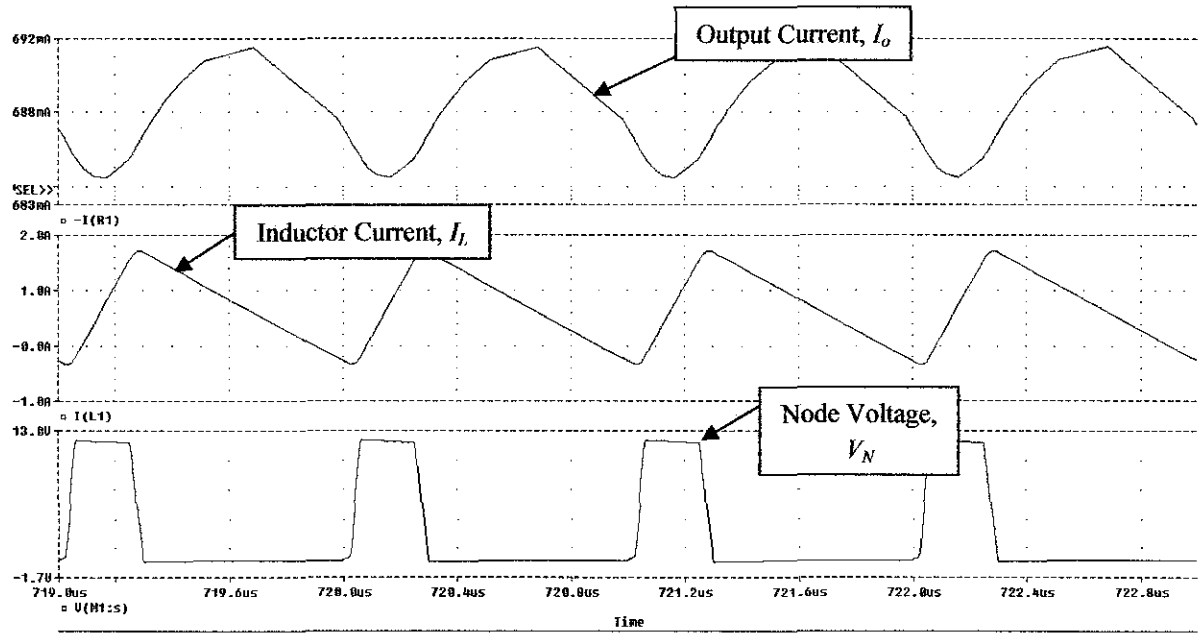

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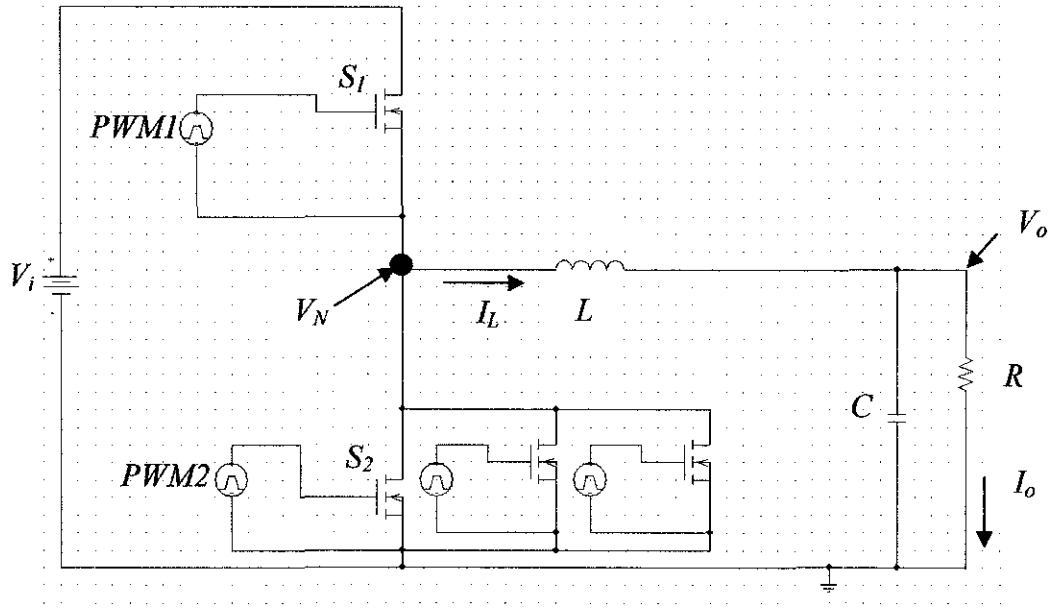

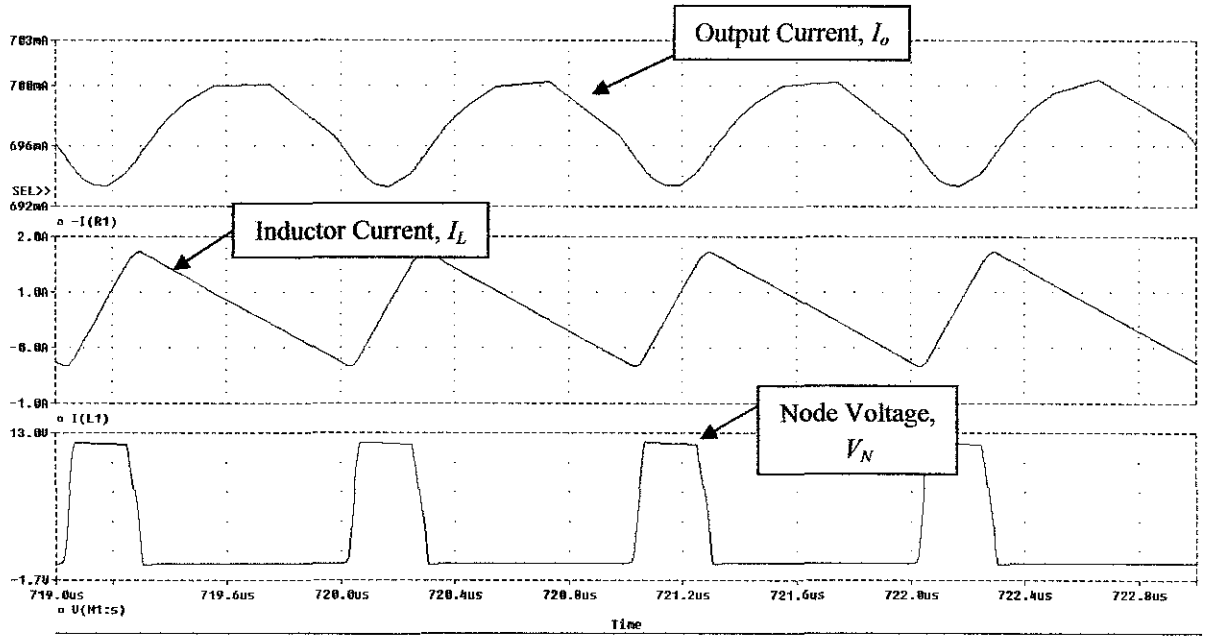

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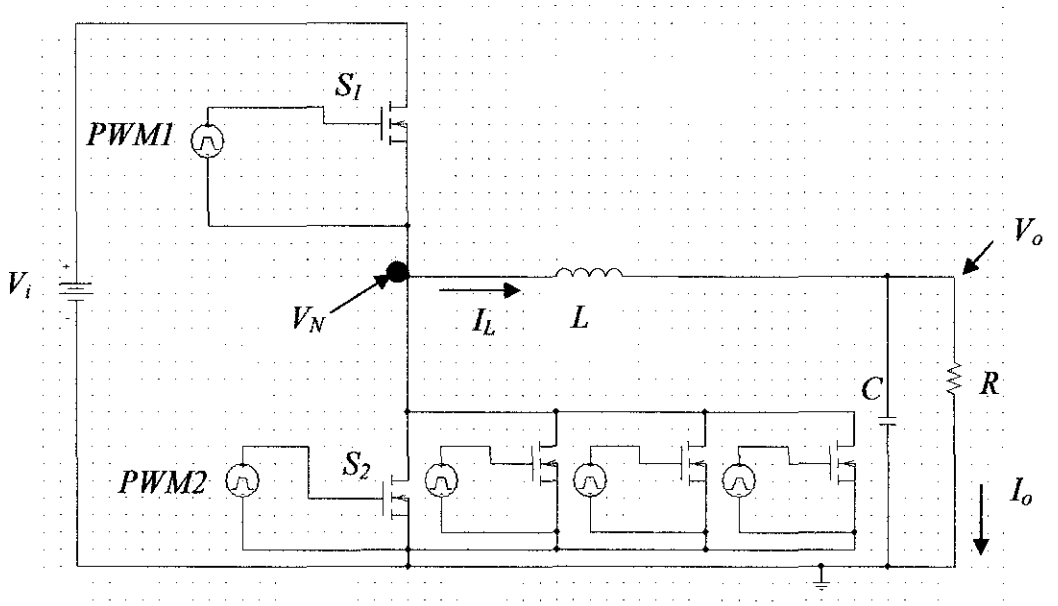

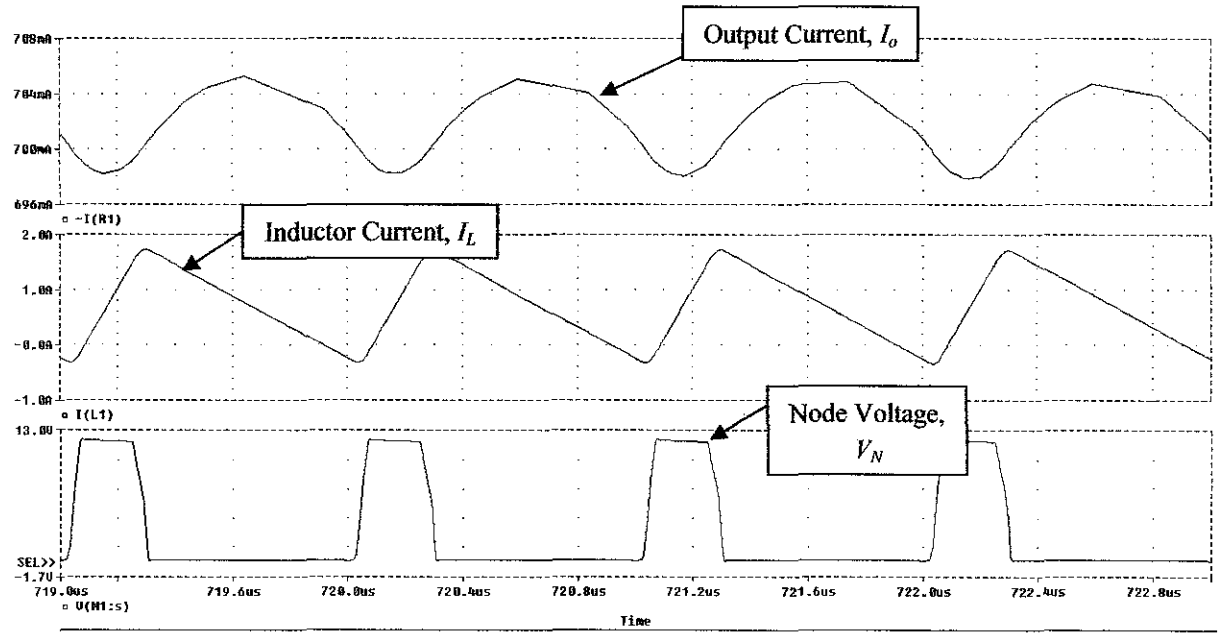

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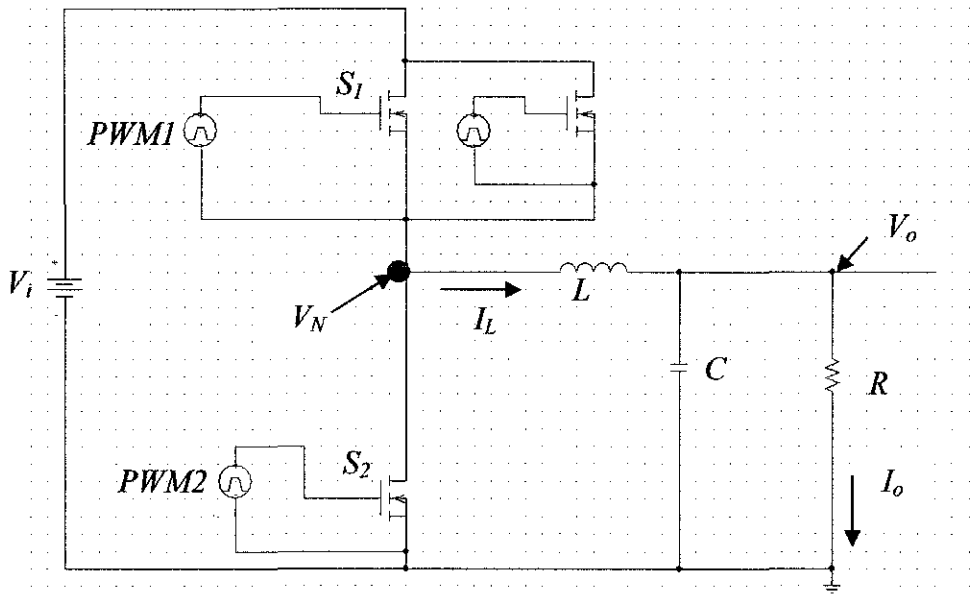
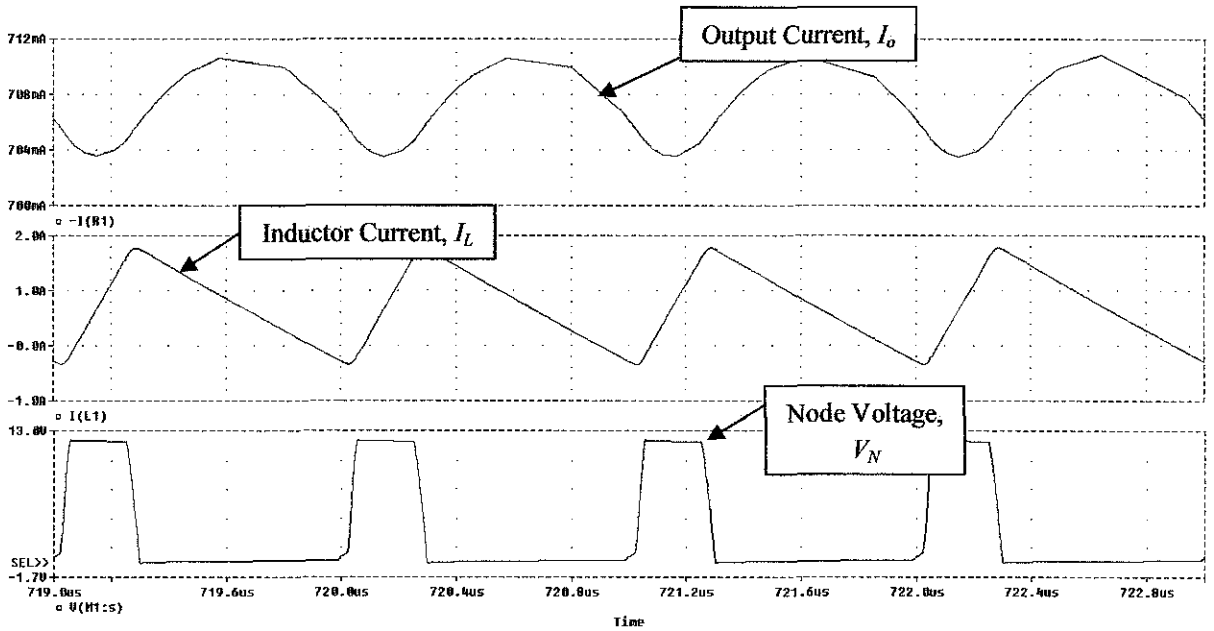
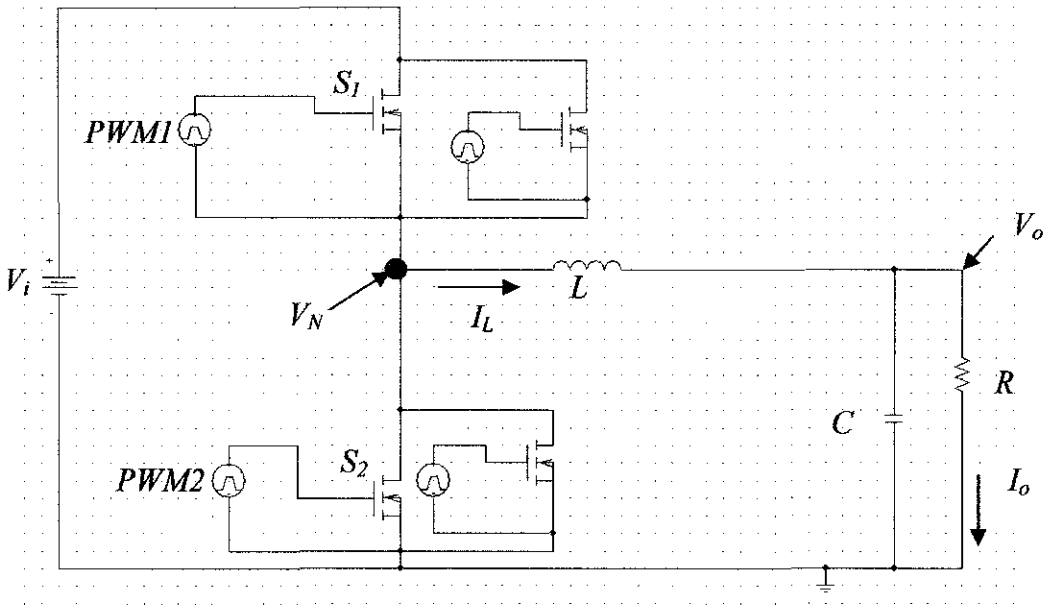
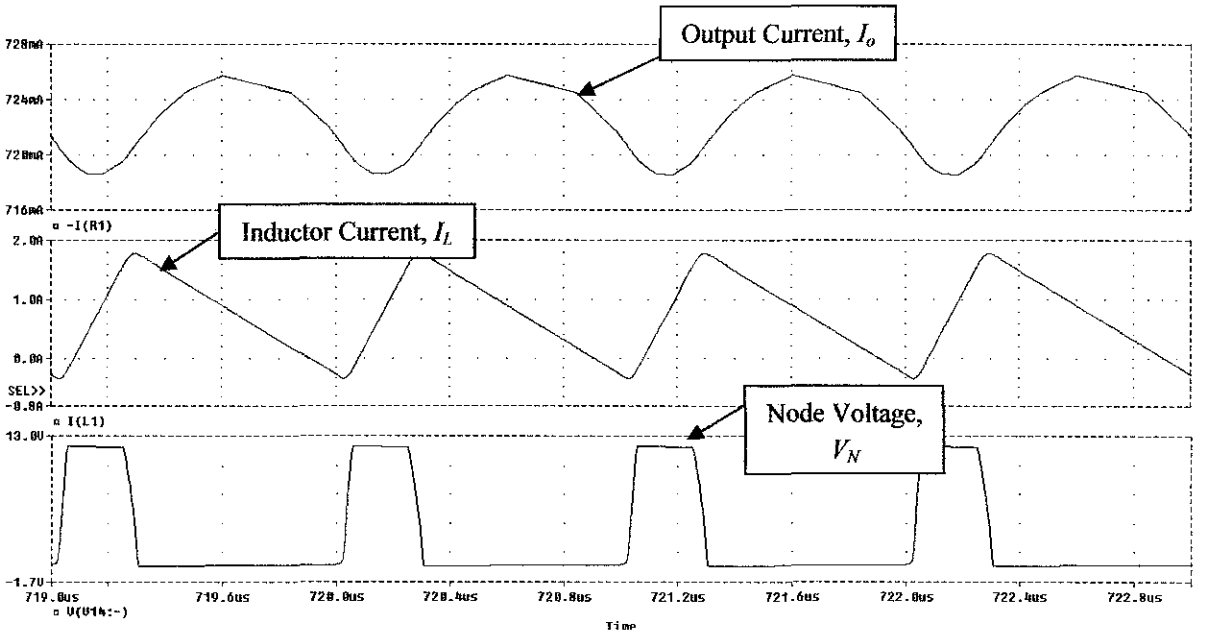


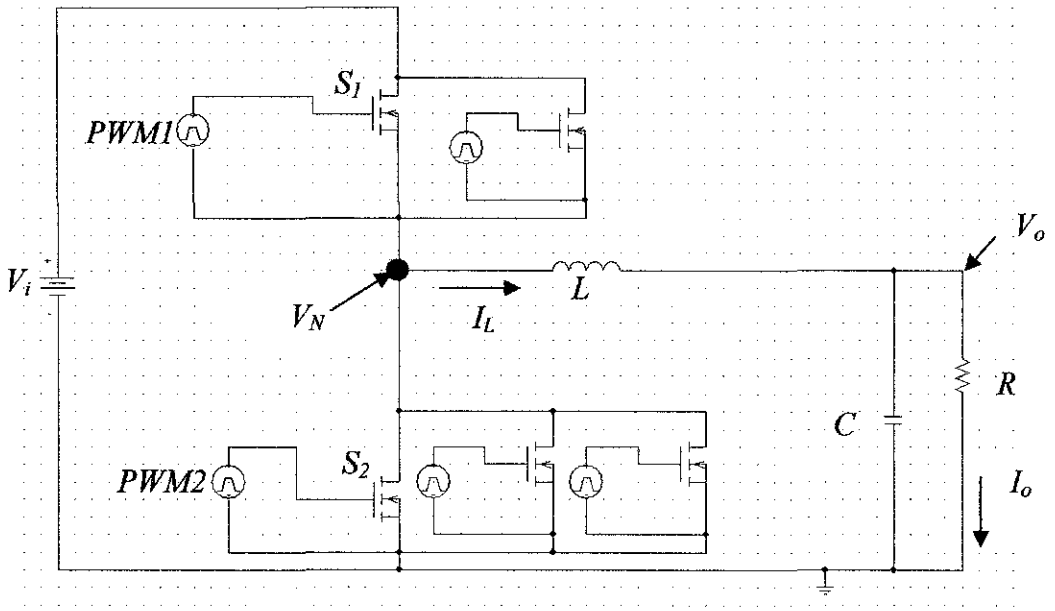


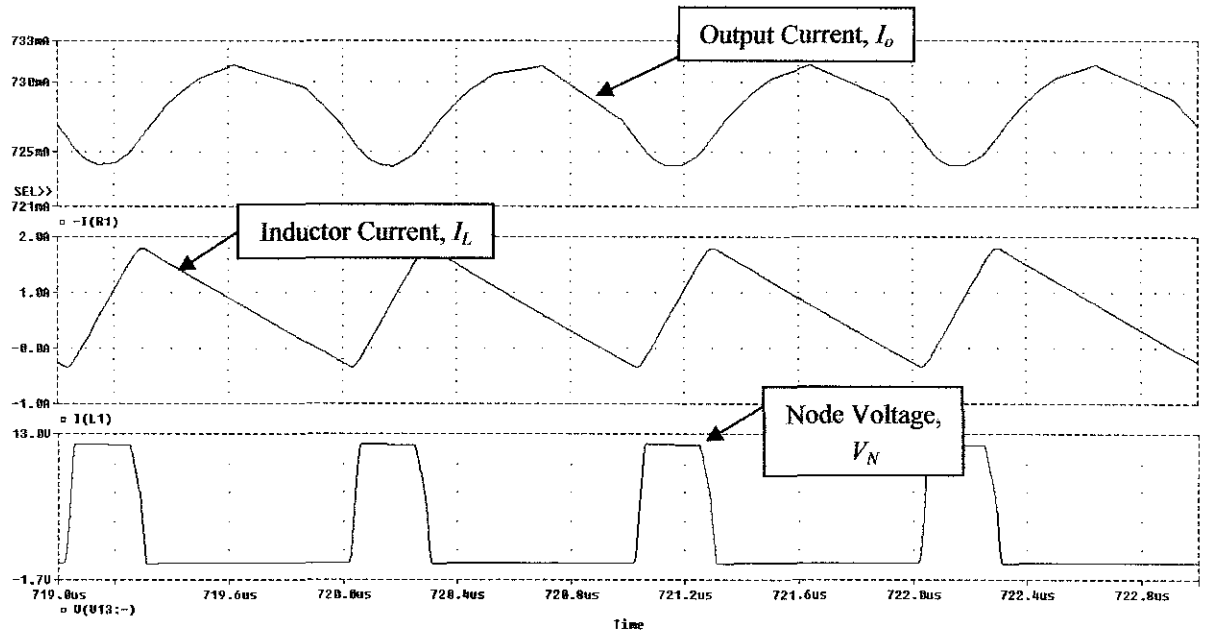
6) Configuration of (*S1*:2; *S2*:2)



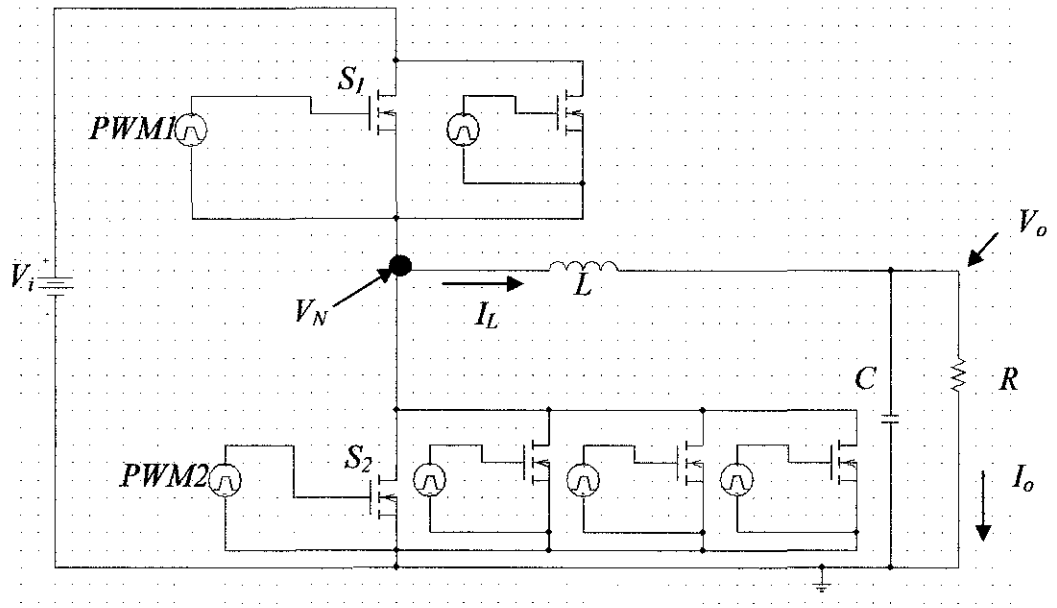


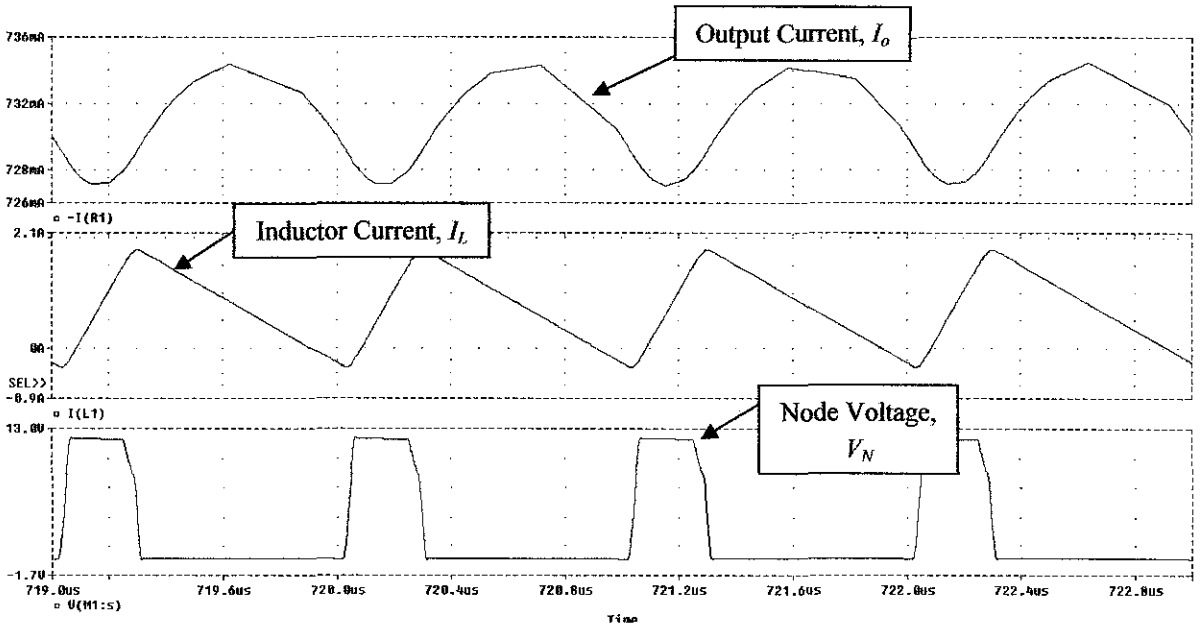
7) Configuration of (*S1*:2; *S2*:3)



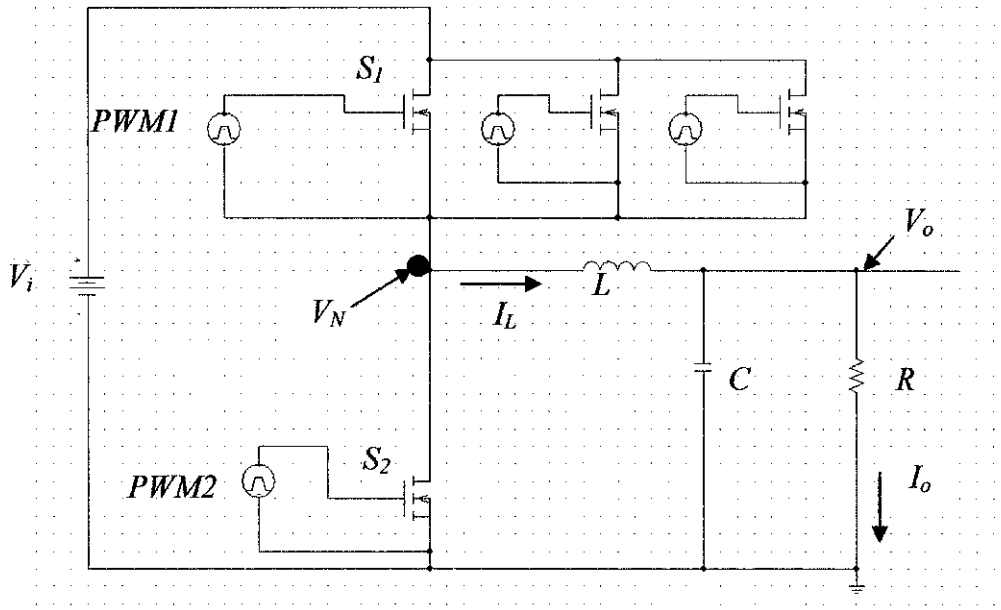


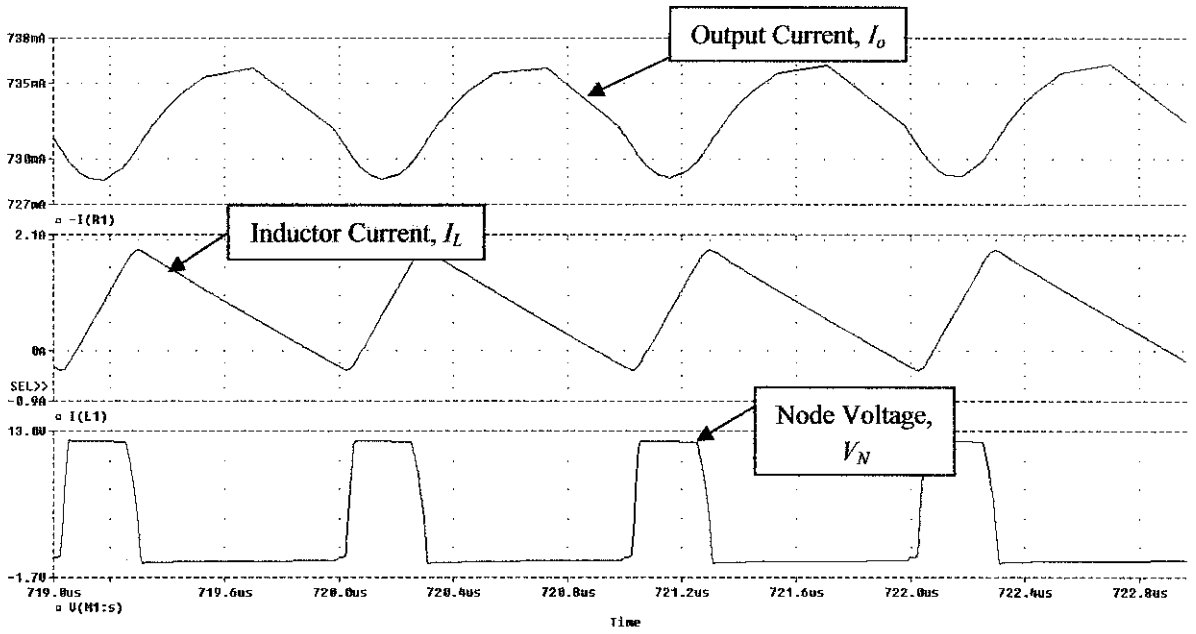
8) Configuration of (*S1*:2; *S2*:4)



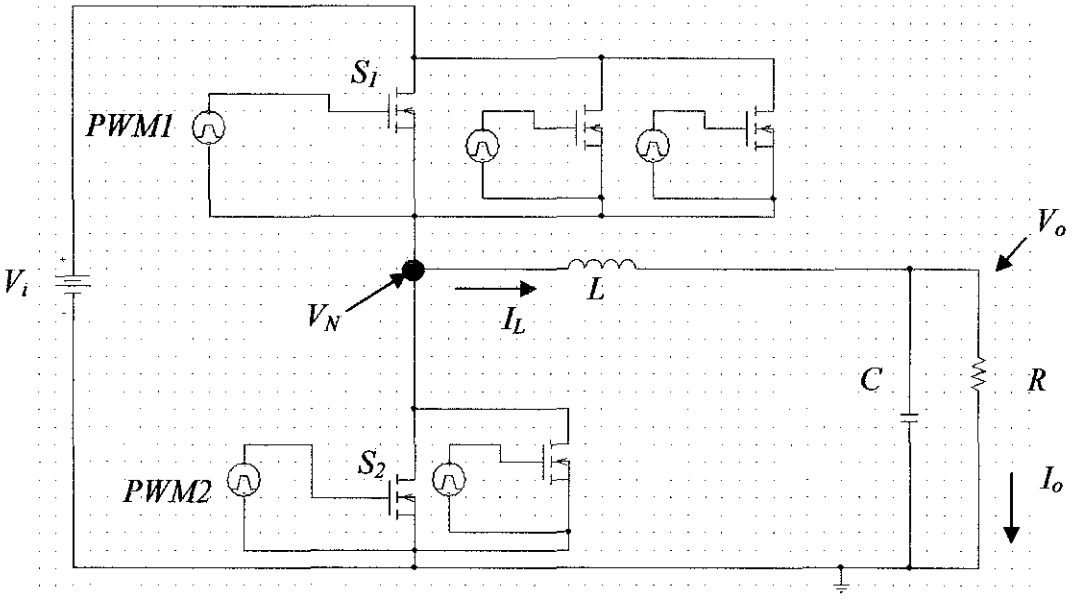


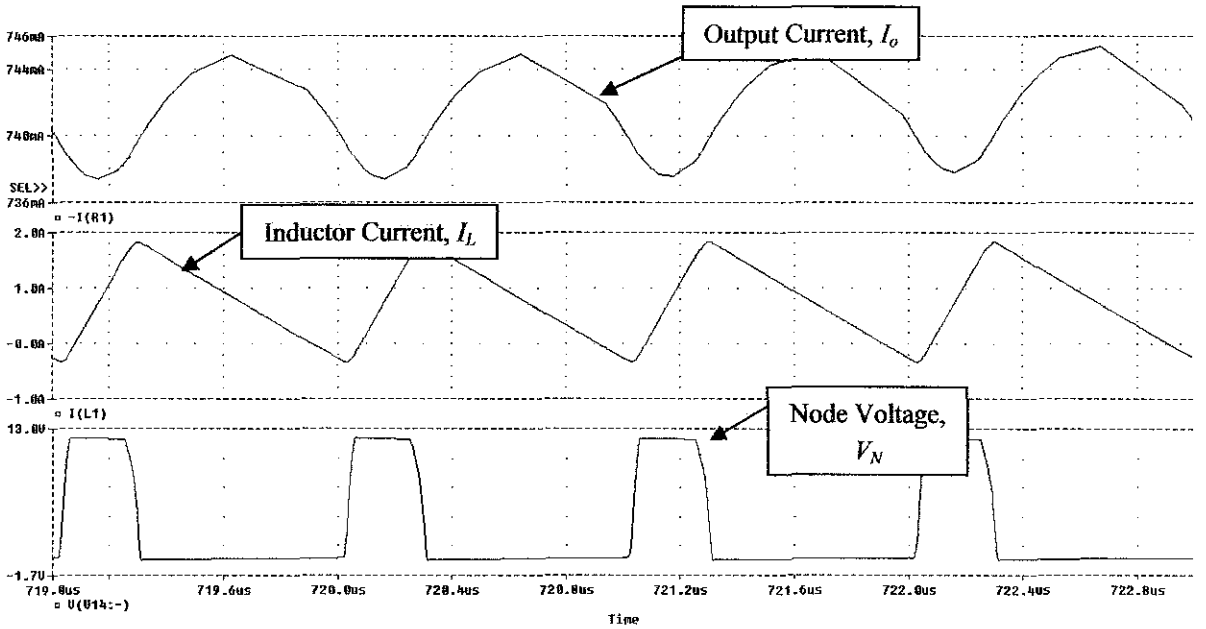
9) Configuration of (*S1*:3; *S2*:1)



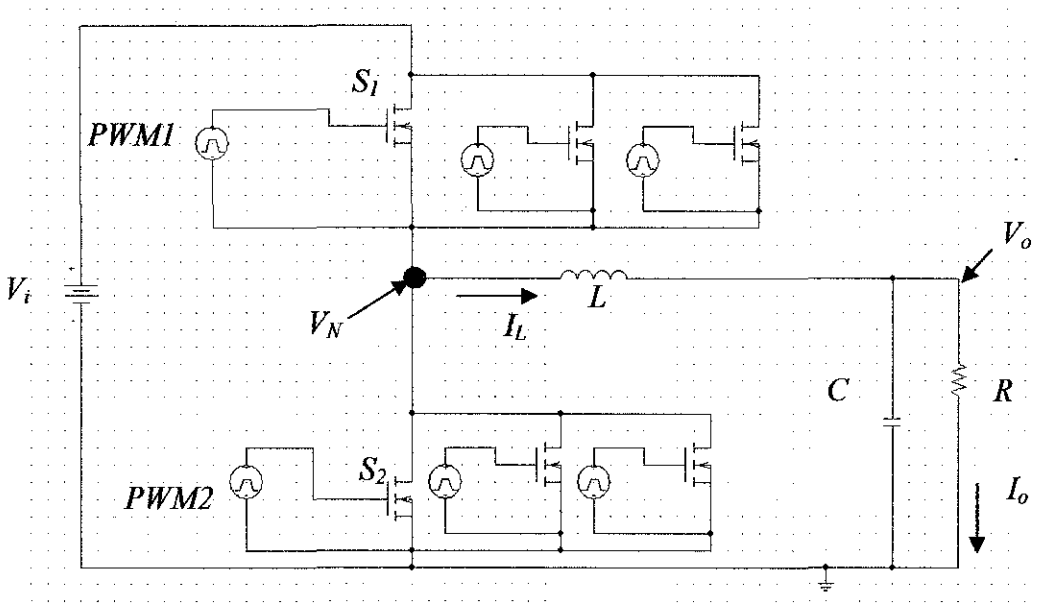


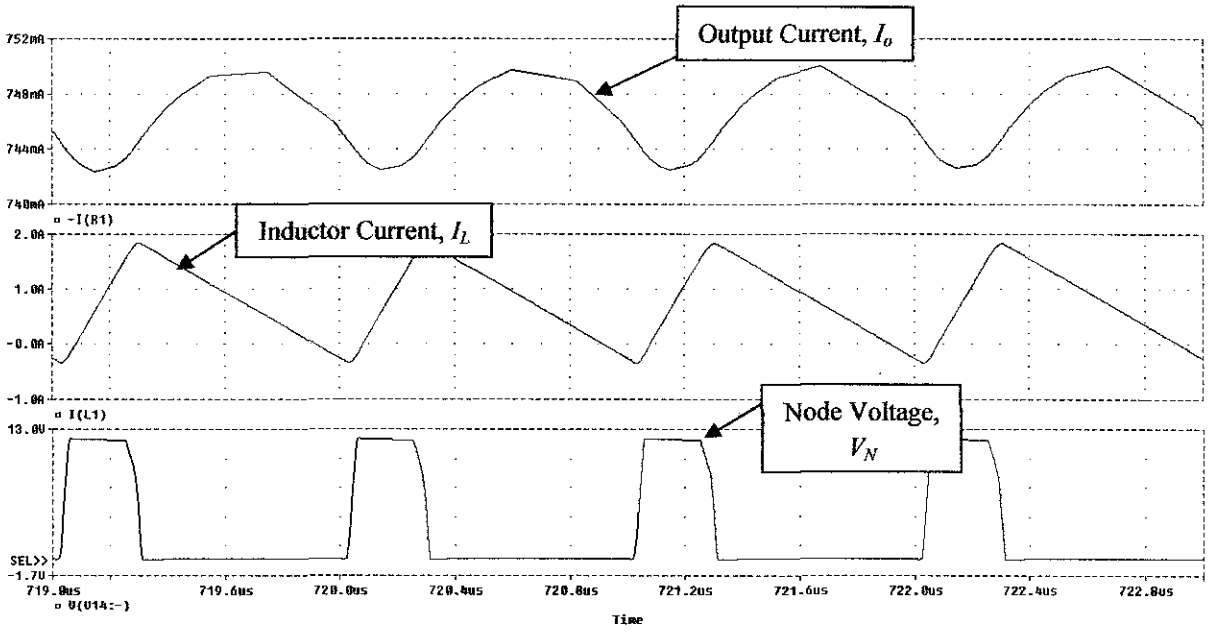
10) Configuration of (*S1*:3; *S2*:2)



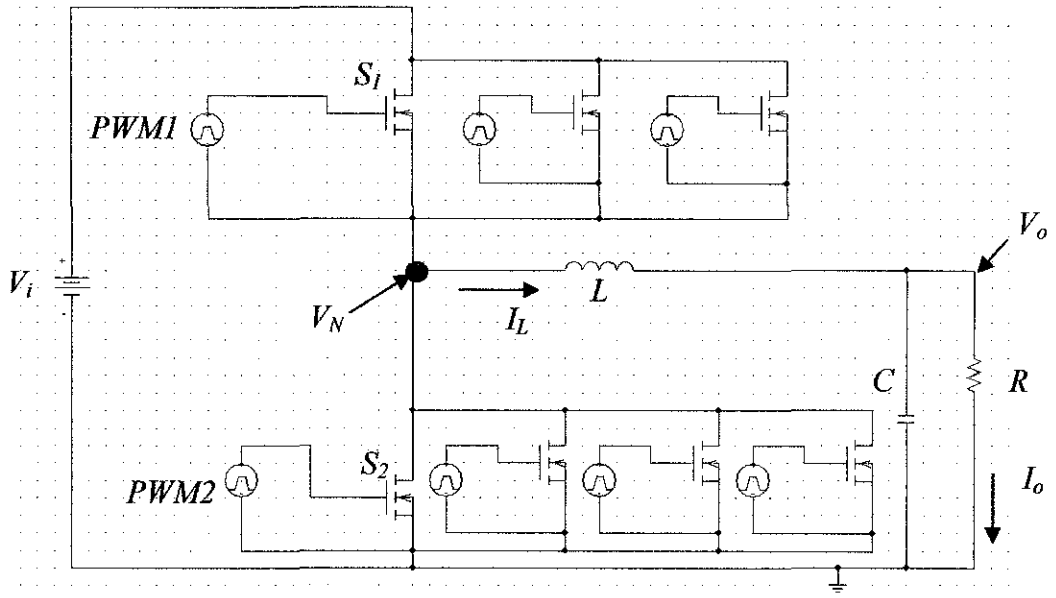


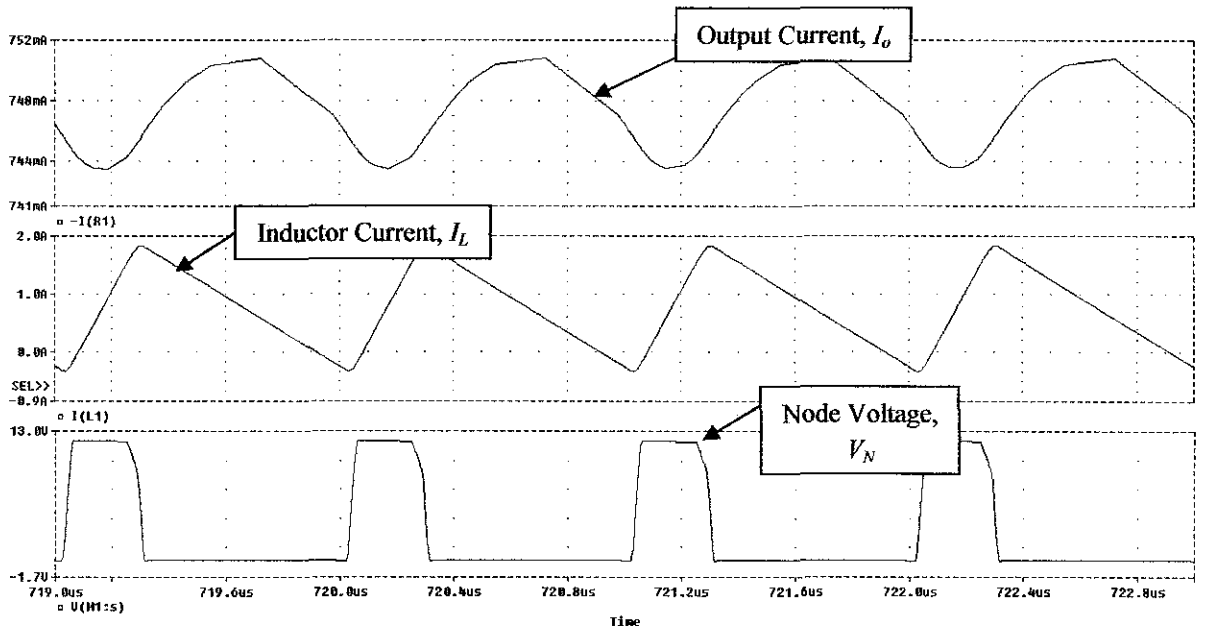
11) Configuration of (*S1*:3; *S2*:3)



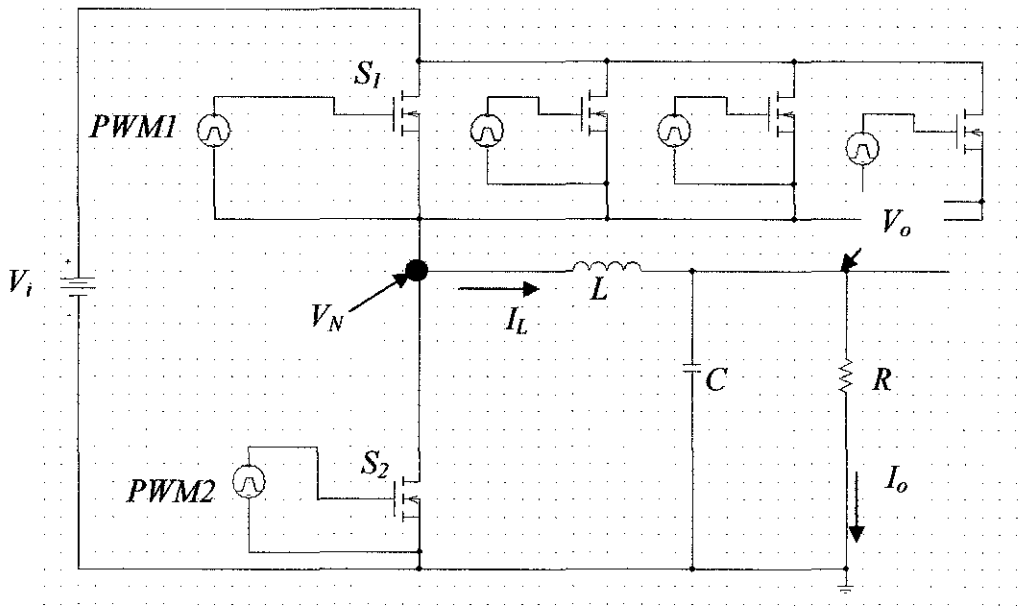


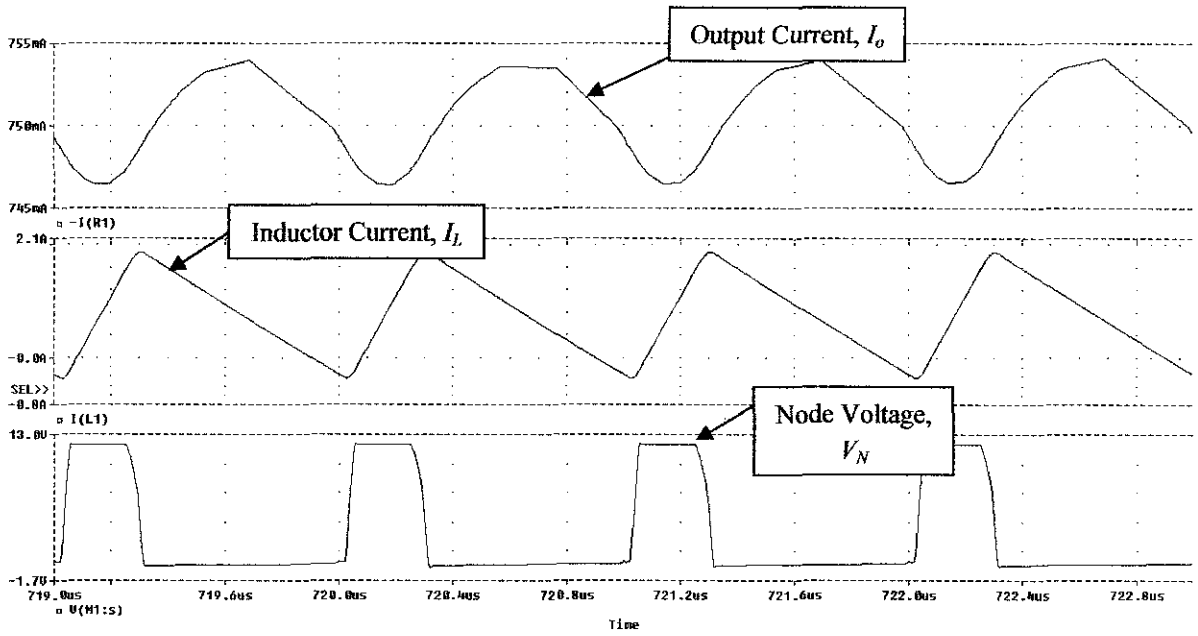
12) Configuration of (*S1*:3; *S2*:4)



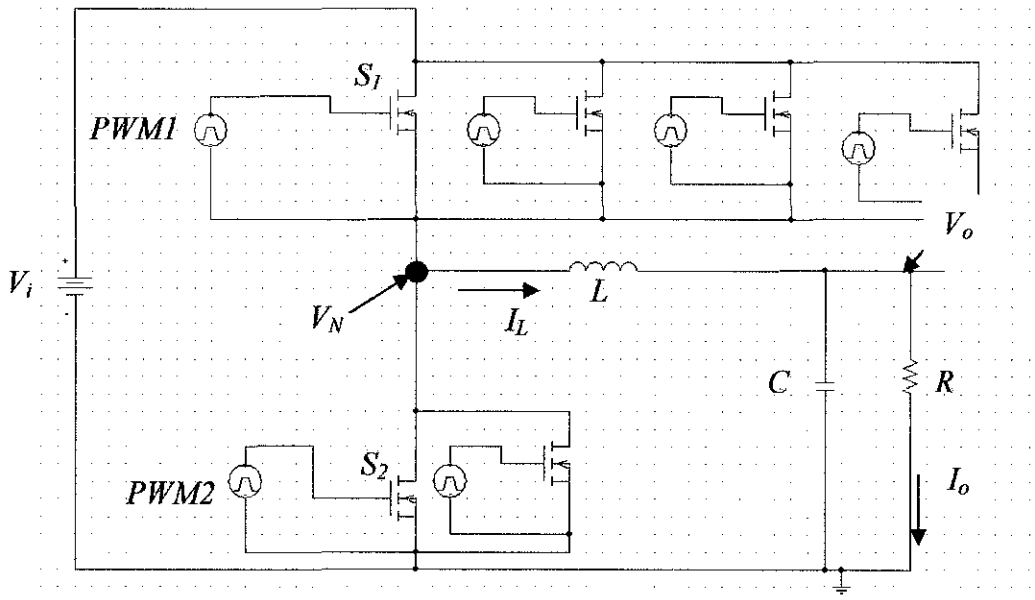


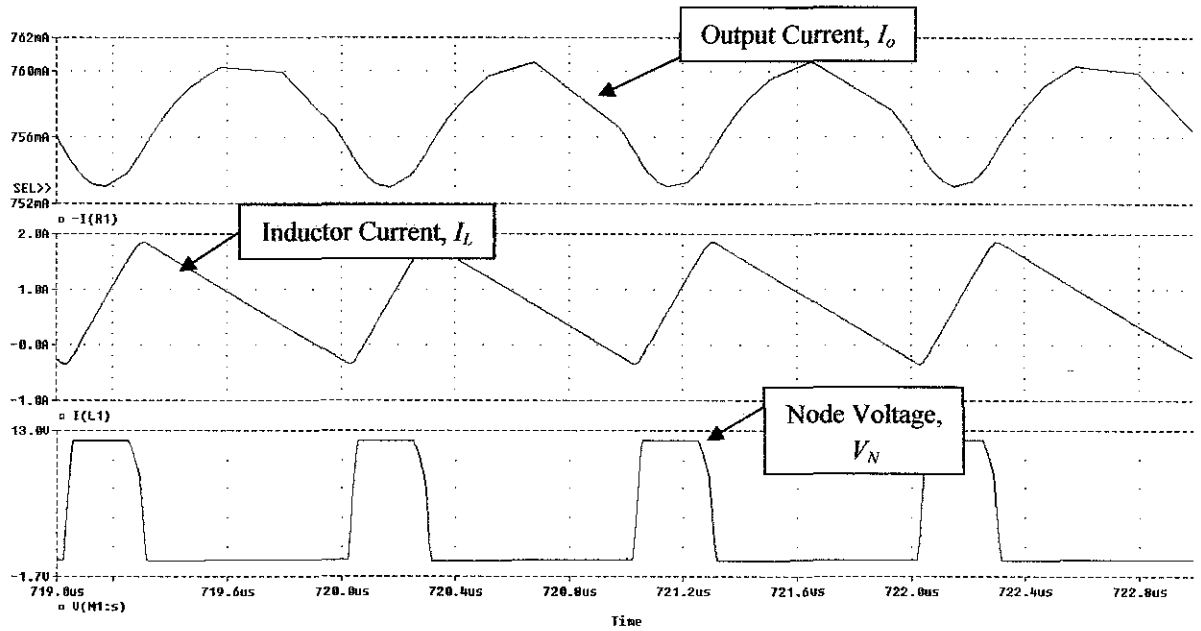
13) Configuration of (*S1*:4; *S2*:1)



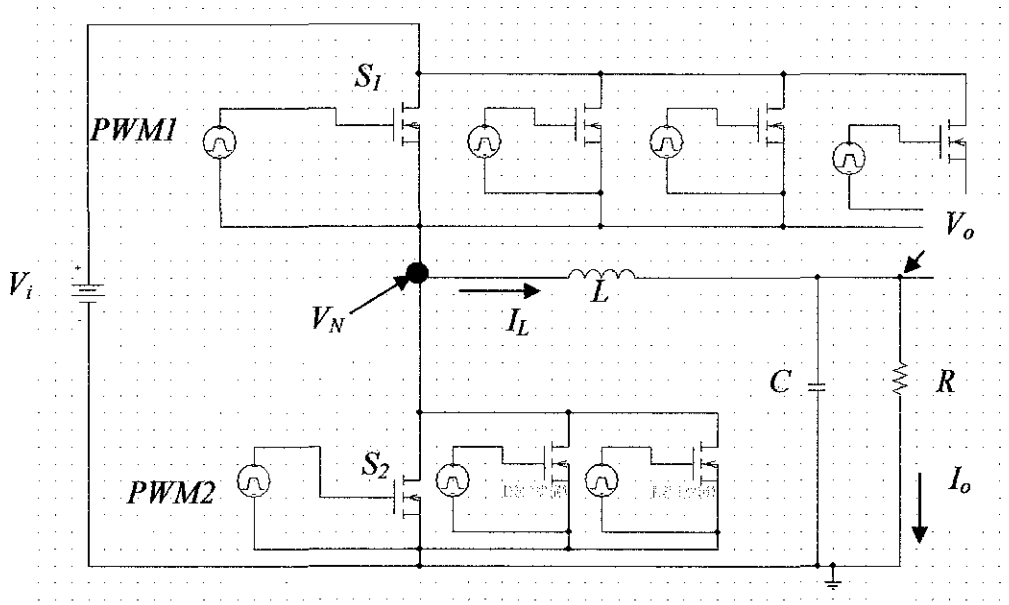


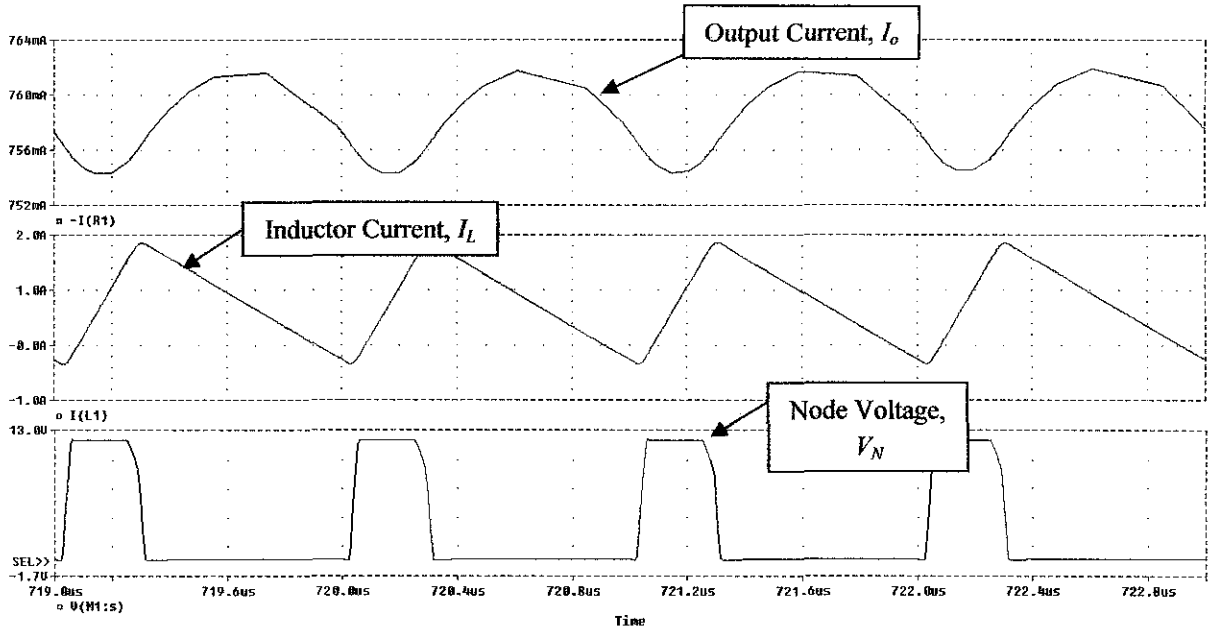
14) Configuration of (*S1*:4; *S2*:2)



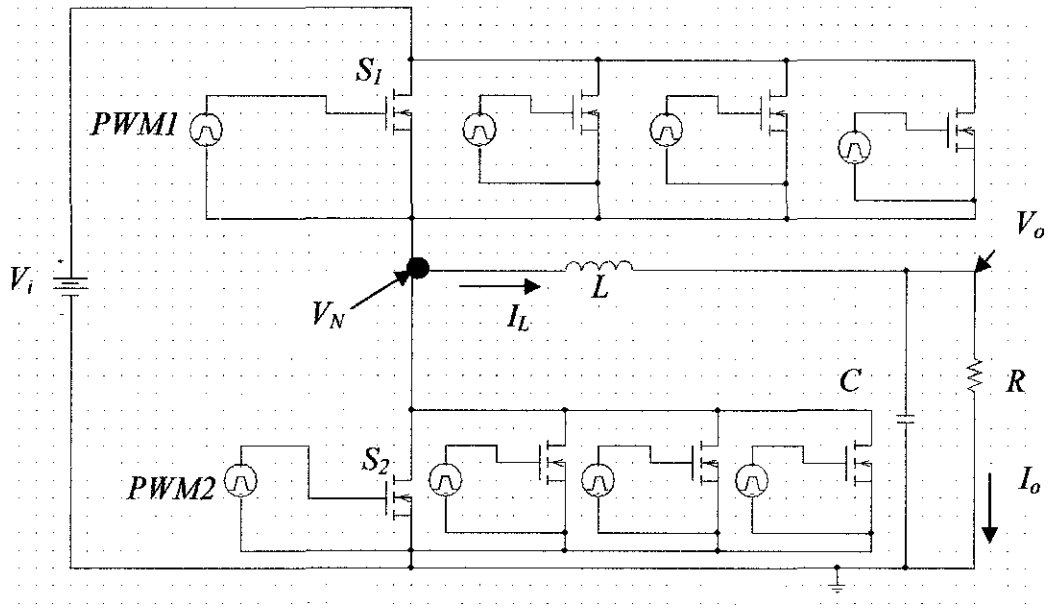


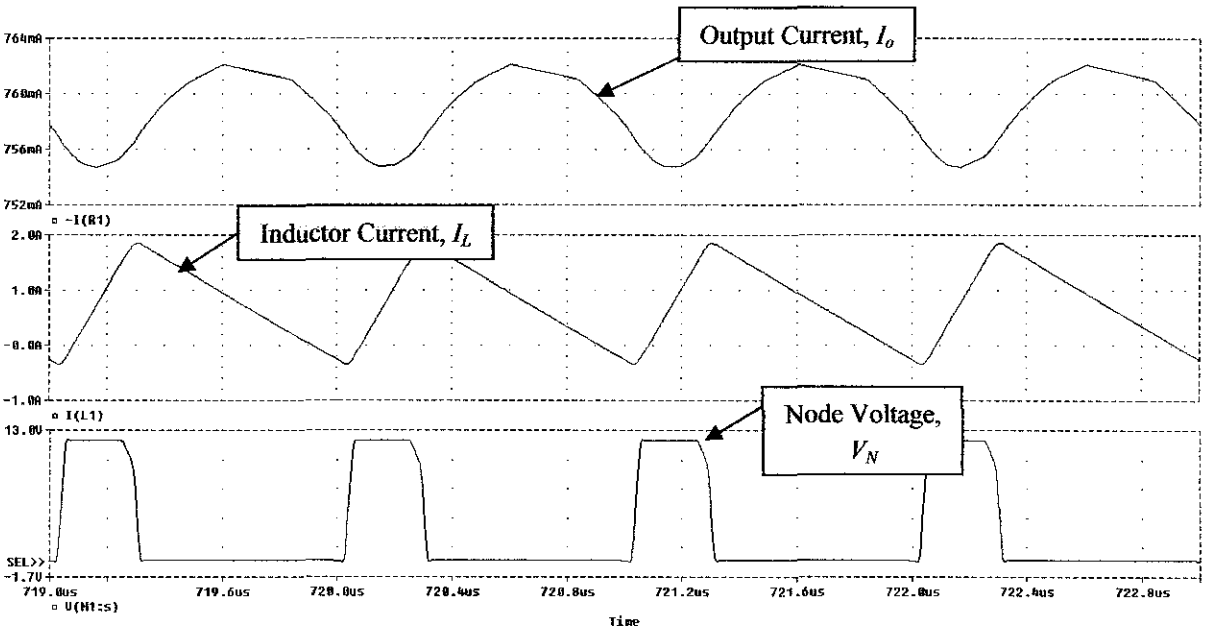
15) Configuration of (*S1*:4; *S2*:3)





16) Configuration of (*S1*:4; *S2*:4)

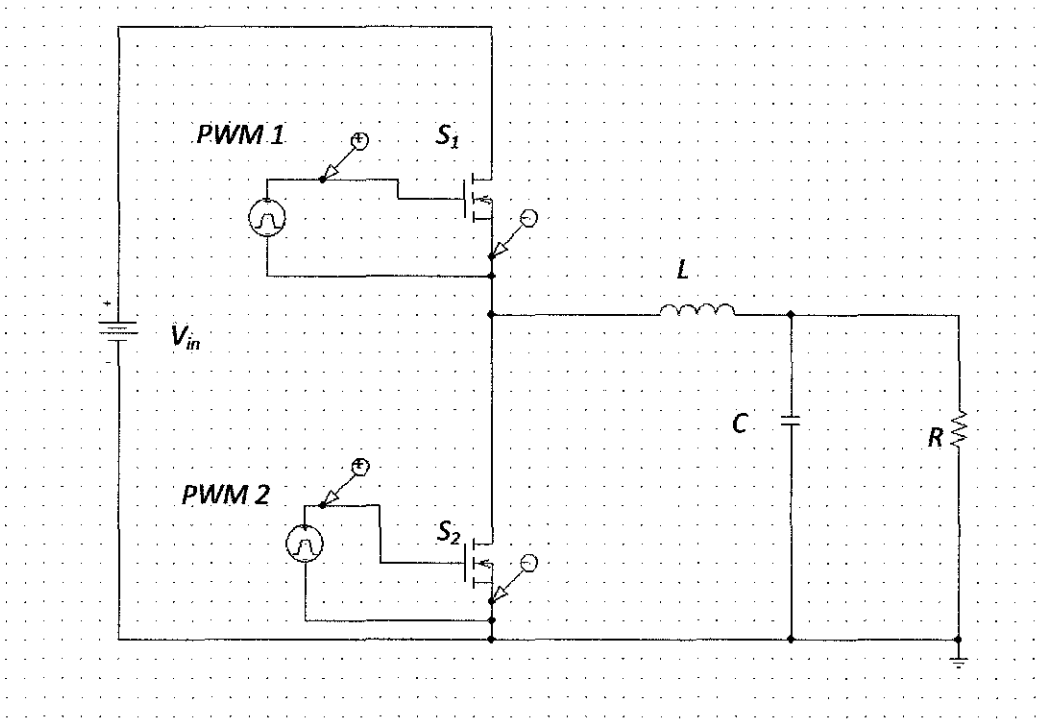




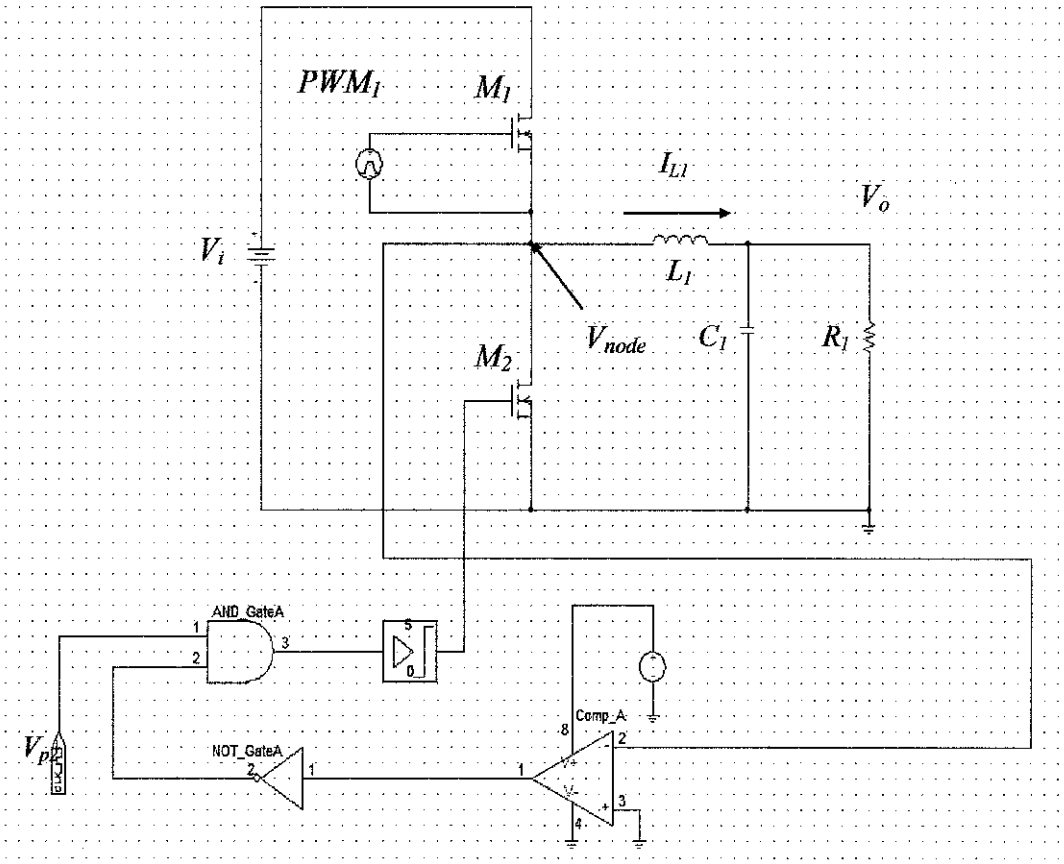
APPENDIX C

Circuit comparison.

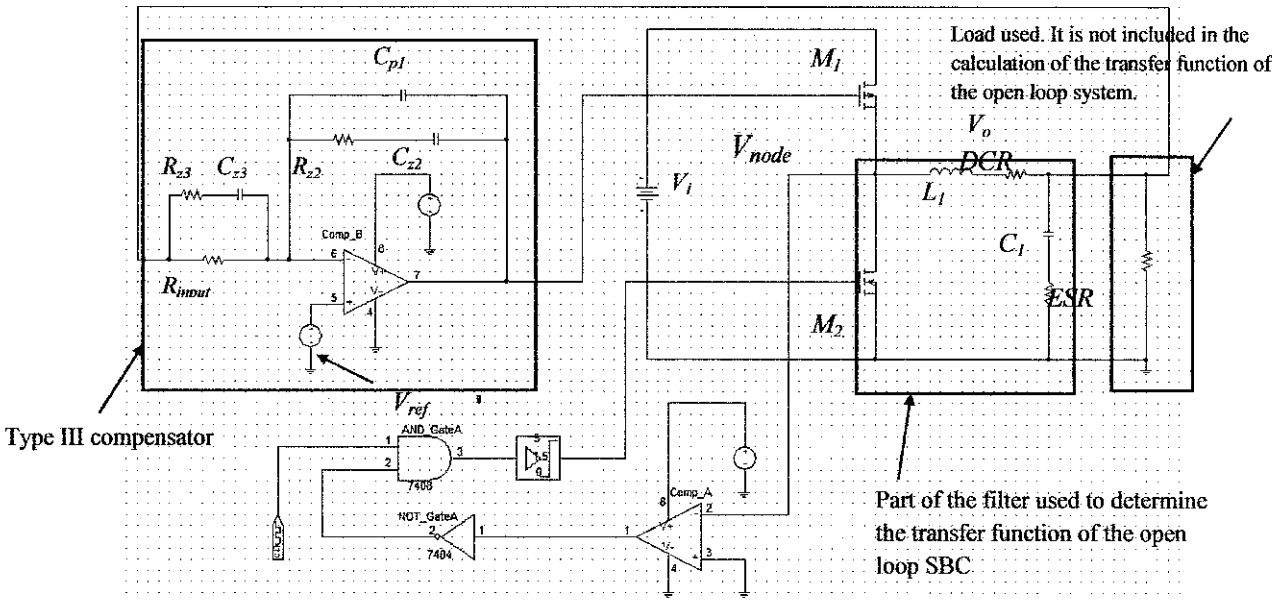
1) SRBC with CGD



2) SRBC with AGD



3) SRBC with compensator-AGD



4) SRBC with MPPT controller