Photon Induced Current Modulation in Nanoscale FETs simulated using ATHENA and ATLAS

By

Mohd Taufik Bin Ibrahim

Dissertation submitted in partial fulfillment of
the requirements for the
Bachelor of Engineering (Hons)
(Electrical and Electronics Engineering)

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CERTIFICATION OF APPROVAL

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A project dissertation submitted to the
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Approved by,

_____
(Dr. Zainal Arif Burhanuddin)
Project Supervisor

UNIVERSITI TEKNOLOGI PETRONAS

TRONOH, PERAK

December 2009

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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MOHD TAUFIK BIN IBRAHIM

ABSTRACT

Field Effect Transistor (FET) was based on the electric field to control the conductivity of channel for the carrier in semiconductor material. Nowadays, the trend to miniaturize the FET to nanoscale FET has been rapidly develops. In nanoscale FET it exhibits the quantum effect which is tunneling. Light illuminated on the surface of conductor can generate electron hole pairs thus; light penetrating into the Single Electron Transistor (SET) can give big influences to the electrical characteristics because the size of SET is very small. Addition of single charge will sensitively modulate the current flow at the top silicon channel. Thus it can be developed into single charge detector. In the conventional photodetector, it cannot detect a single photon, thus based on the sensitivity of SET it can be developed to be used as the single photon detector. In our work, we would like to see the effect of photon induced charge in the silicon-on-insulator SET. This effect will be simulated in the device simulation software, where the interface charge will act as the electron-hole pairs that were generated from light illumination. The findings shows the unexpected results, whereby the interface charge that introduce inside the Silicon-on-Insulator Field Effect Transistor (SOIFET) model do not give any changes to the energy band.

ACKNOWLEDGEMENTS

First and foremost I would like to pray to God for his mercy that I have completed this project. I would like to express my deepest appreciation to my final year project supervisor Dr. Zainal Arif Burhanuddin for valuable guidance and advice. He has become really helpful and has inspired me greatly to work in this project

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To my family and friends who always support and help me to do the research project. Thanks for the bless and the pray from my parents. Without helps of the particular that mentioned above, I would face many difficulties while doing this project.

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LIST OF ABBREVIATIONS

FET	Field Effect Transistor
SET	Single Electron Transistor
SOIFET	Silicon-on-Insulator Field Effect Transistor
LOCOS	Local Oxidation of Silicon

CHAPTER 1
INTRODUCTION

1.1 Background of Study

The Field Effect Transistor (FET) is a transistor whose behavior is controlled by an electrode called gate, capacitive coupled to the active region of the device. The gate is separated from this active semiconductor region called channel by an insulator or depletion region. The two other terminal of FET was source and drain that terminate the channel. The gate simply modifies the conductivity of the channel and thus the carrier flow between source and drain.

In the recent years, the trend to miniaturize the FET to nanoscale FET has been increasing rapidly and the number of nanoelectronics devices has been increasing and one of the nanoelectronics devices is the Single Electron Transistor (SET). The SET is working based on the coulomb blockade phenomena. Based on the Coulomb blockade phenomena, it tells that only one electron can tunnel from one island to another island at one a particular time. In this project, the SET simulation can be divided into two sections which are using C-Program that was written based on Coulomb Blockade Effect and Athena & Atlas simulation software. In the C-program simulation software, the simulated SET can be divided into two models which were single island SET and multiple island SET. These simulations model were to justify the characteristics and behavior of SET without any influence and effect of light penetration. The data were collected and it has been plotted to graph the I-V characteristics of the SET.

The single island SET is consists of drain and source terminal that coupled the island and between the island and the electrode terminal there are tunnel junction. The tunnel junction is consisting of tunnel resistance and tunnel capacitance that act as the barrier for the electron to flow.

Then, 2D-Silicon-on-Insulator Field Effect transistor (SOIFET) structure was modeled using the process simulation software called Athena. The meshes which were the simulation grid and the dimension of the substrate were defined at the early stage of the input file for Athena. After that, the conformal deposition take place as the structure was build layer by layer, and the suitable dopant was introduce at the particular silicon layer. The silicon oxide layer then has been growth to a certain thickness to act as the insulation layer. At the top of gate oxide, silicon channel with acceptor atom and aluminum electrode was deposited.

The SOIFET model then simulated in the device simulation software called Atlas. From this simulation, data were collected and the I-V characteristics and the potential profile of the SET were plotted. The I-V characteristics and potential profile then be analyze based on the parameter that has been varies in each simulation

Light that consist of photon posses the properties of wave and particle that contains a certain amount of energy. When light were illuminated at the surface of the semiconductor, photon will be penetrated into the structure and the energy of the photon could excite the electron in the valence band of acceptor atom to jump to the conduction band. When this situation occurs, the electron-hole pair will be generated inside the semiconductor. When the electron-hole pairs were generated inside the semiconductor, it will influence the current flow.

Using the SOIFET model that has been developed, the effect of photon induced charge will be introduced, and the SOIFET model will be simulated under this effect. In the simulation, photon induced charge effect is represented by interface charge in the SOIFET model.

1.2 Problem Statement

Current trend in miniaturize gate of MOSFET lead to nanoscale channel that has length and width. It has shown that external charges can sensitively effect the operation of these devices. Furthermore, at low temperature, the devices with top-Si channel can behave as single electron transistor which is extremely sensitive to external charge.

Due to the sensitivity of these nanoscale devices to charges, it may be possible to develop these devices into a charge detector. In this work, the sensitivity of the devices to photon induced charges will be investigated. The should show how external charges effect the device current of thin SOIFET and the suitability of the devices as a photon detector

1.3 Objectives and Scope of Study

The objective of this project consists of 3 main parts:

1. Model the I-V characteristics of thin SOIFET using the C program that written based on the orthodox theory of Coulomb blockade effect.
2. To model the thin SOIFET using the Athena software and simulate the I-V characteristics using the Atlas software.
3. To introduce and simulate the effect of light by injecting electron-hole pair in the SOIFET model and investigate this effect to the performance and characteristics of the SET.

The scope of this project is confined to low operating temperature at 0K and the room temperature at 300K of the thin SOIFET. At 0K, the thin SOIFET is simulated based on Orthodox theory of Coulomb Blockade effect and at 300K, it is simulated using the semiconductor theory used in Athena and Atlas

CHAPTER 2
LITERATURE REVIEW

2.1 Single Electron Transistor (SET)

The structure of the single electron transistor (SET) is showed in the Figure 1. The SET structure consists of an island which is the conductive material, the electrode called source and drain and the gate terminal which is coupled to the island through the dielectric. Between the island and the drain/source electrode there is tunnel junction that consist of the tunnel capacitance and tunnel resistance. The tunnel junction is the insulating region that isolates the island from the drain and source. The tunnel junction that acts as leaky capacitor and it is a combination of tunnel resistance and tunnel capacitance [1][2][4]. The tunnel resistance is the special resistance that allows electrons to cross the tunnel junction and the value of the tunnel resistance must be large enough to prevent the electrons from tunneling at any time, but the value of the tunnel resistance must be finite and not too large, so that tunneling can take place under certain bias condition [2][4]. Between the gate terminal and the island, there is gate capacitance.

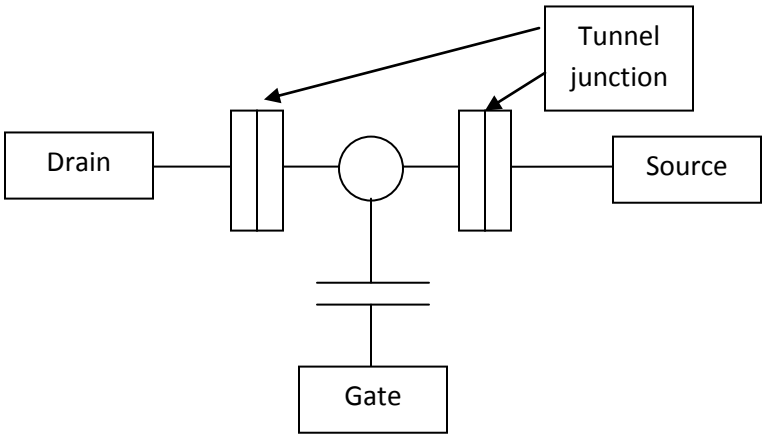

Figure 1 : structure of the Single Electron Transistor (SET)

In the SET, the Coulomb blockade phenomena occur that enable the SET to act as a transistor. The coulomb blockade phenomena tell that only one electron can move from one island to another island at one time [6]. The island is the conductive material and the electron need to tunnel through the tunnel junction from the source to the island, then from the island to the drain. In order for the electron to tunnel through the tunnel junction it require certain amount of energy to overcome the electrostatics energy of the island. Therefore the external applied bias need to provide the enough energy for the electron to enable the tunneling process.

To understand further about this phenomenon, it is good to examine the energy band diagram of this structure [4]. Consider that the junction with identical capacitance. The Fermi level of the source and drain is lower from the energy band gap level of the coulomb island as shown in Figure 2. Therefore, it is not possible for the electron to tunnel from source to the island and the energy gap size is $e^2/2c$.

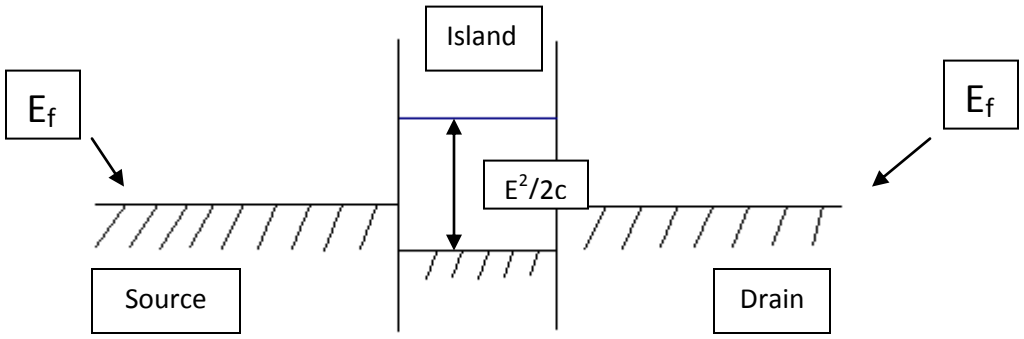

Figure 2: the energy band gap for the SET

When there is bias applied to the SET, it will change the energy band diagram of the SET structure. As showed in figure 3, the Fermi energy level of the source is increases more than the energy band gap level of the island and it will allow an electron to tunnel into the island.

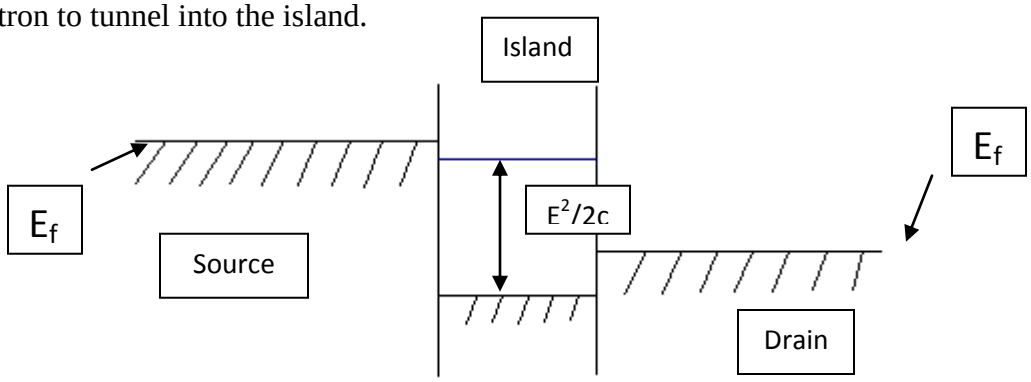

Figure 3: the energy band diagram of the SET when we apply biased

The I-V characteristics of the SET devices are based on the theory is showed in Figure 4 and the SET device is the single island.

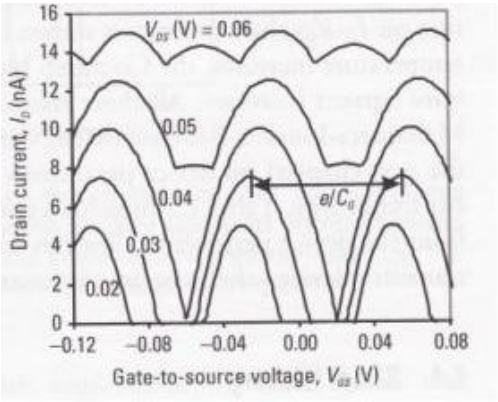

Figure 4: the Id-Vgs characteristics of the single island SET [1]

Due to the technological constraint to build the single island SET, an alternative approach is to build the multiple island of the SET. In the multiple island of the SET, the drain and source is coupled by several island instead of one. The configuration of the multiple island of the SET is showed in the Figure 5

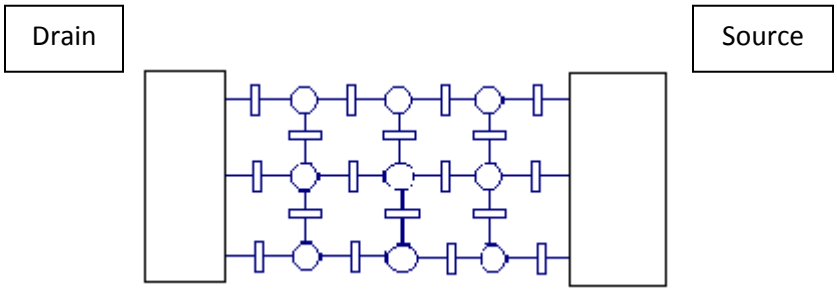

Figure 5: the SET structure for the multiple islands (3 by 3 islands)

For the multiple island SET, the I_d-V_g characteristics graph is slightly different with the single island SET. As shown from the Figure 6 we can see that the I_d increasing as we keep increasing the V_g. This is due to the multiple of island, so many electrons moving from source to drain by tunneling from one island to another island.

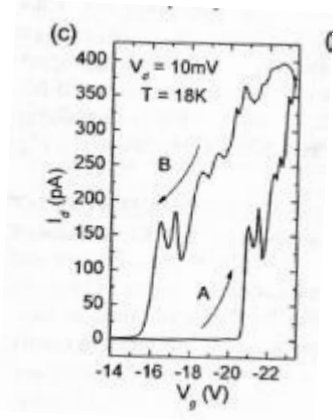

Figure 6: the Id-Vgs characteristics for the multiple islands SET [3]

2.2 Sensitivity to External Charge

Due to the high sensitivity of the SET, any different and changes of charge, would affect the performance of the SET. One of the factors that could generate charges near to the SET channel is the light. When light is illuminated on the semiconductor, electron-hole pair will be generated and the generated charge would influence the performance of this SET.

Light posses 2 characteristics which is waves and particles. Light is consist of photon and the photon is consist of energy $E=hv$ where h is the Planck constant while v is the photon frequency. The photon travel at the speed of light in vacuum and having zero rest mass.

In the SET model, the SET channel thickness is about 5nm, this channel is made of silicon that has been doped with impurity. When the light passes through it, only a part of the light will be absorb by the silicon and others will be transmitted. The photon that is absorbed will be converted into free electrons. The equation of the light absorption is given by

$$I(x) = I_o \exp(-\alpha x)$$

I_o= incident light intensity

$I(x)$ = intensity at a distance x into the semiconductor

α = absorption coefficient

The photon only been absorbed if the energy contain in it can overcome the energy band gap between valence band and conduction band of the semiconductor. The absorption coefficient of the photon is depending on the material and the wavelength [10].

The penetration of light into the SET is determined by the skin depth of the silicon. Based on the table of the silicon at 300K the relationship between the absorption coefficient and the skin depth is:

$$\text{Skin depth} = 1/\alpha$$

As the wavelength is higher, the absorption coefficient will decrease and the skin depth will increase [11]. Skin depth is the distance where the magnitude of the penetrate wave become e^{-1} or approximately about 37% of the magnitude.

Several works has been done to investigate the ionization in nanoscale FET's, one of these is in the single-hole-tunneling (SHT) transistor that fabricated on silicon-on–insulator (SOI) wafer. The ionization occurred in a thin p-Si epilayer during the formation of depletion region give an effect to the charge flowing at the top silicon layer. The device structure for SHT transistor was prepared by wafer bonding technique and the wafer consist of p-Si layer doped with boron acceptor concentration of 1.5×10^{16} / cm^3, and p^+-Si layer doped with Boron acceptor concentration of $3.0 \times 10^{18}/cm^3$ [3].

Furthermore, ultra narrow channel MOSFETs and point-contact MOSFETs are two types of silicon nanoscale devices that were fabricated shows the quantum confinement effect and single electron charging effect [13].

The fabrication of multidot Si channel for the SET devices can be formed using the nanometer scale local oxidation of Si (nano-LOCOS) that can control the size of Si dots. The ambipolar characteristics has been exhibit by this devices due to the schottky contact between the drain, source and Si channel, and it's become the important characteristics to this design [14].

CHAPTER 3

METHODOLOGY

3.1 Procedure Identification

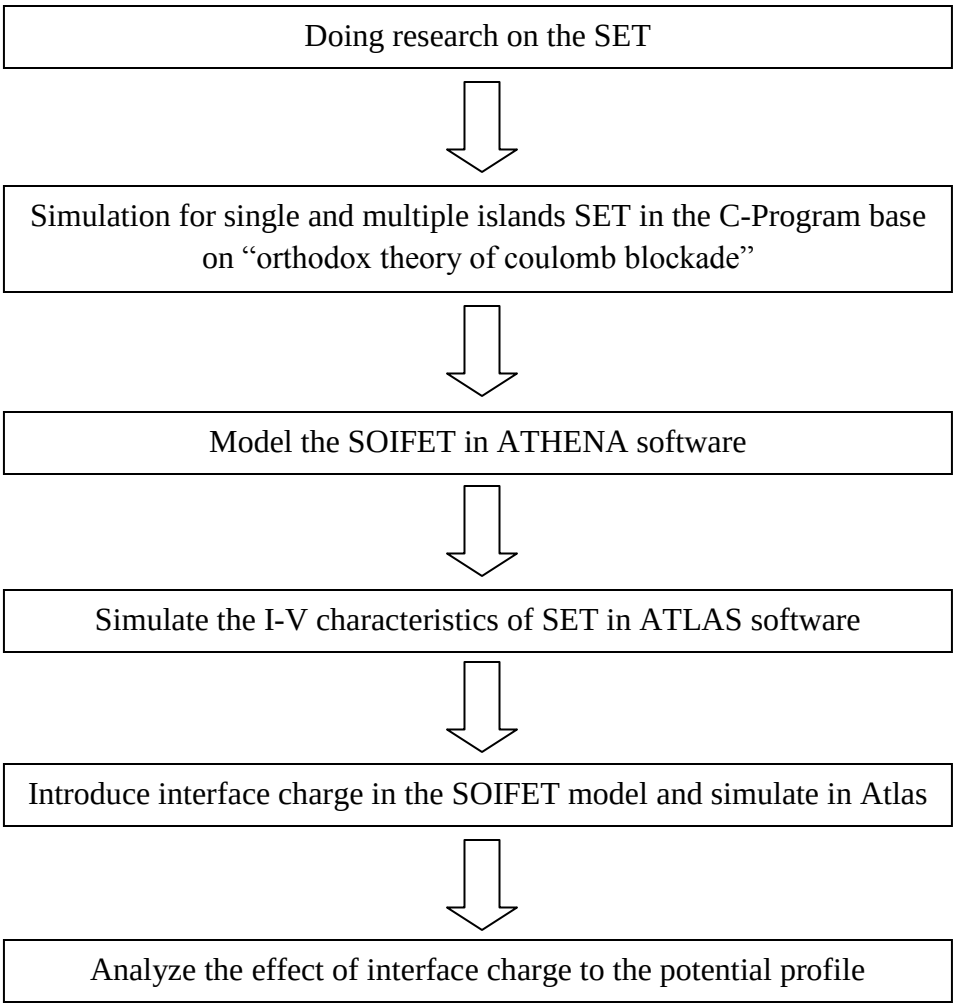

Figure 7: The flow chart of the project work

The flow chart of this project work was shown in Figure 7, where the project begun with a research on the SET. The resource for this research comes from books, journal, technical papers, proceedings and internet and main aspect of this research covers the structure of the SET and the I-V characteristics. Then the works continues with the simulation of the SET in C-Program that written based on the Coulomb Blockade effect. Then, SOIFET structure was model in Athena process simulation software by using layer by layer deposition. After that, the SOIFET model was simulated in Atlas to generate the I-V characteristics. The procedure then continues by introducing the interface charge that will act as the effect of photon induced charge into the SOIFET model. The SOIFET model that has been introduced with interface charge will then be simulated with different quantity of the interface charge density. The results from this simulation were gathered and further analyses were done in the next chapter.

3.2 Project Activities

3.2.1 C-Program simulation

The main research method used in this project is by using software simulation. The simulation started with the C program that written based on the orthodox theory of Coulomb blockade effect. This C-Program was run in the command window. By using this simulation program, the behavior and I-V characteristics of the SET were observed. This simulation program use text file for the input and it can be referred at the appendix section of this report. In the input file, there are certain values that need to be set.

- Junction capacitance and resistance
- Gate capacitance
- Drain voltage and gate voltage (V_d and V_g)
- Island node number and the initial charge at each island

The simulation were started with single island SET structure and the temperature were set to 0.1mK. Tunnel capacitance and tunnel resistance were fix at 2aF and 1kΩ, while the gate capacitance was fixed at 1aF. For I_d vs. V_d simulation, the value for gate voltage was set at 10mV the drain voltage sweep from -300mV to +300mV. For I_d vs. V_g simulation, the drain voltage was fixed at 10mV and gate voltage sweep from -300mV to +300mV. After the simulation has finished, it will generate output file which contain the data needed to observe the I-V characteristics. This data were collected and stability chart of the single island SET was plotted.

Then, the simulation was proceed with multiple island of SET and the multiple islands was set to be 5 x 5 islands. All of the islands and tunnel junctions need to be assign with a number and all of the junction capacitance, junction resistance and gate capacitance is set to 2aF, 1kΩ and 1aF and the voltage sweep for this simulation was from 0mV to 200mV. The input file for this simulation can be referred at the appendix section.

3.2.2 Athena Simulation

The SOIFET structure then been modeled in Athena, this structure will be used in Atlas simulation to generate the I-V curve. In the Atlas simulation, input for the SET were given and the parameter were varied, then the graph of I-V curve and potential profile can be plotted from the simulation results.

The SOIFET was being model in the ATHENA software and the specifications of the model were:

- Silicon thickness 5nm
- Aluminum thickness 100nm
- SiO2 thickness 45nm
- P-Si thickness 1000nm
- P^+ -Si thickness 40um

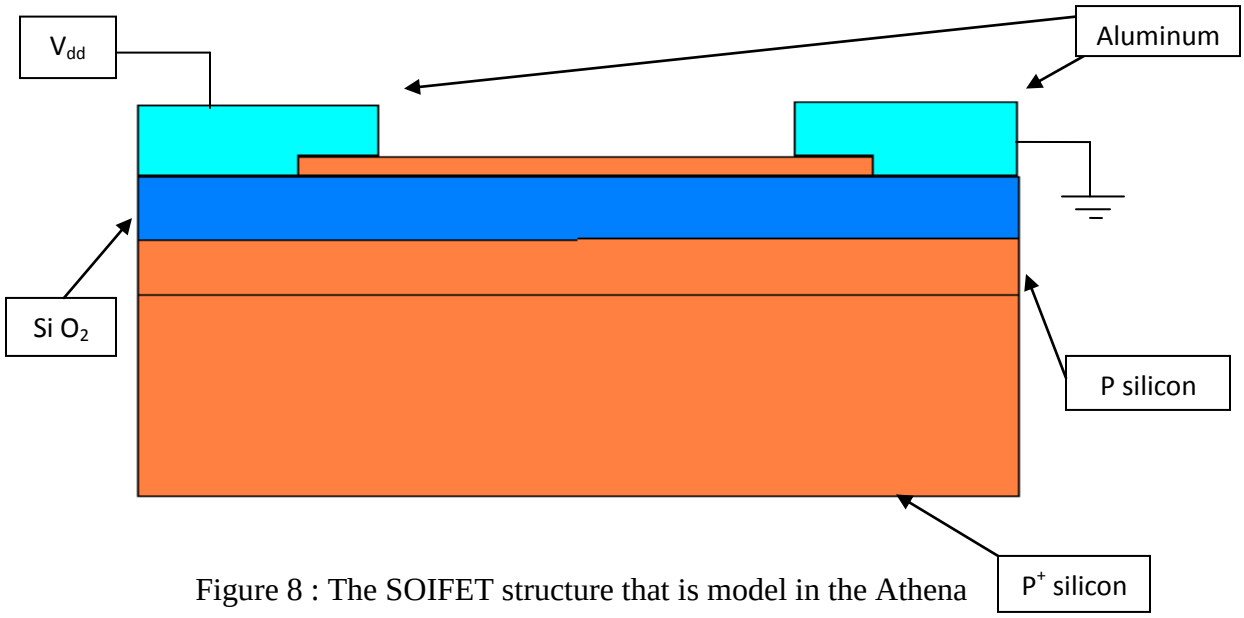

Figure 8 : The SOIFET structure that is model in the Athena

The design process is start by defining the mesh of the substrate. The mesh is the rectangular grid and the number of the nodes in the grid has direct influence in simulation accuracy and time. The mesh define in the simulation can be referred at the appendix site. A finer grid should exist in those areas of the simulation structure where photon induced charge will occur.

During mesh initialization process, the substrate of the structure was defined with the acceptor atom dopant. The dopant for the substrate was boron and doping concentration was $3.0x10^{18}$ that will make the substrate P^+-Si and it will also act as the backgate to the SET. Then another silicon layer with the impurity of boron atoms and doping concentration of $1.5x10^{16}$ was deposited.

Then, silicon dioxide (SiO_2) layer was grown on top of the P-Si layer and it has been done by diffusion process. In diffusion process, there were certain parameter that was needed to be set and the parameters were:

- Time = 11.5626 minute
- Temperature = 1040.63 ^{0}C
- Gas pressure = 1.57672 atm
- HCL = 5.25572 %.

These parameter values were result after the optimizer process was performed. After the diffusion process has been performed, the thickness of the silicon dioxide can be measured by using the extract process. In the extract window, "material thickness" was selected for the extract field and the material field is set to "Silicon Dioxide", the extract location was "X" and the value for the location was 0.05. After that, the program will be run and there was the result for the thickness of SiO_2 that have been fabricated. From the result that was generated, some modification needs to be done to the SiO_2 thickness, and this can be done by using the optimizer. The optimizer will automatically modify the diffusion parameter, so that the SiO_2 thickness was 45nm.

After SiO_2 has been grown with the thickness of 45 nm, the top silicon layer was deposited with the thickness of 5nm and doping concentration of $1.5x10^{16}$ of boron atom on top of the SiO_2 layer. The top silicon layer is the silicon channel for this SET and it will be coupled by two electrodes. When the silicon layer has been introduced, a portion of the silicon layer at the left side of the model will be etched. The objective of this etching process is to provide a place for aluminum deposition. Aluminum is the drain and source terminal of this SOIFET model. The aluminum was also introduced by deposition process. The source code for the Athena simulation can be referred to appendix site.

3.2.3 Atlas simulation

After the SOIFET structure has been model electrical characteristics will be simulated in Atlas simulation software. In the Atlas simulation software, the I-V characteristics data were generated. For the atlas simulation, it started by creating the input deck file which taken from the SOIFET model that have been made in the Athena. Then, the suitable model parameter for the simulation were specify, Lombardi model (CVT) was used for the simulator. Next, the contact characteristics of the electrode need to be specified because an electrode that was in contact with semiconductor material will be assume to be ohmic[15]. Schottky contact needs to be made between the silicon channel and electrode to simulate the ambipolar characteristics of the SET [14]. The interface properties used also need to be specified, in this case the default value of $3x10^{10}$ for interface charge density. After that, the Gummel and Newton numerical method used for calculating the solutions to semiconductor problems were selected.

3.2.3.1 Simulation without Photon Induced charge Effect

The SOIFET will be simulated without any photon induced charge effect. The simulations of I_d vs. V_g were sweep from -5V to +5V with the value of drain voltage was from -5mV and it is repeated with an increment of 1mV. While for I_d vs. V_d, it sweep from -5V to +5V with the value of gate voltage was from -5V and it is repeated with an increment of 1V for each simulation.

3.2.3.2 Simulation with Photon Induced Charge Effect

Light will illuminated on the surface of SOIFET will be pass through the silicon channel and the SiO_2 layer and it will penetrate to the P-silicon layer and substrate. As the results of this penetration, photon will excite the valence electron of the atom to move to the conduction band and electron-hole pair will be generated.

To simulate the effect of photon induced charge, interface charge will be introduced to act as the electron–hole pairs generated inside the SOIFET. This interface charge density was varied from -1E10 to -3E10 and the changes in potential profile will be observed. From this variation of the interface charge it can be predicted that the performance of SOIFET would also been influence. Then SOIFET will be simulated under this effect and the data for electrical characteristic and potential profile were generated.

3.3 Tools and Equipment Required

In this project, there were three simulation software used that were C-Program, Athena and Atlas. C-Program was written based on the "orthodox theory of Coulomb blockade" while the Athena and Atlas was simulation software manufacture by Silvaco.

CHAPTER 4
RESULTS AND DISCUSSION

4.1 Simulation Using C-Program

The simulation of the SET model begin with the simulation of the C-Program simulation file, the single island SET model has been simulated at the low temperature and the characteristics graph of the single island SET was generated. Figure 9 shows the graph for I_d vs. V_g for the single island SET. From Figure 9 it shows that at a certain value of V_g there is no current flow, this is due to the Coulomb Blockade effect. While in the region where there is current flowing, it shows that electron was tunneling from the drain to the source

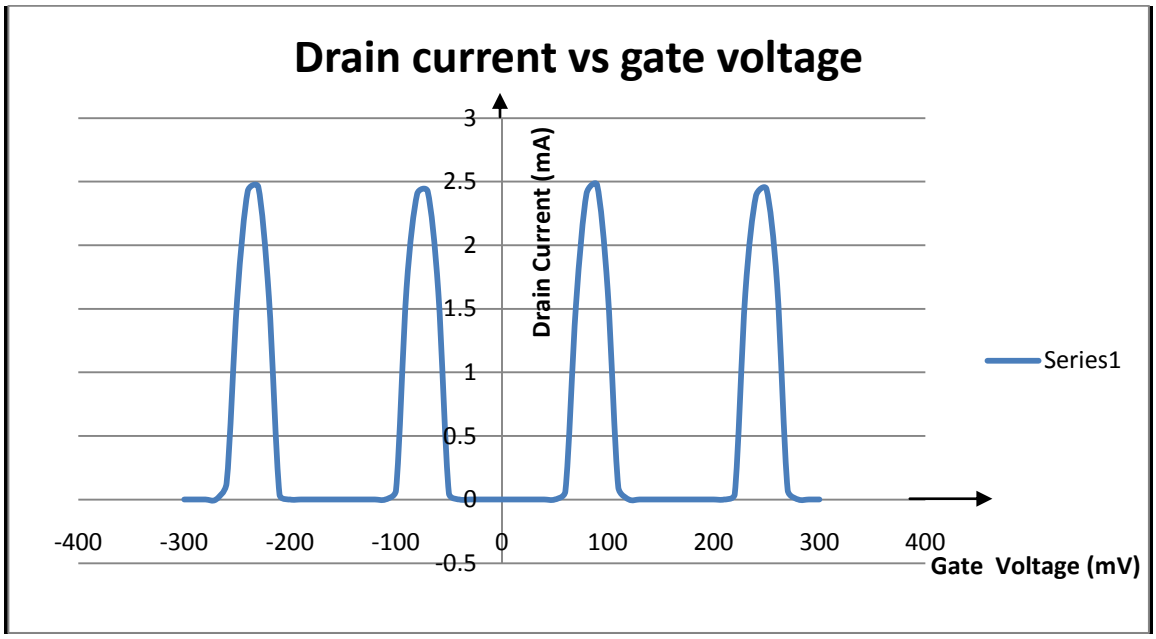

Figure 9 : Graph of I_d vs. V_g for single island SET

While, for Figure 10 it shows the graph of I_d vs. V_d for single island SET. At the 0nA drain current, there is no electron tunneling the region is called Coulomb Blockade region. As the drain voltage increases, the drain current also increases in a steplike pattern because the number of electron tunneling inside the SET was increasing.

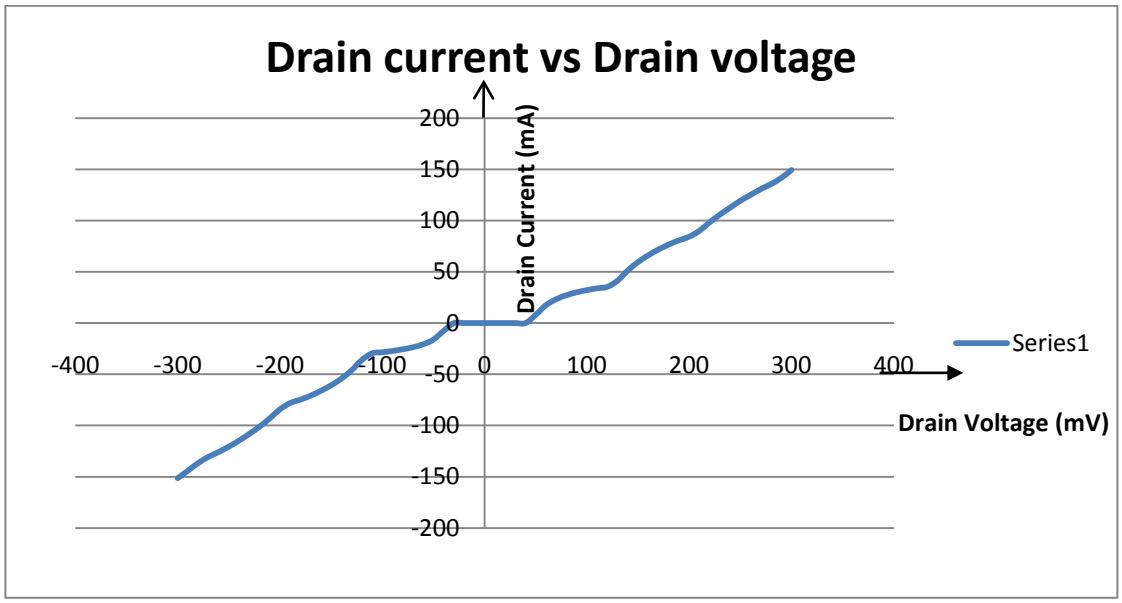

Figure 10 : Graph of I_d vs. V_d for single island SET

The stability chart for the single island SET is showed in the Figure11. In this stability chart it shows the region of drain current was 0nA and this was the Coulomb blockade region. Coulomb Blockade prevent the electron from tunneling in this region

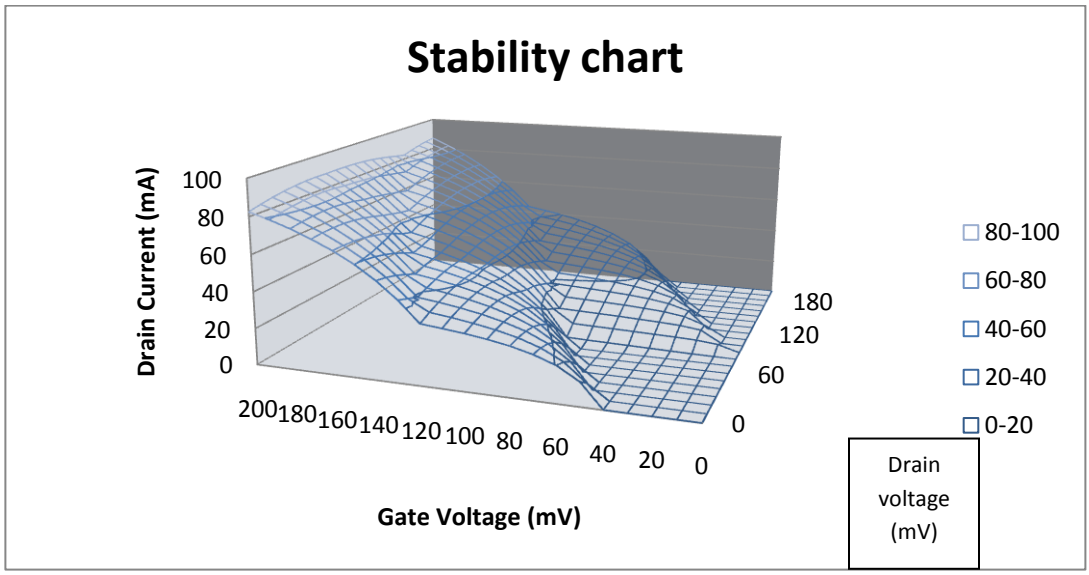

Figure 11 : Stability chart for single island SET

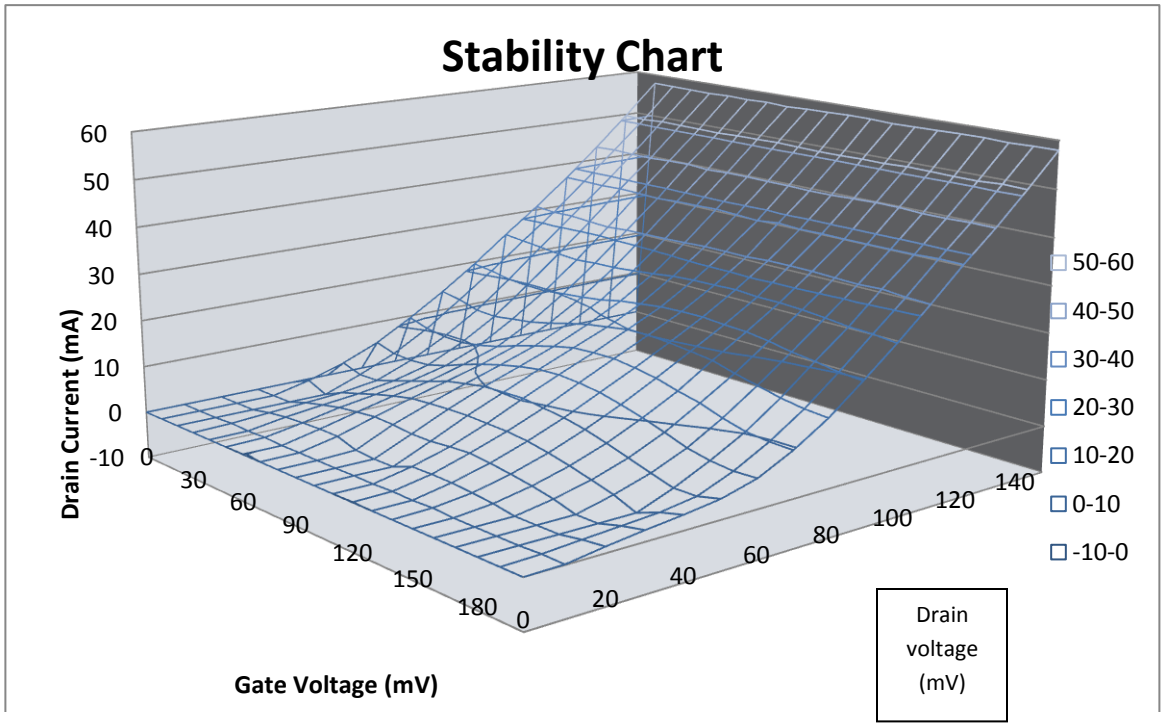

Figure 12 : Stability chart for multiple island SET

Then the 5x5 multiple islands of SET models were also simulated in the C-Program simulation file to generate the data for the drain current at each gate voltage and drain voltage. Figure 12 shows the stability chart for the multiples island of SET that has been simulated under the low temperature condition. As can be seen from Figure 12, the Coulomb Blockade region was still occurring from 0mv to 20mv of the drain voltage. As compared to the stability chart for the single island SET model, the area that covers the Coulomb Blockade region for multiple island is reduce. This is because the path that can be tunnel by the electron from drain to source also has been increasing. Due to the increased in the tunneling path, the area of Coulomb Blockade region has been reduces.

4.2 Simulation Using Athena

After the simulation of SET model in C-Program simulation file, the works continued with the simulation of the SOIFET structure that has been modeled in the Athena. The SOIFET model structures were showed in Figure 13 and Figure 14. In Figure 13, the green line shows the meshes for the SOIFET structure, and it is concentrated at the silicon channel and at the center of the structure. This is because during the device simulation, it is really crucial to have a finer mesh grid to make sure the calculation done was accurate.

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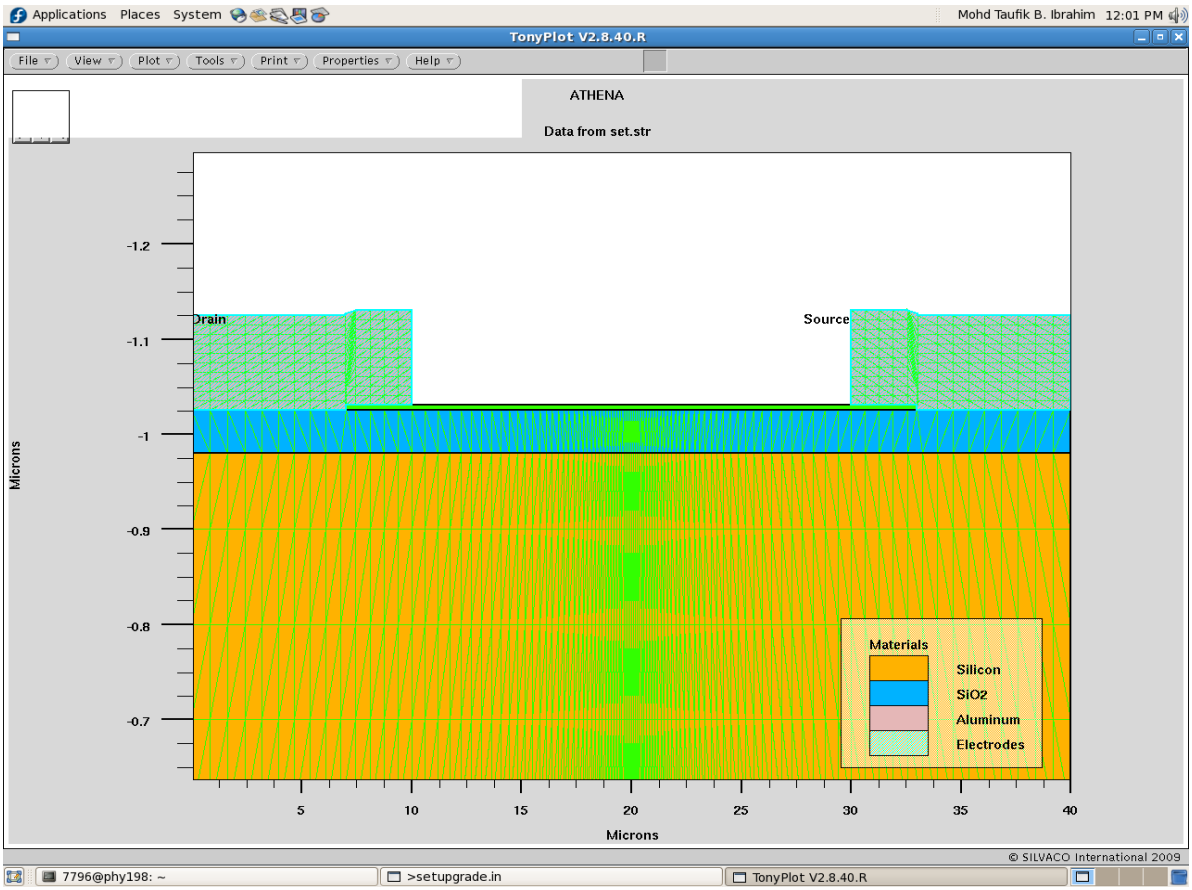

Figure 13 : SET structure in Athena software with meshes

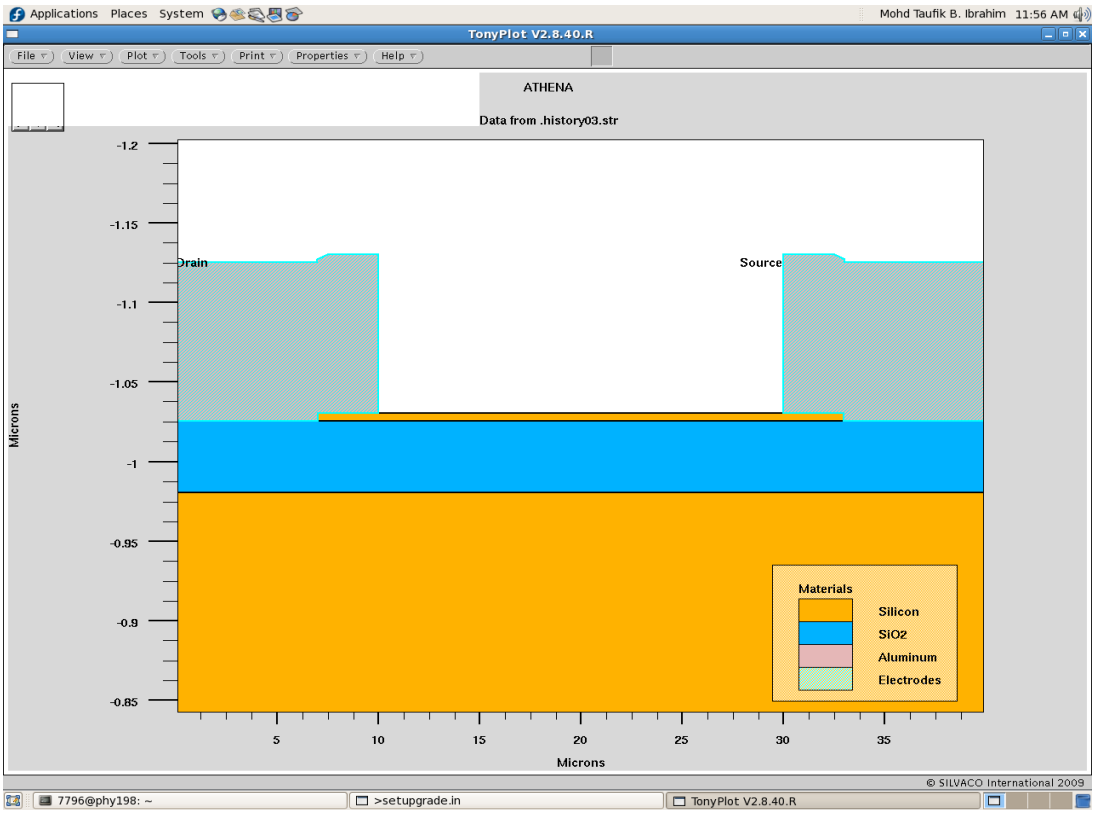

Figure 14 : Top silicon channel of the SOIFET

4.3 Simulation Using Atlas

Then, the I-V characteristic for the SOIFET model was simulated in the Atlas simulation software and the results were plotted for I_d vs. V_d that shown in Figure 15 for the different value of V_g.

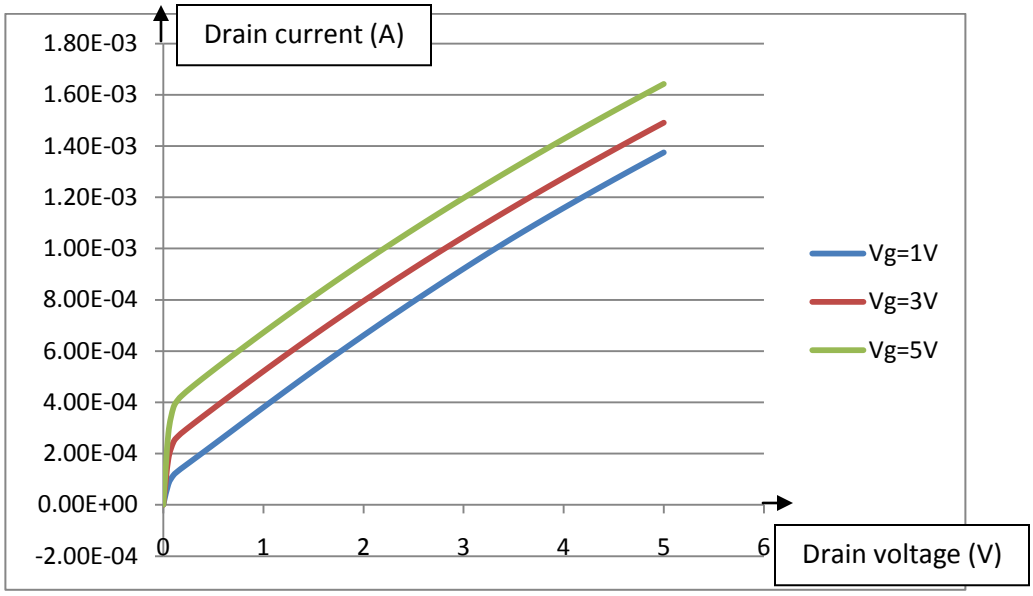

Figure 15 : Graph of I_d vs. V_d for different V_g

From the simulation, it shows that the drain current increases as the drain voltage keep increasing but the drain current do not shows any sign that it will be saturated. As the values of V_g were increases, the current values also increasing.

For Figure 16, it shows the graph of I_d vs. V_g and the value used for V_d was 1mV, 3mV and 5 mV. When drain voltage was increased the value of drain current also increasing. This graph shows that the I_d-V_g characteristic is consistent with the normal MOSFET operation.

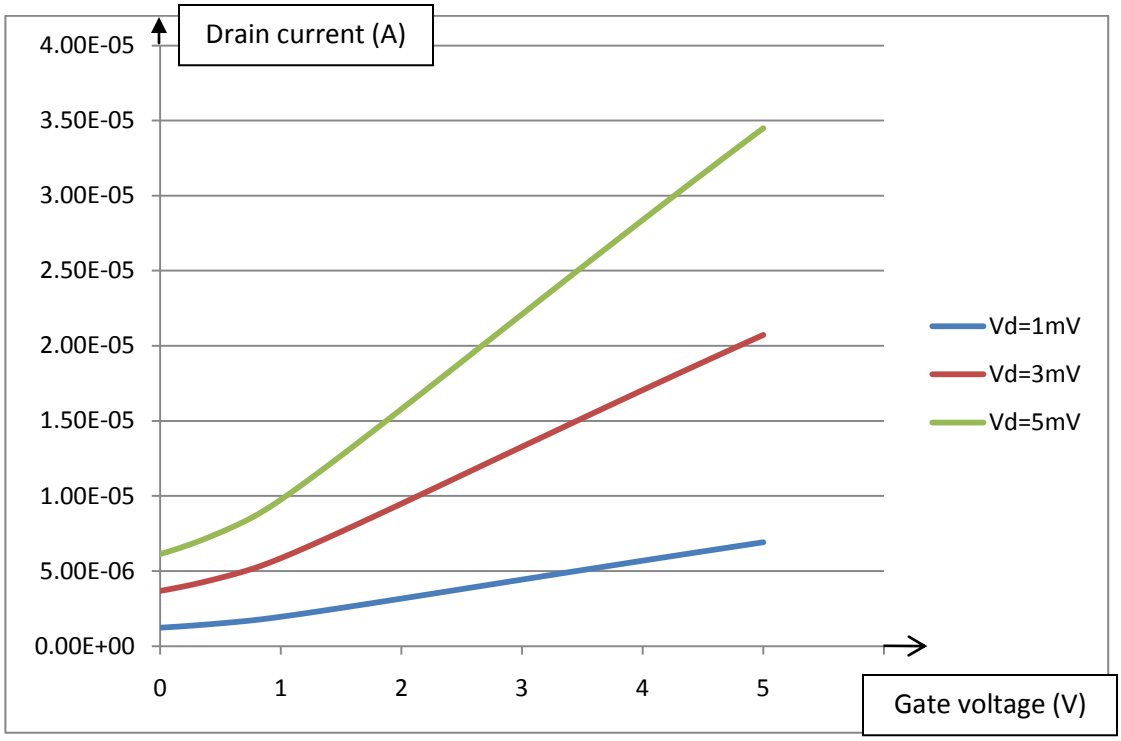

Figure 16 : Graph of I_d vs. V_g for three different V_d

The simulated SOIFET in Atlas simulation have been done at room temperature and the I-V characteristics was different with the SET model that simulated at low temperature in the C-Program simulation file. This shows that increase in temperature minimize or in fact remove Coulomb Blockade characteristics. From now on, the SET simulated on room temperature will be called thin Silicon-on-Insulator FET (SOIFET).

When the SOIFET model was biased with negative sweep for the voltage drain and the gate voltage was negative value, the energy band of the SOIFET was modified. Figure 17 shows the changes on the bending of the energy band. It shows that the depletion increases as the $|V_g|$ was increased. Thus suggest the photon absorption is increased as well.

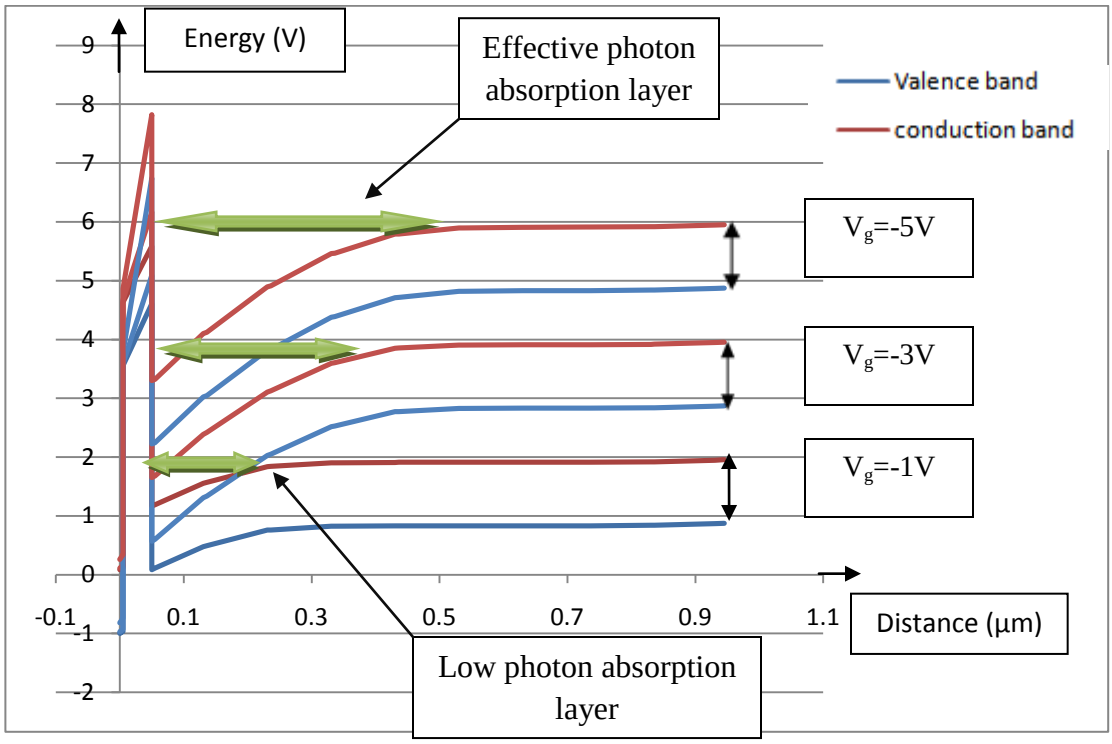

Figure 17 : Energy band diagram for the simulated SOIFET

4.4 Investigate Light Effect

Based on the data of optical properties of intrinsic silicon at 300K [12], the suitable wavelength of light that will be used is about 0.79µm because the skin depth of this wavelength is about 1µm and it is really suitable because the light can nicely penetrate the SOIFET and the hole-pair can be generated at the P-silicon layer.

Table 1: Optical properties of silicon at 300k

Wavelength (µm)	Skin depth (cm)	Photon energy (ev)
0.75	7.63×10^{-4}	1.653
0.76	8.40×10^{-4}	1.632
0.77	9.09×10^{-4}	1.610
0.78	9.71×10^{-4}	1.590
0.79	1.08×10^{-3}	1.570
0.80	1.18×10^{-3}	1.550
0.81	1.29×10^{-3}	1.531

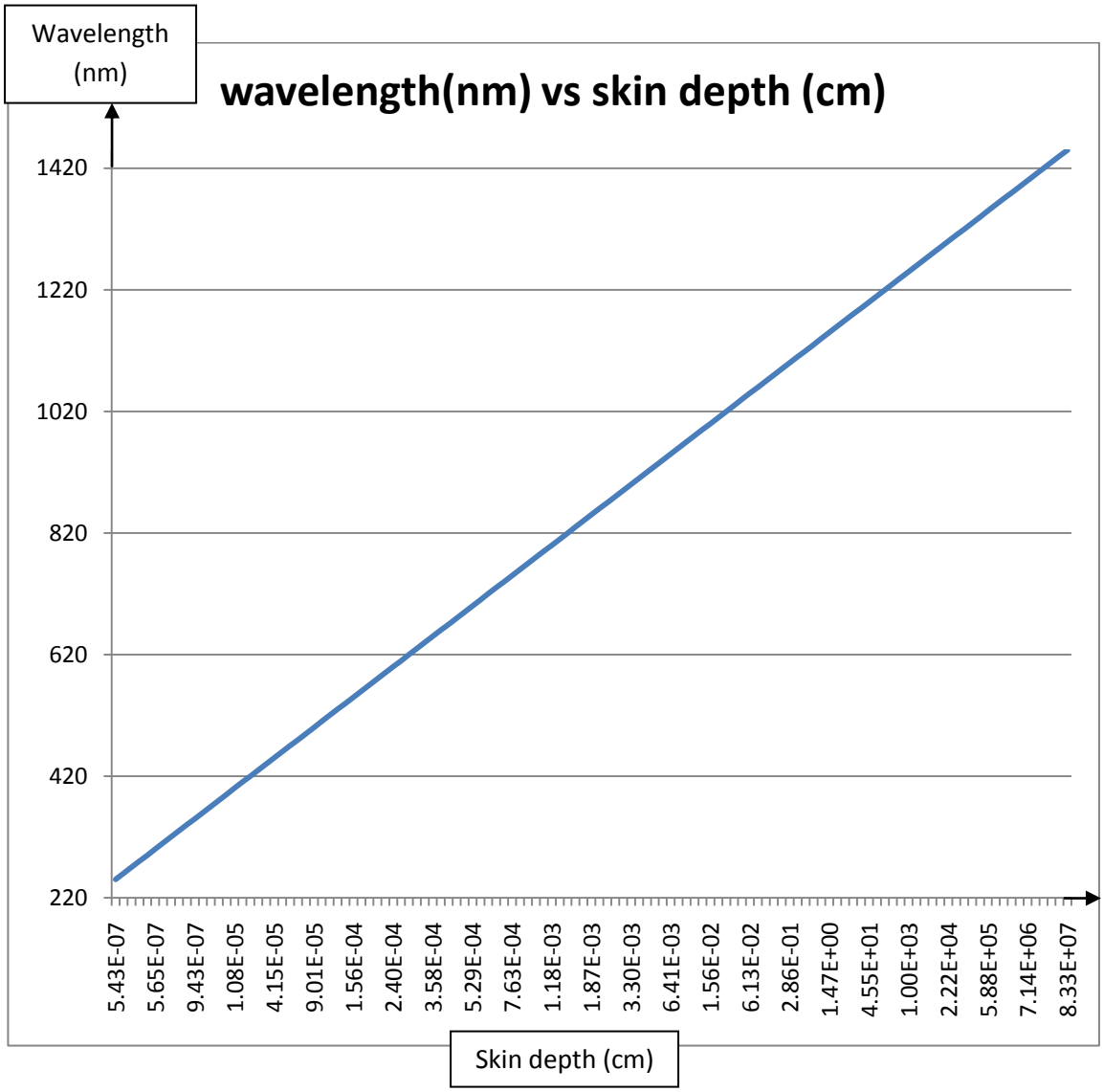

Figure 18 : Graph of wavelength vs. skin depth for the silicon properties at 300K

The minimum energy level that is required to free the valence electron of the silicon is 1.12ev. For light with wavelength that is below the minimum photon energy value, the electron-hole pair cannot be generated. These two factors will determine the wavelength of light that will be used.

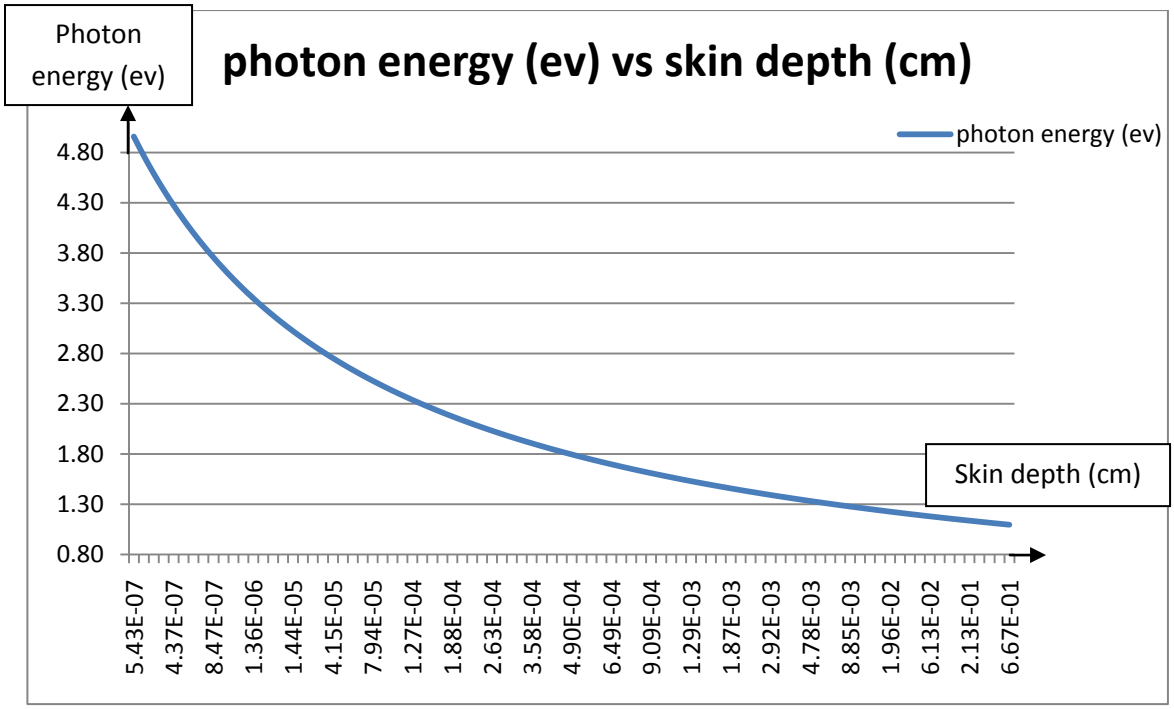

Figure 19 : Grpah for the photon energy vs. skin depth

4.5 Effect of Light Simulated Using Interface Charge

Based on the plotted graph in Figure 20, there were no change in the energy band bending of the valence band and the conduction band at the edge between the silicon oxide and the P-silicon layer. The gate voltage has been fixed to 5V and the

drain voltage has been sweep from 0V to 5V. The interface charge has been introduced to the SOIFET but the bending of the potential profile do not varies. It seems that the interface charge introduce to the SOIFET does not give the expected results where it is expected that by introducing the interface charge, the energy bending will be modulated. However, the unexpected result may have been caused by incorrect parameters used during the simulation that has not been identified yet at this time.

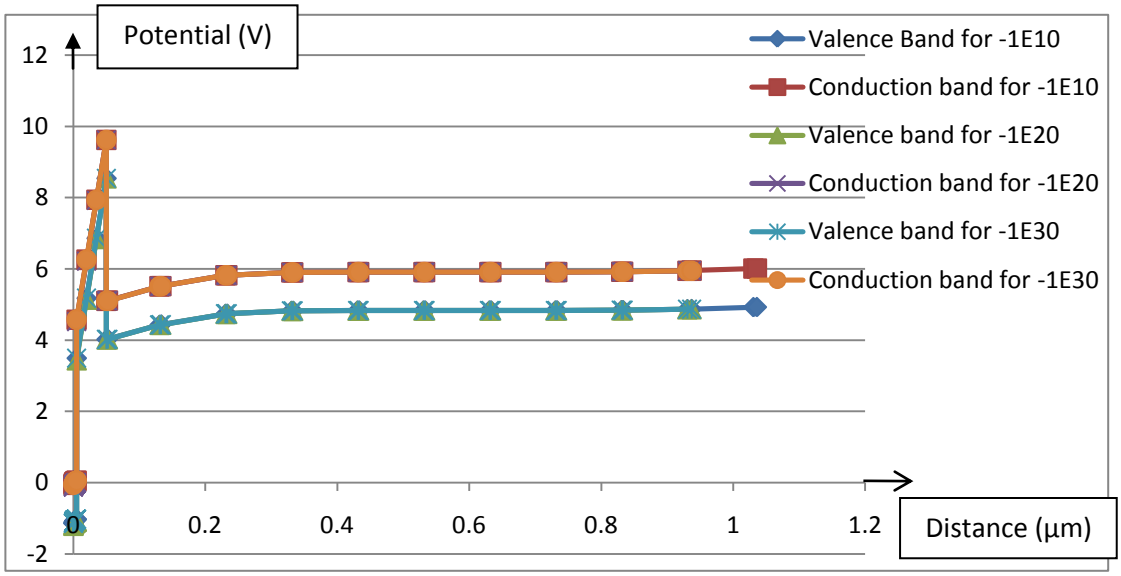

Figure 20 : Energy band diagram for SOIFET with different interface charge density

CHAPTER 5
CONCLUSION AND RECOMMENDATION

The SOIFET model has been build and the properties of I-V curve at low and room temperature were presented. It shown that it operates based on the theory of Coulomb blockade. The wavelength of the light that is suitable to be used is about 0.79μm and it penetrates to the P-silicon layer of the SOIFET. There is an inconclusive result for the effect of photon induced charge in the SOIFET because the band diagram does not change as expected. Therefore, the effect of the photon induced charge cannot be seen clearly.

As for the recommendation, this project needs to be revised. The errors in the simulation might be identified. Furthermore, much time are needed in order to simulate the thin SOIFET in many conditions and acquire all data from the simulation.

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APPENDICES

APPENDIX 1

CODING ATHENA AND ATLAS

Coding for Athena

```
go athena

#Define the mesh
Line x loc=0.00 spac=0.8
Line x loc=0.03 spac=0.6
Line x loc=0.05 spac=0.08
#
Line y loc=0.00 spac=0.08
Line y loc=0.8 spac=0.1
Line y loc=1.0 spac=0.5
Line y loc=40 spac=0.8

#Mesh initialize
Init silicon c.boron=3.0e18 orientation=100 two.d

#P-silicon deposition
Deposit silicon thick=1 c.boron=1.5e16 divisions=10

#Gate oxidation
Diffuse time=11.5626 temp=1040.63 dryo2 press=1.57672 hcl.pc=5.25572

#Extract gate oxide thickness
Extract name=”gateoxide” thickness material=”SiO~2” mat.occno=1 x.val=0.05

#Silicon channel deposition (5nm)
Deposit silicon thick=0.005 c.boron=1.5e16 divisions=10

#Etch the silicon channel
Etch silicon left p1.x=0.01

#Deposit the aluminum electrode
Deposit aluminum thick=0.1 divisions=10

#Etch the aluminum
Etch aluminum right p1.x=0.2
```

```
#Completed the structure by mirrored
Struct mirror right

#Declare the electrode name
Electrode name =drain  x=0.01
Electrode name=source  x=0.09
Electrode name=gate  backside

#Output file
Struct outfile=taufikset.str
```

Coding for Atlas

```
Go atlas

#Get the structure input file from Athena
Mesh   infile=taufikset.str

#Define the model use for this simulation
Models  srh  cvt  boltzman  print  temperature=300

#Mobility parameter for carrier
Mobility     bn.cvt=4.75e+07 bp.cvt=9.925e+06 cn.cvt=174000 cp.cvt=884200 \
             taun.cvt=0.125 taup.cvt=0.0317 gamn.cvt=2.5 gamp.cvt=2.2 \
             mu0n.cvt=52.2 mu0p.cvt=44.9 mu1n.cvt=43.4 mu1p.cvt=29 \
             mumaxn.cvt=1417 mumaxp.cvt=470.5 crn.cvt=9.68e+16 crp.cvt=2.23e+17 \
             csn.cvt=3.43e+20 csp.cvt=6.1e+20 alphn.cvt=0.68 alphp.cvt=0.71 \
             betan.cvt=2 betap.cvt=2 pcn.cvt=0 pcp.cvt=2.3e+15 deln.cvt=5.82e+14 \
             delp.cvt=2.0546e+14

#Declare contact workfunction
Contact  name=drain   aluminum
Contact  name=source   aluminum

#Interface charge
Interface   x.min=0.01   x.max=0.09   y.min=-0.98   y.max=-0.2   s.n=1e17 s.p=1e17 \
              q.f= -1e20

#Method use to solve  the simulation
Method      newton gummel  itlimit=5  trap  atrap=0.5  maxtrap=4  auton r \
            nrcriterion=0.1  tol.time=0.005  dt.min=1e-25  damped delta=0.5 \
            damploop=10  dfactor=10  iccg lu1cri=0.003 lu2cri=0.03 maxinner=25

#solve for Id-Vd curve
Solve init
Solve vgate=3
Log outf=set1_0.log
Solve name=drain  vdrain=0  vfinal=5  vstep=0.05
 Tonyplot set1_0.log
Log off
```

```
#solve for Id-Vg curve
Solve init
Solve vdrain=0.001
Log outf=2_0.log
Solve name=gate vgate=0  vfinal=5  vstep=0.05
Tonyplot set2_0.log
```

APPENDIX 2

INPUT FILE FOR C-PROGRAM BASED ON COULOMB BLOCKADE EFFECT

Input file for single island SET

```
c1      0       2       2a      1x

c2      2       1       2a      1x

cg      2       3       1a


vd      1       0       10m

vg      3       0       (-300m  -290m  -280m  -270m  -260m  -250m  -240m  -230m  -220m
        -210m   -200m   -190m   -180m   -170m   -160m   -150m   -140m   -130m   -120m   -110m
        -100m   -90m    -80m    -70m    -60m    -50m    -40m    -30m    -20m    -10m    0m
        10m     20m     30m     40m     50m     60m     70m     80m     90m     100m    110m
        120m    130m    140m    150m    160m    170m    180m    190m    200m    210m    220m
        230m    240m    250m    260m    270m    280m    290m    300m)

s       2

q       0


i       1       2       3n

time    53n
```

Input file for the multiple islands SET

c1	1	2	2a	1x
c2	2	3	2a	1x
c3	1	3	2a	1x
c4	3	4	2a	1x
c5	1	4	2a	1x
c6	4	5	2a	1x
c7	1	5	2a	1x
c8	5	6	2a	1x
c9	1	6	2a	1x
c10	2	7	2a	1x
c11	7	8	2a	1x
c12	3	8	2a	1x
c13	8	9	2a	1x
c14	4	9	2a	1x
c15	9	10	2a	1x
c16	5	10	2a	1x
c17	10	11	2a	1x
c18	6	11	2a	1x
c19	7	12	2a	1x
c20	12	13	2a	1x
c21	8	13	2a	1x

c22	13	14	2a	1x
c23	9	14	2a	1x
c24	14	15	2a	1x
c25	10	15	2a	1x
c26	15	16	2a	1x
c27	11	16	2a	1x
c28	12	17	2a	1x
c29	17	18	2a	1x
c30	13	18	2a	1x
c31	18	19	2a	1x
c32	14	19	2a	1x
c33	19	20	2a	1x
c34	15	20	2a	1x
c35	20	21	2a	1x
c36	16	21	2a	1x
c37	17	22	2a	1x
c38	22	23	2a	1x
c39	18	23	2a	1x
c40	23	24	2a	1x
c41	19	24	2a	1x
c42	24	25	2a	1x
c43	20	25	2a	1x
c44	25	26	2a	1x
c45	21	26	2a	1x

c46	22	0	2a	1x
c47	23	0	2a	1x
c48	24	0	2a	1x
c49	25	0	2a	1x
c50	26	0	2a	1x

cg1	2	27	1a
cg2	3	27	1a
cg3	4	27	1a
cg4	5	27	1a
cg5	6	27	1a
cg6	7	27	1a
cg7	8	27	1a
cg8	9	27	1a
cg9	10	27	1a
cg10	11	27	1a

cg11	12	27	1a
cg12	13	27	1a
cg13	14	27	1a
cg14	15	27	1a
cg15	16	27	1a
cg16	17	27	1a
cg17	18	27	1a
cg18	19	27	1a
cg19	20	27	1a

cg20	21	27	1a
cg21	22	27	1a
cg22	23	27	1a
cg23	24	27	1a
cg24	25	27	1a
cg25	26	27	1a
vd	1	0	150m
vg	27	0	(0m 10m 20m 30m 40m 50m 60m 70m 80m 90m 100m 110m 120m 130m 140m 150m 160m 170m 180m 190m 200m)

s	2	3	4	5	6	7	8	9	10	11	12
	13	14	15	16	17	18	19	20	21	22	23
	24	25	26								
q	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0
	0	0	0								
i	0	1	3n								
time	53n										

APPENDIX 3

GANTT CHART FOR PROJECT WORK

Milestone for the First Semester of 2-Semester Final Year Project

No.	Detail/ Week	1	2	3	4	5	6	7		8	9	10	11	12	13	14
1	Selection of Project Topic	■	■						Mid-semester break							
2	Preliminary Research Work		■	■	■											
					●											
3	Submission of Preliminary Report															
4	Seminar 1 (optional)					■	■	■								
5	Project Work (Athena and Atlas simulation)					■	■	■								
										●						
6	Submission of Progress Report															
7	Seminar 2 (compulsory)										■	■	■	■		
8	Project work (orthodox theory of coulomb blockade)									■	■	■	■	■	●	
9	Submission of Interim Report Final Draft															●
10	Oral Presentation															
			●													

■ Suggested milestone

■ Process

Milestone for the Second Semester of 2-Semester Final Year Project

No.	Detail/ Week	1	2	3	4	5	6	7		8	9	10	11	12	13	14
1	Project Work Continue	■	■	■					Mid-Semester Break							
2	Submission of Progress Report 1				●											
3	Project Work Continue				■	■	■	■								
4	Submission of Progress Report 2									●						
5	Seminar (compulsory)										■	■	■			
5	Project work continue									■	■	■	■			
6	Poster Exhibition											●				
7	Submission of Dissertation (soft bound)													●		
8	Oral Presentation														●	
9	Submission of Project Dissertation (Hard Bound)															●

● Suggested milestone

■ Process