NUMERICAL DIRECTIONAL OVERCURRENT PROTECTION FOR POWER DISTRIBUTION NETWORK

By

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FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
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CERTIFICATION OF APPROVAL

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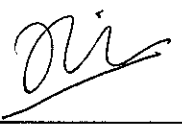
CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



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ABSTRACT

The study propose the use of symmetrical-phase-sequence which combine both fault direction and inverse time response characteristics of overcurrent protection in determining fault direction with high sensitivity in parallel transmission lines. Non-directional overcurrent protection systems fail to discriminate the fault for the relay co-ordination when fault current can flows in either forward or reverse directions. In the other hands, analogue overcurrent protection system has many weaknesses such as very low reliability, inaccurate, inconsistence, and slow response which can be encountered by using digital technique. Meanwhile for the single transmission lines models, there are still several flaws that can be found, like if a fault occurred in the middle of transmission line and in the same time one of the generator facing a problem, certain busbar that supplied to the load will lost its function. The scheme used is based on the symmetrical-phase-sequence components which consist of zero-phase sequence, positive-phase sequence, and negative-phase sequence. Some studies have been made to identify several types of faults related to the systems proposed. Every protection systems have three basic components: instrument transformers, relays and circuit breakers. Generally, the currents and voltages of each phase are converted from analogue to digital signal by data acquisition system (DAS), which located inside digital directional overcurrent relay. The concept to be employed to perform digital directional overcurrent protection system is discussed in this report. The future work to be done is to do simulation in order to prove that the algorithm proposed is applicable to perform the digital directional overcurrent protection for the parallel-line distribution network.

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Greatest thanks to my family and friends and everywhere for their support and prayers for my success. Besides, the author also wishes to thank those who have either directly or indirectly involve in this project. May God pay for their kindness.

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ABBREVIATIONS AND NOMENCLATURES

TMS	Time multiplier setting
I_s	Relay setting current
$\mathbf{V}$	Voltage phasor
$\mathbf{I}$	Current phasor
$\mathbf{I_{res}}$	Phasor of residual current
$\mathbf{V_a}$	Phasor of voltage in phase a
$\mathbf{V_b}$	Phasor of voltage in phase b
$\mathbf{V_c}$	Phasor of voltage in phase c
$\mathbf{I_a}$	Phasor of current in phase a
$\mathbf{I_b}$	Phasor of current in phase b
$\mathbf{I_c}$	Phasor of current in phase c
R	Resistance
X	Reactance
Z	Magnitude of impedance
θ_Z	Angle of impedance
θ_v	Angle of the voltage
θ_i	Angle of the current
Δt	Sampling time interval
V_a	Magnitude of the voltage in phase a
V_b	Magnitude of the voltage in phase b
V_c	Magnitude of the voltage in phase c
I_a	Magnitude of the current in phase a
I_b	Magnitude of the current in phase b
I_c	Magnitude of the current in phase c
I_{res}	Magnitude of the residual current

I_s Magnitude of the current setting

I_{resset} Magnitude of the residual current setting

V_{set} Magnitude of voltage setting

Δ Increment

$\mathbf{V}_{fk}^{a}$ Phasor of the fault voltage in phase a at the fault location k

$\mathbf{V}_{fk}^{b}$ Phasor of the fault voltage in phase b at the fault location k

$\mathbf{V}_{fk}^{c}$ Phasor of the fault voltage in phase c at the fault location k

$\mathbf{I}_{fk}^{a}$ Phasor of the fault current in phase a at the fault location k

$\mathbf{I}_{fk}^{b}$ Phasor of the fault current in phase b at the fault location k

$\mathbf{I}_{fk}^{c}$ Phasor of the fault current in phase c at the fault location k

$\mathbf{V}_{fk}^{0}$ Phasor of the fault voltage in zero-phase-sequence at the fault location k

$\mathbf{V}_{fk}^{1}$ Phasor of the fault voltage in positive-phase-sequence at the fault location k

$\mathbf{V}_{fk}^{2}$ Phasor of the fault voltage in negative-phase-sequence at the fault location k

$\mathbf{I}_{fk}^{0}$ Phasor of the fault current in zero-phase-sequence at the fault location k

$\mathbf{I}_{fk}^{1}$ Phasor of the fault current in positive-phase-sequence at the fault location k

$\mathbf{I}_{fk}^{2}$ Phasor of the fault current in negative-phase-sequence at the fault location k

$\mathbf{A}^{0}$ Busbar A in zero-phase-sequence

$\mathbf{B}^{0}$ Busbar B in zero-phase-sequence

$\mathbf{C}^{0}$ Busbar C in zero-phase-sequence

$\mathbf{I}_A^0$ Phasor of the current in zero-phase-sequence at the busbar A

$\mathbf{V}_A^0$ Phasor of the voltage in zero-phase-sequence at the busbar A

$\mathbf{Z}^0$ Phasor of the impedance in zero-phase-sequence

Z^0 Magnitude of the impedance in zero-phase-sequence

$\theta_z{}^0$ Angle of the impedance in zero-phase-sequence

$\theta_{VA}{}^0$ Angle of the voltage in zero-phase-sequence at the busbar A

$\theta_{IA}{}^0$ Angle of the current in zero-phase-sequence at the busbar A

R^0 Resistance in zero-phase-sequence

X^0 Reactance in zero-phase-sequence

$\mathbf{Z}^2$ Phasor of the impedance in negative-phase-sequence

Z^2 Magnitude of the impedance in negative-phase-sequence

$\theta_z{}^2$ Angle of the impedance in negative-phase-sequence

R^2 Resistance in negative-phase-sequence

X^2 Reactance in negative-phase-sequence

$\theta_{VA}{}^2$ Angle of the voltage in negative-phase-sequence at the busbar A

$\theta_{IA}{}^2$ Angle of the current in negative-phase-sequence at the busbar A

CHAPTER 1
INTRODUCTION

1.1 Background of Study

The National Electrical Code® defines overcurrent as any current in excess of the rated current of equipment or the capacity of a conductor. It may result from overload, short circuit, or ground fault.

Overcurrent is defined as any current in excess of the rated current of equipment or the capacity of a conductor. It may result from short circuit or ground fault. Current flow in a conductor always generates heat. Thus, the greater is the current flow, the hotter the conductor. The excess heat can damage the electrical components. For that reason, a conductor has a rated continuous current carrying capacity or also known as capacity of the conductor which cannot be exceeded.

Overcurrent protection devices are used to protect conductors from excessive current flow and designed to keep current flow at a safe level to prevent the circuit conductors from overheating and damaging equipment.

Basically, in overcurrent protection, it is required to isolate only the faulty section or zone of the power system network and leaving the rest of the system uninterrupted or remain in operation. Therefore, it is necessary to provide discrimination to achieve correct relay co-ordination for all the relays in the network.

Conventional overcurrent protection is totally depends on the circuit current. When the fault current can flows in either forward or reverse direction through a circuit

breaker, the overcurrent relay at that location will not be able to provide necessary discrimination for protection purpose. Thus, the directional overcurrent protection is required to provide directional discrimination and hence, the circuit breaker will be operated appropriately.

Basically, there are three possible methods to achieve correct discrimination. The first method is the discrimination by time. Meanwhile, the second method is to obtain discrimination by current that relies on the fact that the fault current varies with the position of the fault because of the difference in impedance values between the source and the fault. The third method, which is the best method, is to combine both time and current to achieve discrimination.

Directional overcurrent principle depends on both voltage and current in the circuit. Thus, additional voltage input must be provided to the relay. Then, it is possible to define the direction of the fault occurrence. Therefore, tripping command will only be generated to the circuit breaker if the fault is in the forward direction to clear the fault from the whole system.

In this report, forward fault is referred to the fault which is in the direction of protection coverage. Meanwhile, the reverse fault is the fault that is in the opposite direction of the forward fault.

Moreover, the enthusiasm to use numerical technology for the protection system has been due to the perceived power of the technology to improve and change the way thing is done. This project will fully utilize the development and advantages in the numerical technology to design the numerical directional overcurrent protection.

1.2 Problem statement

Conventional non-directional overcurrent protection system cannot provide necessary discrimination for the correct relay co-ordination when fault current can flows in either forward or reverse directions through circuit breaker at the relay

location. For example, system with loops and/or multiple infeeds cannot be efficiently protected by conventional overcurrent protection. Thus, the directional overcurrent protection is needed to provide proper discrimination.

In addition, analogue overcurrent protection system that is based on electromechanical co-ordination has countless weaknesses such as very low reliability, inaccurate, inconsistence, slow and many others. These weaknesses must be encountered to provide a better protection system, thus, enhance the power system itself. Consequently, the numerical system development seems to be the best solution to be employed to the directional overcurrent protection to encounter all the weaknesses in analogue system.

1.3 Objectives

The objectives to be achieved in the project are:

- To use symmetrical-phase-sequence components to provide directional property.
- To determine and simulate the directional discrimination principle for numerical directional overcurrent protection related to the three-phase balance fault and earth fault.

1.4 Scope of study

The project mainly covering the determination and simulation of directional discrimination algorithm related to the three-phase balanced fault and earth fault using symmetrical-phase-sequence components technique. Due to the time limitation, this project is not covering the simulation of the time/current grading principle and directional discrimination of other types of faults.

CHAPTER 2
LITERATURE REVIEW

2.1 Implementation of Time/Current Grading in Numerical System

Basically, in overcurrent protection, it is required to isolate only the faulty section or zone of the power system network and leaving the rest of the system uninterrupted or remain in operation. There are three possible methods to achieve correct discrimination.

The first method is the discrimination by time. An appropriate time setting is given to each relays controlling the circuit breakers in power system to ensure that the breaker nearest to the fault opens first. However, more severe fault is cleared in the longest operating time.

Meanwhile, the second method is to obtain discrimination by current, which relies on the fact that the fault current varies with the position of the fault because of the difference in impedance values between the source and the fault.

The best method is to combine both time and current to achieve discrimination. Disadvantages due to the discrimination by time or current alone are countered with this method.

2.2 Overview of Directional Discrimination Property

Consider the network in Figure 2-1. In this network, the feeder has infeeds from both ends. Lets take that the protection location is at busbar C as shown in Figure 2-1. If fault occurs at F_1, it is said to be a forward fault, and if it occurs at F_2 it should be identified as a reverse fault. At the protection location as shown in Figure 2-1, if the fault occurs between busbars C and B, then circuit breaker CB1 is tripped. But if the fault occurs between busbars C and D, the circuit breaker should not be tripped. However, the fault current, $\mathbf{I_F}$, can flows through CB1 in either forward or reverse direction. Therefore, we need to have directional element to discriminate the direction of the fault and hence only trips CB1 when fault occurs between busbars C and B.

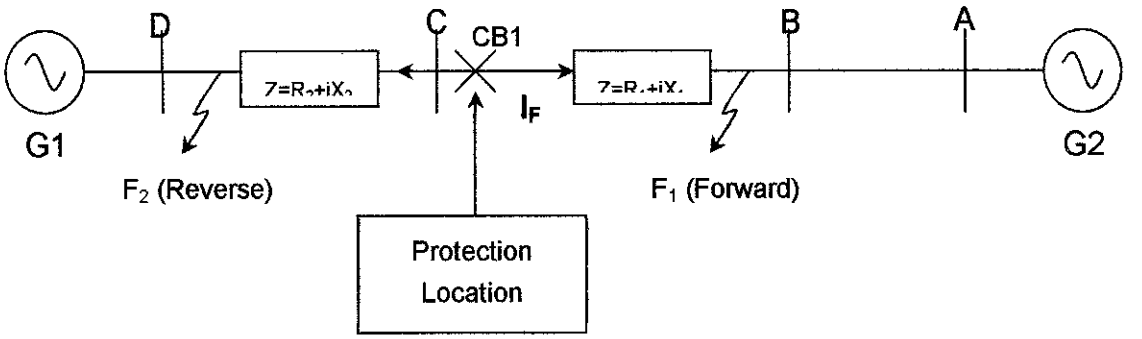

Figure 2-1: Network feeder having infeeds from both ends

In this project, the direction of fault is determined by using the phase angles of the voltages and current phasors at the protection location. Basically, the directional detection can be developed based on symmetrical-phase-sequence components of voltage and current phasors measured.

Negative-phase-sequence components are used for phase-to-phase faults. For earth faults, zero-phase-sequence components provide reliable detection of fault direction. Hence, algorithm is developed for distinguishing between phase faults and earth faults. This allows the correct sequence components to be chosen in the processing. The use of negative- and zero-phase-sequence components offer high sensitivity

which is independent of load currents and avoid the problems encountered in close-up faults in detecting direction of phase-to-phase faults or phase-to-earth faults. For three-phase balanced faults where both the negative- and zero-phase-sequence components are negligible, phase voltages and currents are applied to achieve the required directional property.

In this report, the directional discrimination property for the three-phase balance fault and earth fault are developed and discussed in detail.

2.3 Numerical Directional Overcurrent Protection Components

2.3.1 Overview

Components in numerical protection can be divided into several sub systems which are [1]:

a. signal conditioning subsystem
b. conversion subsystem
c. numerical processing relay subsystem

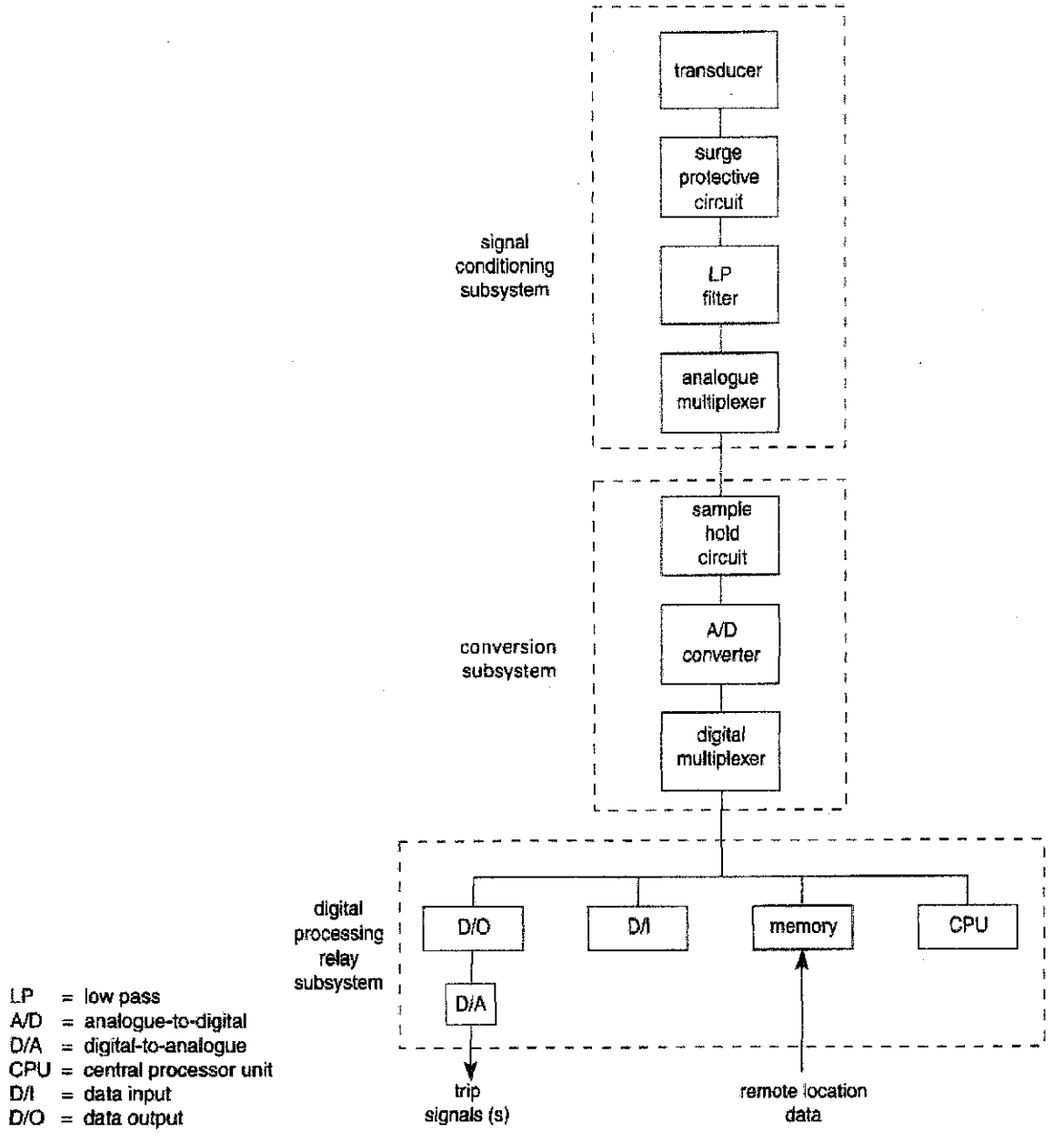

Figure 2-2: Basic components of a numerical relay

HVDC simulators are required in order to conduct the simulation studies for HVDC transmission system. There are three possible software that can be used for that purpose which are ATP, ATOSEC5 and SIMUSEC. Each software is designed for time domain analysis of power supply, power electronic converters and converter fed machine respectively.

ATP is an EMTP simulation program that is used in analyzing power system, which includes thyristor converters that are used in HVDC transmission system. There are

several reasons that make ETP widely utilized in power simulation studies such as it has list of models for the power system components and its price-wise affordability. The usage of ATP can be applied in the study of power electronic converter and system that use electronic converters.

2.3.2 Signal Conditioning Subsystem

Transducer

Primary current and voltage transducers (CTs and VTs) reduced currents either to 5A or 1A, and voltages to 110V or 120V. These must be done because primary power system currents and voltages are usually relatively high and not possible to transfer these signal to protective relays.

Surge Protection Circuits

Surge protective circuits consist of capacitors and isolating transformers that connected from CTs and VTs, which means the current and voltage from secondary is flowed to this components. Zener diodes are also commonly utilized, but it depends on the exact physical circuit arrangement used. It common function is to convert the secondary current measurands into low-level voltage signals with a suitable connected burden and current-to-voltage amplifier arrangement. Secondly used are careful screening techniques.

Analogue Filtering

Low-pass filters is usually used to separate unwanted high frequencies before sampling, and the amount of filtering depends on the data requirements of a particular numerical relay. Anti-aliasing function that is importantly fulfilled by the analogue low-pass filters, which must be designed with a cutoff frequency (f_c) that perform satisfactory signal components rejection above a given frequency. Important factors of the low-pass filters:

a) the rise time, which gives a indication of duration it takes the output of a low-pass filter to traverse its final value following a step unit;
b) the overshoot, which indicates by how much the filter output will exceed its steady-state value on the initial response to a unit step input;
c) the settling time, which is an indication of duration it takes a given filter to settle at its steady-state output value;

Analogue Multiplexers

Its main function to selects a signal from one of a number of inputs channels and transfers it to its output channels, by that means permitting the transmission of several signals in a serial manner over a single communication channel. This concept of multiplexing has its origins in communications engineering. The principles of multiplexing are shown in Figure 2-3, in which the solid-state multiplexer is same to multi-terminal rotary switch.

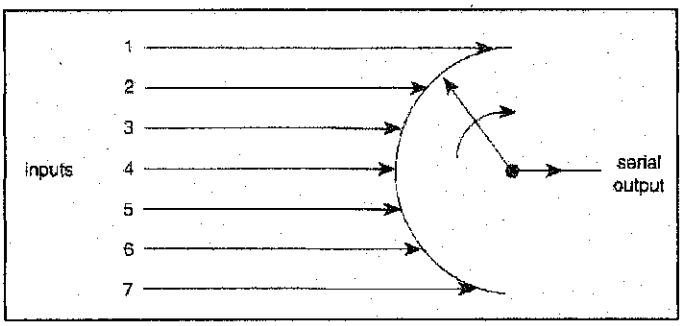

Figure 2-3: Principle of multiplexing

2.3.3 Conversion Subsystem

The Sampling Theorem

A band-limited signal can be uniquely specified by its sampled values if and only if the sampling frequency is at least twice the maximum frequency component contained within the original signal and this is what we call sampling theorem.

$$f_s \geq 2f_m$$

Where f_s is the sampling frequency and f_m is the maximum significant frequency within the signal sampled.

The Nyquist frequency f_N, is known as a frequency component at half the sampling frequency.

$$f_N = f_s/2$$

To achieved sampling process effectively, an analogue signal $f(t)$ is connecting to the data acquisition system by means of a fast acting switch, which closes for a very short

time but remains open for the rest of the period. This activity can be viewed as a multiplier.

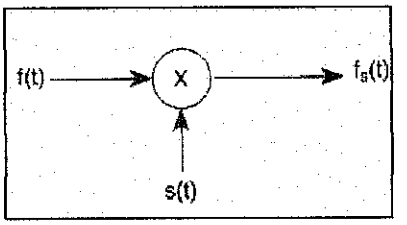

Figure 2-4: Sampling process, shown representation of the sampler.

Where $f(t)$ is the band-limited analogue signal to be sampled, and $s(t)$ is known as a sampling function. In result, sampling function is made of a train of pulses alternating between a value of +1 and 0. Thus can be defined as follows:

$$s(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_s)$$

The output of the multiplier $f_s(t)$ is then

$$f_s(t) = f(t) \sum_{n=-\infty}^{\infty} \delta(t - nT_s)$$

$$= \sum_{n=-\infty}^{\infty} f(nT_s)\delta(t - nT_s)$$

Signal aliasing error

When sampling rate is set so that sampling frequency less than twice the maximum significant frequency contained in the original signal, then equation

$$f_s \geq 2f_m$$

is not satisfied. There will be an overlap between adjacent part of $F_s(\omega)$, that causes an error in the analysis as a result of difficulty in distinguishing between low- and high-frequency components. This error basically known as 'aliasing error'. In the condition when the sampling rate does not meet the above equation, a low-frequency component that does not actually exist in the original signal, would nevertheless be apparent within the sampled signal.

Sample and hold circuit

Each sample can be stored or held until the next sample is taken when switched-capacitor is replaced. This activity gives sufficient time to elapse for the subsequent process of analogue to-digital conversion to be completed. Figure 2-5 shows the principles of a simple sample and hold circuit.

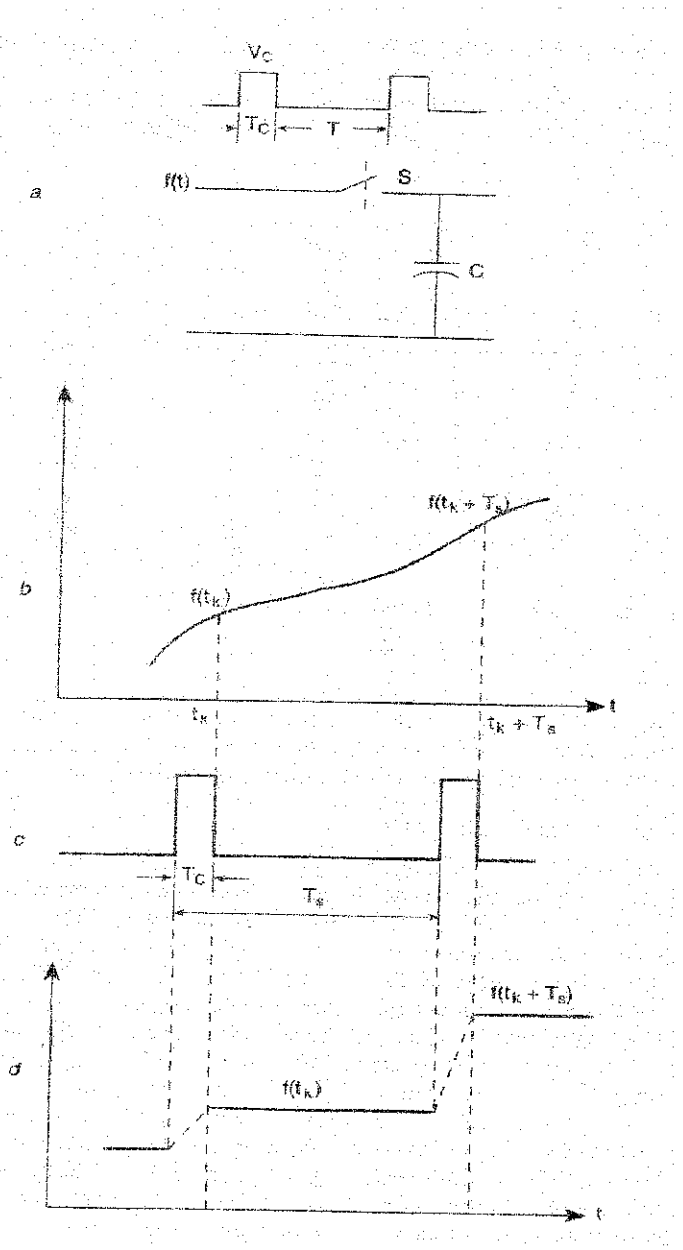

Figure 2-5: Sample and hold circuit principle (a) switching circuit, (b) analogue input, (c) control waveform, (d) circuit output

Analogue signal $f(t)$ which is sampled at a rate of $1/T_s$ is an input signal. Control Waveform V_c, function as to control the sampling by closes and opens the switch. The capacitor is charged to the value $f(t)$ during the closing time T_c, while during the hold time $T_H = T_s - T_c$, the capacitor holds the sample value. Performance of all devices work on the principles outlined, being defined in terms of accuracy and sampling rates.

Digital multiplexing

A network with a number of input ports channeled to a single output is called digital multiplexer. Digital words of information of one or more bits are the inputs to these ports. A general representation of a digital multiplexer that allows one of its three inputs to pass to the output is shown in the Figure 2-6;

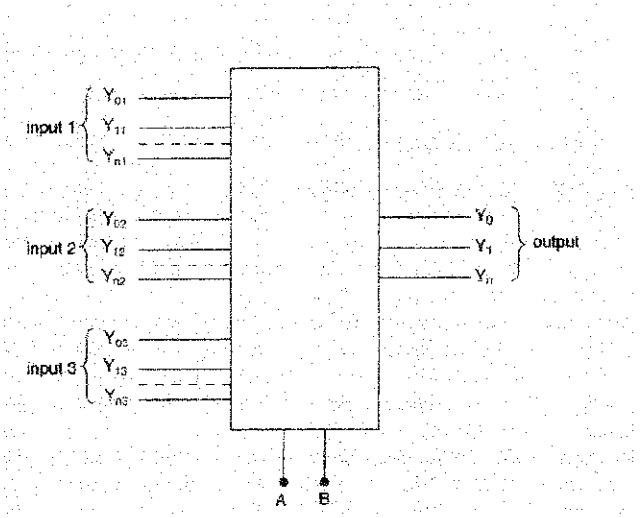

Figure 2-6: Digital multiplexer arrangement

Digital-to-analog conversion

A device for converting a digital (usually binary) code to an analog signal is called digital-to-analog converter. The operation such as converting a four-bit binary parallel digital word $W_3W_2W_1W_0$, which W_i can be either 0 or 1, to the analogue voltage that is proportional to the binary number represented in digital word. If W_i = 1, then S_i is connected to V_R, while in the other hand when W_i = 0, then S_i is connected to ground. (Figure 2-7)

One thing to be noticed is that, input impedance of the operational amplifier is very high, the currents I_s and I_f are roughly equal to each other. The equation that can relate between output voltage of the operational amplifier (V_o) and the digital input can be derived as follows:

$$I_s = (2^3W_3 + 2^2W_2 + 2^1W_1 + 2^0W_0)V_R/R$$

$$V_o = -I_fR_f = -I_sR_f$$

$$= -(2^3W_3 + 2^2W_2 + 2^1W_1 + 2^0W_0)V_RR_f/R$$

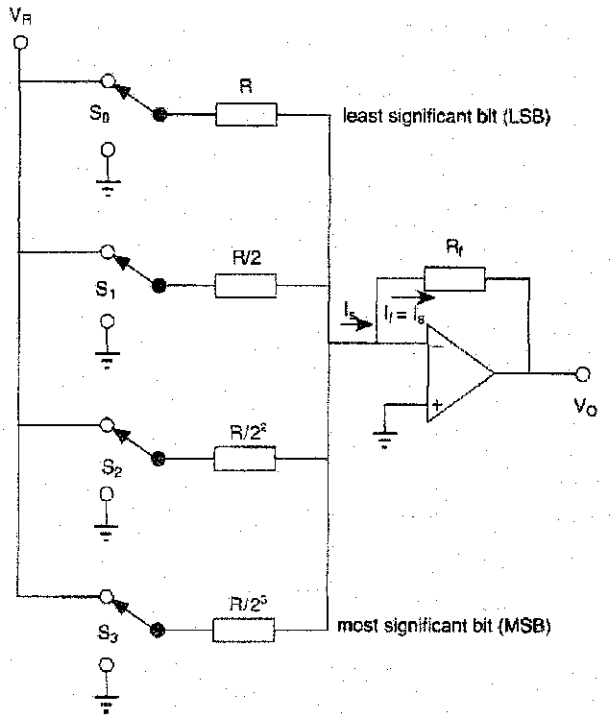

Figure 2-7: Basis of simple digital-to-analogue converter arrangement

Analogue-to-digital conversion

Many methods have been developed in the field of digital integrated electronics for converting analogue signals to digital form. Counter-controlled converters, dual-slope converters and parallel comparator converter are the most commonly being used.

I. Counter-controlled converter

It includes three main components which are: a counter, a D/A converter, and an analogue comparator.

Operations: Counter will set to zero at the starting of each cycle. This will cause the output of D/A converter V_c to be zero. Voltage is compared with the input voltage V_i fed by the sampled-and-hold. Comparator output will be either 1 or 0 depending on the relative magnitudes of V_i and V_c, where if $V_i > V_c$ then 1 will be the output which is used to enable the AND gate. This will make sure the clock pulses to enter the counter. Output voltage of the A/D converter will increase by a single step of 1 V. When V_c become greater than V_i the output will be zero from the comparator. The AND gate then will disable, and make the counter stop because the clock pulses are

prevented from reaching the counter. Output terminal of the counter then will read the output of the A/D converter.

II. Dual-slope converter

This type of converter normally consists of an analogue integrator, a comparator and a counter.

Operation: at default, the switch S_1 is connected to A, and V_a (sample hold voltage) is applied to the analogue integrator for fixed time T1 which integrates V_a. Then switch S_1 is thrown to B, which gives a reference voltage $-V_r$ to the integrator. As a result of integrated reference voltage, the output of the integrator starts to shift in the positive direction. Once the integrator output voltage V_c achieve zero, the G gate will disable, and makes the clock pulses stops from achieving the counter, hence stopping the count. The number pulses acknowledge to the counter is those proportional to the magnitude of the input voltage V_a, which is represent in digital after converted. In actual situation, the reset voltage V_r, is put to stop the count quickly. Even though this type of converter is highly accurate, but it does have a relatively slow rate of conversion, which limits its utilization in certain digital relaying devices.

III. Parallel comparator converter

This comparator consists of C1 to C7, a register of seven flipflops and a decoder. The input is divided into eight reference segments which are ranges from 0 to V_o. Six of those segments have a value of $V_o/7$ the two end segments having a value of $V_o/14$.

Operations:

If an input voltage is ranging from 0 to $V_o/14$, is applied to the converter then the outputs of all comparators will set to logic 0. The output at the converter will be in digital representation in 000, which is equivalent to a zero analogue voltage. The 'quantization' error occurred when an error of $V_o/14$ is introduced on account of the input being equal to one level of resolution ($V_o/14$).

The output of all comparators will be 0 except the first one which will be 1, when the input voltage magnitude is between $V_o/14$, and $3V_o/14$. Register flip-flops

will receive input from comparators at the occurrence of a clock pulse and then register output will convert by the decoder to a three-bit unipolar binary code.

CHAPTER 3
METHODOLOGY/ PROJECT WORK

3.1 Procedure Identification

The procedures adopted to achieve the objectives of this project are illustrated in the flow chart of Figure 3-1.

This project is started by studying the conventional non-directional overcurrent protection system. This is important to get the overview of the overcurrent protection. This is followed by studying the analogue directional overcurrent protection system. The method to achieve overcurrent relay co-ordination in analogue system has to be reviewed to understand the related principle of overcurrent protection. Meanwhile, the directional discrimination technique used is also studied.

The heart of this project is to determine the digital directional overcurrent technique to be implemented in the digital directional overcurrent protection relay. The direction of fault must be distinguished to make sure that a circuit breaker is only tripped in case of a forward fault.

Consequently, a model of a distribution network system is developed. This distribution network system is used to validate the directional overcurrent protection system. The network must have characteristics that make it necessary to apply directional overcurrent relays. For instance, the network with parallel feeders or network which is fed by two generating sources each at different end. The network parameters and other characteristics are selected based on typical distribution network system. Finally, the simulations will be perform, and the results confirm the correctness of the design.

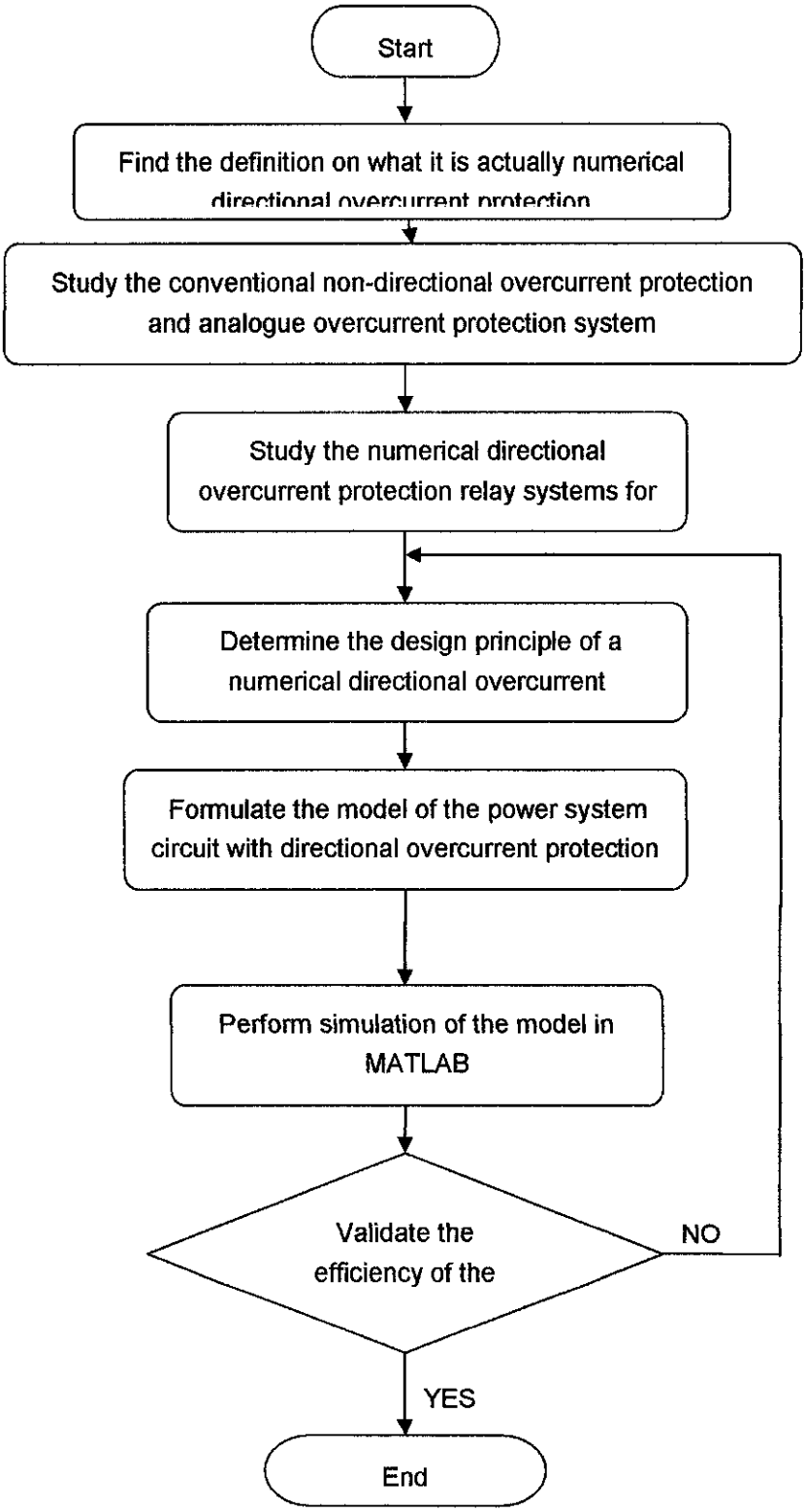

Figure 3-1: Project flow chart

3.2 Software

This project only utilizes the MATLAB software. No hardware is designed or used in order to complete this project.

In addition, MATLAB SimPowerSystems tool is used to design the model of the distribution network as well as to perform simulations in order to test the directional discrimination principle. Moreover, the simulation is also done using MATLAB SimPowerSystems tool to validate the efficiency of the protection system designed.

Basically, SimPowerSystems is an electrical power system analysis and design tool that is a component in MATLAB. SimPowerSystems uses the Simulink environment, allowing user to build a model using simple click and drag procedures. Not only can user draw the circuit topology rapidly, but analysis of the circuit can include its interactions with mechanical, thermal, control, and other disciplines. This is possible because all the electrical parts of the simulation interact with the extensive Simulink modeling library. Since Simulink uses MATLAB as its computational engine, designers can also use MATLAB toolboxes and Simulink blocksets. SimPowerSystems and SimMechanics share a special Physical Modeling block and connection line interface.

3.3 Three-phase-balanced Fault Directional Property

First and foremost, the three-phase balanced fault is analyzed and then necessary technique to obtain directional property for it, can be provided. When three-phase balanced fault occurs, voltage and current phasors at the measurement location will also be balanced. Voltage phasors during the fault will have same magnitude and angle deviation 120° between each other. The current phasors also have the same property. Therefore, if we transform the voltage and current phasors to the symmetrical-phase-sequence components we will notice that negative- and zero-phase sequence component are negligible. Consequently, in this case, we propose to use the phase angle of voltages and currents to detect the direction of fault.

The fundamental equation to determine the direction of current is given by equa. (3.1) below:

$$\frac{\mathbf{V}}{\mathbf{I}} = R + jX = Z\angle\theta_Z \tag{3.1}$$

From equa. (3.1) the voltage is divided by the current which gives the impedance. Hence, the magnitude of the impedance and angle of the impedance can be calculated. The angle of the impedance, θ_Z, is given by equa. (3.2) that is the difference between angle of the voltage, θ_v, and angle of the current, θ_i:

$$\theta_Z = \theta_v - \theta_i \tag{3.2}$$

Besides, θ_Z, is also given by equa (3.3):

$$\tan\theta_Z = \frac{X}{R} \tag{3.3}$$

Referring to Figure 2-1, it is obvious that if fault occurs at F_1 (i.e. forward fault), the fault current, $\mathbf{I}_F$, will flow in the forward direction through the protection location. As the forward direction fault is taken as positive and reverse direction fault as negative, thus, the angle of the impedance when forward fault occurs which is given by equa. (3.2) is obviously will be within 0° to 90° as shown in (3.4):

$$\textit{Forward fault} \quad \text{when} \quad 0^\circ \le \theta_Z < 90^\circ \tag{3.4}$$

Meanwhile, if fault occurs at F_2 (i.e. reverse fault), the fault current, $\mathbf{I}_F$, will flow in the reverse direction through the measurement location, thus, giving negative current. Clearly, the angle of the impedance which is given by equa. (3.2) will be within -180° and -90° as shown in (3.5):

$$\textit{Reverse fault} \quad \text{when} \quad -180^\circ \le \theta_Z < -90^\circ \tag{3.5}$$

Therefore, by taking the difference between the angle of the voltage and the angle of the current, the direction of the fault can be discriminated successfully as given in (3.4) and (3.5), when three-phase balanced fault occurs.

3.4 Earth Fault Directional Property

The most frequent type of fault that occurs in power network is the single-phase-to-earth fault or also known as earth fault. Therefore, it is necessary to provide efficient protection against single-phase-to-earth fault. In the directional overcurrent protection system, the direction of the current during single-phase-to-earth fault is also crucial. Hence, it is also important to develop a technique to achieve correct directional property for single-phase-to-earth fault.

When single-phase-to-earth fault occurs, obviously the voltage and current phasors are imbalanced. Therefore, there will be significant value of zero- and negative-phase sequence components of voltage and current phasors. Consequently, the zero-phase-sequence components can be analyzed in order to determine the direction of fault in this project. The use of zero-phase-sequence is also consistent with earth-fault protection with high sensitivity.

3.4.1. PHASE-'A'-TO-EARTH FAULT

Basically, there are three cases of single-phase-to-earth fault for single circuit network: phase-'a'-to-earth, phase-'b'-to-earth and phase-'c'-to-earth fault. For the case where there is a phase-'a'-to-earth fault at location k in the network as shown in Figure 3-2, then the fault constraints are given in equas.(3.6)-(3.8):

$$\mathbf{V}_{fk}^{a} = 0 \tag{3.6}$$

$$\mathbf{I}_{fk}^{b} = 0 \tag{3.7}$$

$$\mathbf{I}_{fk}^{c} = 0 \tag{3.8}$$

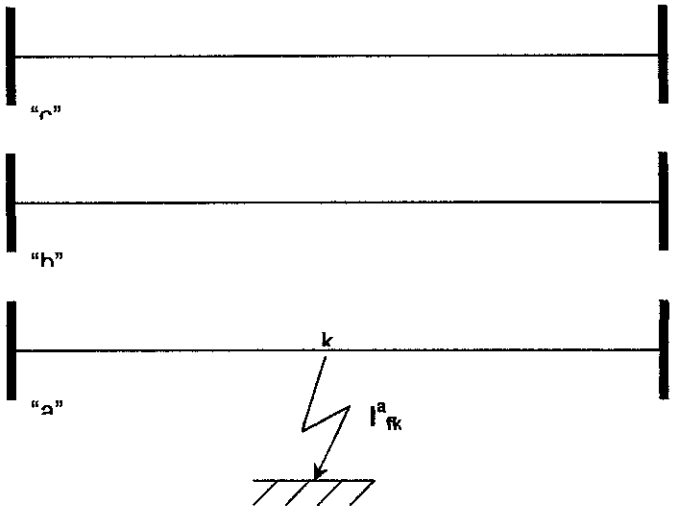

Figure 3-2: Phase-'a'-to-earth fault at location k

Transforming the fault-path currents from conductor variables to a symmetrical-phase-sequence components is done as given in equa. (3.9):

$$\begin{bmatrix} \mathbf{I}^0_{fk} \\ \mathbf{I}^1_{fk} \\ \mathbf{I}^2_{fk} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} \mathbf{I}^a_{fk} \\ \mathbf{I}^b_{fk} \\ \mathbf{I}^c_{fk} \end{bmatrix} \tag{3.9}$$

where

$$a = \exp\left\{ j\frac{2\pi}{3} \right\} \tag{3.10}$$

Substituting equas. (3.7) and (3.8) into (3.9):

$$\begin{bmatrix} \mathbf{I}^0_{fk} \\ \mathbf{I}^1_{fk} \\ \mathbf{I}^2_{fk} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} \mathbf{I}^a_{fk} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} \tag{3.11}$$

Therefore:

$$\mathbf{I}^0_{fk} = \mathbf{I}^1_{fk} = \mathbf{I}^2_{fk} = \frac{1}{3}\mathbf{I}^a_{fk} = \mathbf{I}_{fk} \tag{3.12}$$

Similarly, the fault voltages at fault location k is transform from phase-variables to symmetrical-phase-sequence components. This gives equas. (3.13)-(3.15):

$$\mathbf{V}_{fk}^{0} = \frac{1}{3}\left[\mathbf{V}_{fk}^{b} + \mathbf{V}_{fk}^{c}\right] \tag{3.13}$$

$$\mathbf{V}_{fk}^{1} = \frac{1}{3}\left[a\mathbf{V}_{fk}^{b} + a^{2}\mathbf{V}_{fk}^{c}\right] \tag{3.14}$$

$$\mathbf{V}_{fk}^{2} = \frac{1}{3}\left[a^{2}\mathbf{V}_{fk}^{b} + a\mathbf{V}_{fk}^{c}\right] \tag{3.15}$$

Taking the sum of all sequences component give us zero as shown in equa. (3.16).

$$\mathbf{V}_{fk}^{1} + \mathbf{V}_{fk}^{2} + \mathbf{V}_{fk}^{0} = 0 \tag{3.16}$$

Thus, the relationships in equas (3.12) and (3.16) can be interpreted by interconnecting the symmetrical components networks as shown in Figure 3-3.

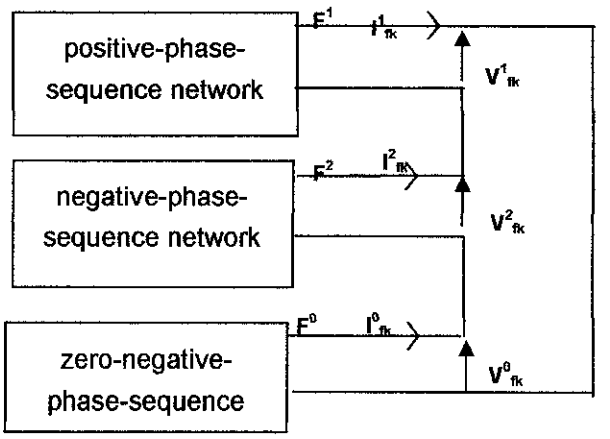

Figure 3-3: Interconnection of sequence networks at fault location k in single-phase-to-earth fault on phase 'a' [2]

The zero-phase-sequence equivalent network is modeled in detail as shown in Figure 3-4.

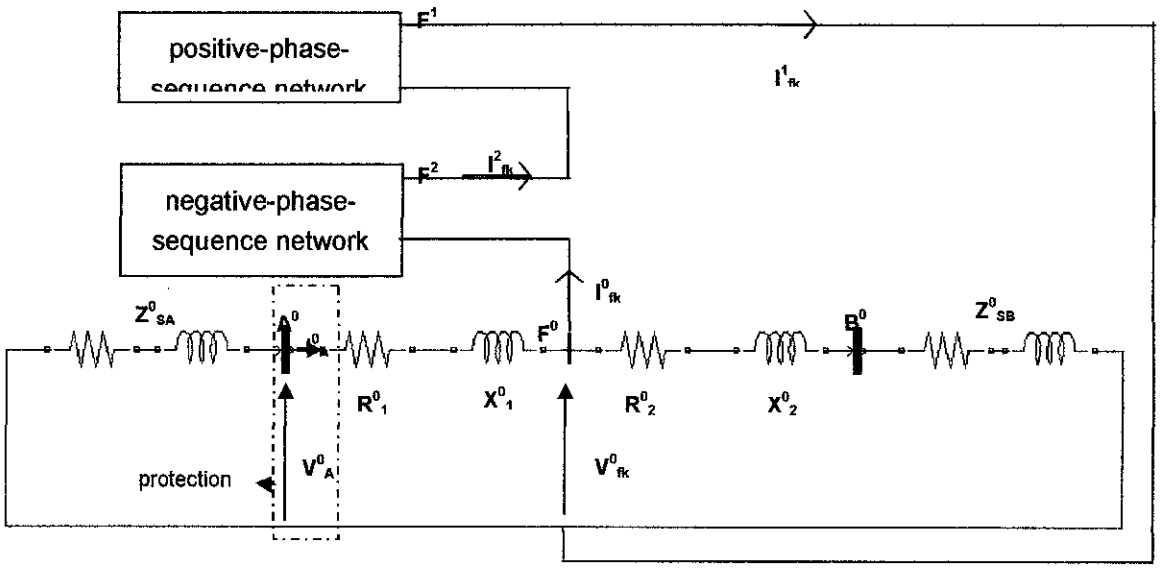

Figure 3-4: Zero-phase-sequence equivalent network and interconnection of sequence networks at fault location k in single-phase-to-earth fault on phase 'a' for forward fault

There are no voltage sources in the zero-phase-sequence network. The only input to the zero-phase-sequence network is the zero-phase-sequence fault current at the fault location. There are also $\mathbf{Z^0_{SA}}$ and $\mathbf{Z^0_{SB}}$ which are the equivalent zero-phase-sequence source impedances of sources A and B respectively.

For forward fault, the zero-phase-sequence equivalent network and interconnection of sequence networks at the fault location k in phase-'a'-to-earth fault, is shown in Figure 3-4. In this analysis, the location of protection is taken at busbar A. In zero-phase-sequence busbar A is denoted as A_0. The voltage and current phasors measured at the protection location are denoted by V_A and I_A respectively. By symmetrical

phase-sequence transformation, zero-phase-sequence components of voltage and current phasors denoted by V_A^0 and I_A^0 respectively is obtained. Hence, from Figure 3-4, equas. (3.17) and (3.18), can be derived:

$$\mathbf{V}_{\mathbf{A}}^{\mathbf{0}} = \mathbf{V}_{\mathbf{fk}}^{\mathbf{0}} + (R_1^0 + jX_1^0)\mathbf{I}_{\mathbf{A}}^{\mathbf{0}} \tag{3.17}$$

$$\mathbf{V}_{\mathbf{A}}^{\mathbf{0}} = -(\mathbf{Z}_{SA}^{0})\mathbf{I}_{\mathbf{A}}^{\mathbf{0}} \tag{3.18}$$

However equa. (4.17) is useless for determining the direction of fault because zero-phase-sequence fault voltage $\mathbf{V}_{\mathbf{fk}}^{\mathbf{0}}$ is not available. Rather equa. (3.18) can be used to distinguish the direction of fault. Rearranging equa. (3.18) gives:

$$\frac{\mathbf{V}_{\mathbf{A}}^{\mathbf{0}}}{\mathbf{I}_{\mathbf{A}}^{\mathbf{0}}} = -(\mathbf{Z}_{SA}^{0}) \tag{3.19}$$

Meanwhile, it is known that:

$$(\mathbf{Z}_{SA}^{0}) = Z_{SA}^{0}\angle\theta_{SA}^{0} \tag{3.20}$$

In power system, the impedance angle, θ_{SA}^{0}, is given by:

$$0^o \le \theta_{SA}^{0} < 90^o \tag{3.21}$$

Nevertheless, from equa. (4.43) we have $-\mathbf{Z}_{SA}^{0}$, thus we should have $\theta_{SA}^{0}{}'$ which is given by (3.22):

$$-180^o \le \theta_{SA}^{0}{}' < -90^o \tag{3.22}$$

Similar analysis is done for the fault in reverse direction to see the difference between the two cases. Thus, the zero-phase-sequence equivalent network and interconnection of sequence networks at the fault location k in phase-'a'-to-earth fault for reverse fault is illustrated as shown in Figure 3-5.

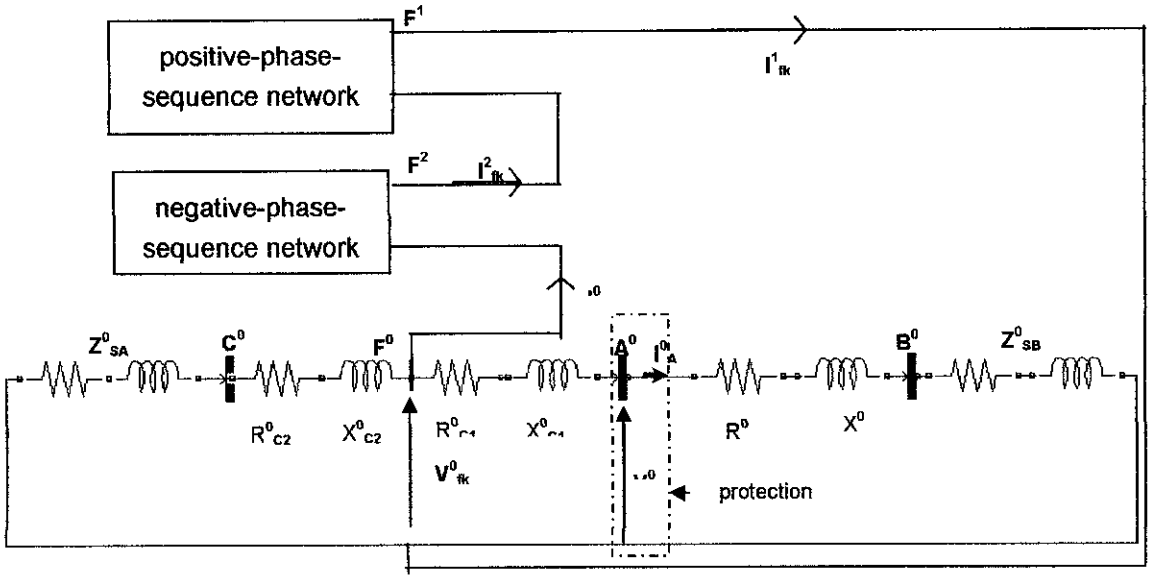

Figure 3-5: Zero-phase-sequence equivalent network and interconnection of sequence networks at fault location k in single-phase-to-earth fault on phase 'a' for reverse fault

From Figure 3-5 equa. (3.23) can be obtained:

$$\mathbf{V}_{\mathrm{A}}^{0} = (R^{0} + jX^{0})\mathbf{I}_{\mathrm{A}}^{0} + \mathbf{Z}_{SB}^{0}\mathbf{I}_{\mathrm{A}}^{0} \tag{3.23}$$

Rearranging equa. (3.23) gives equa. (3.24):

$$\mathbf{V}_{\mathrm{A}}^{0} = (R^{0} + jX^{0} + \mathbf{Z}_{SB}^{0})\mathbf{I}_{\mathrm{A}}^{0} \tag{3.24}$$

Hence:

$$\frac{\mathbf{V}_{\mathrm{A}}^{0}}{\mathbf{I}_{\mathrm{A}}^{0}} = (R^{0} + jX^{0} + \mathbf{Z}_{SB}^{0}) = \mathbf{Z}_{\mathrm{T}}^{0} \tag{3.25}$$

where $$\mathbf{Z}_{\mathrm{T}}^{0} = Z_{T}^{0}\angle\theta_{T}^{0} \tag{3.26}$$

In power system:

$$0^{o} \le \theta_{T}^{0} < 90^{o} \tag{3.27}$$

From (3.22) for forward fault and (3.27) for reverse fault, the direction of the fault can be obviously distinguished by calculating the angle of the impedance in zero-phase-sequence component.

Knowing that:

$$\mathbf{V}_{\mathbf{A}}^{\mathbf{0}} = V_A^0 \angle\theta^0{}_{VA} \tag{3.28}$$

and

$$\mathbf{I}_{\mathbf{A}}^{\mathbf{0}} = I_A^0 \angle\theta_{IA}^0 \tag{3.29}$$

Moreover, from equas. (3.22) and (3.27), $(\theta_{SA}^0)'$ and θ_T^0 is actually can be calculated by the same equation. Denoting the angle calculated as θ_Z^0, therefore:

$$\theta_{\mathbf{Z}}^{\mathbf{0}} = \theta_{VA}^0 - \theta_{IA}^0 \tag{3.30}$$

As a result, the direction of fault can distinguish by calculating the difference between the angle of zero-phase-sequence voltage and the angle of zero-phase-sequence current. If the fault is in the forward direction, the angle calculated will be within -180° and -90°. Meanwhile, if the fault is a reverse fault, the angle will be within 0° and 90°. Therefore, the directional discrimination property can be achieved for phase-'a'-to-earth fault which is summarized in (3.31) and (3.32).

$$\textit{Forward fault} \quad \text{when} \quad -180^\circ \le \theta_Z^0 < -90^\circ \tag{3.31}$$

$$\textit{Reverse fault} \quad \text{when} \quad 0^\circ \le \theta_Z^0 < 90^\circ \tag{3.32}$$

3.4.2. PHASE-'B'-TO-EARTH FAULT

For the case where there is a phase-'b'-to-earth fault at location k in the network, the constraints are given in equas.(3.33)-(3.34):

$$\mathbf{V}_{fk}^{b} = 0 \tag{3.33}$$

$$\mathbf{I}_{fk}^{a} = 0 \tag{3.34}$$

$$\mathbf{I}_{fk}^{c} = 0 \tag{3.35}$$

Symmetrical-phase sequence transformation gives:

$$\mathbf{I}_{fk}^{0} = \frac{1}{3}\left[\mathbf{I}_{fk}^{b}\right] \tag{3.36}$$

$$\mathbf{I}_{fk}^{1} = \frac{1}{3}\left[a\mathbf{I}_{fk}^{b}\right] = a\mathbf{I}_{fk}^{0} \tag{3.37}$$

$$\mathbf{I}_{fk}^{2} = \frac{1}{3}\left[a^{2}\mathbf{I}_{fk}^{b}\right] = a^{2}\mathbf{I}_{fk}^{0} \tag{3.38}$$

From equas. (3.36)-(3.38):

$$\mathbf{I}_{fk}^{0} = a^{2}\mathbf{I}_{fk}^{1} = a\mathbf{I}_{fk}^{2} \tag{3.39}$$

Meanwhile, for fault voltage:

$$\begin{bmatrix} \mathbf{V}_{fk}^{a} \\ \mathbf{V}_{fk}^{b} \\ \mathbf{V}_{fk}^{c} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^{2} & a \\ 1 & a & a^{2} \end{bmatrix} \begin{bmatrix} \mathbf{V}_{fk}^{0} \\ \mathbf{V}_{fk}^{1} \\ \mathbf{V}_{fk}^{2} \end{bmatrix} \tag{3.40}$$

Thus:

$$\mathbf{V}_{fk}^{b} = \mathbf{0} = \mathbf{V}_{fk}^{0} + a^{2}\mathbf{V}_{fk}^{1} + a\mathbf{V}_{fk}^{2} \tag{3.41}$$

Then, the relationships in equas.(3.39) and (4.41) can be interpreted by interconnecting the symmetrical components networks as shown in

Figure 3-6.

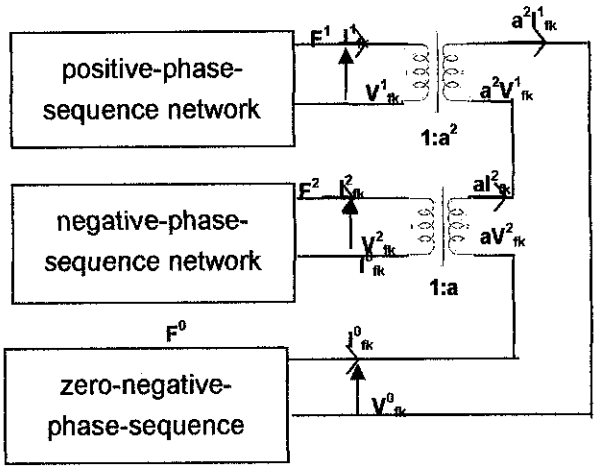

Figure 3-6: Interconnection of sequence networks at fault location k in single-phase-to-earth fault on phase 'b'

Then, the same analysis as that in case with phase-'a'-to-earth fault analysis can be done for phase-'b'-to-earth fault to show that the directional property can be derived from the zero-phase-sequence components of voltage and current at the protection location. Correspondingly, the directional discrimination property for phase-'b'-to-

earth fault is exactly similar to the phase-'a'-to-earth fault which is summarized in (3.31) and (3.32).

3.4.3. PHASE-'C'-TO-EARTH FAULT

Furthermore, for the case where there is a phase-'c'-to-earth fault at location k in the network, then the constraints are given in equas.(3.42)-(3.44):

$$\mathbf{V}_{fk}^{c} = 0 \tag{3.42}$$

$$\mathbf{I}_{fk}^{a} = 0 \tag{3.43}$$

$$\mathbf{I}_{fk}^{b} = 0 \tag{3.44}$$

Symmetrical-phase sequence transformation gives:

$$\mathbf{I}_{fk}^{0} = \frac{1}{3}\left[\mathbf{I}_{fk}^{c}\right] \tag{3.45}$$

$$\mathbf{I}_{fk}^{1} = \frac{1}{3}\left[a^{2}\mathbf{I}_{fk}^{c}\right] = a^{2}\mathbf{I}_{fk}^{0} \tag{3.46}$$

$$\mathbf{I}_{fk}^{2} = \frac{1}{3}\left[a\mathbf{I}_{fk}^{c}\right] = a\mathbf{I}_{fk}^{0} \tag{3.47}$$

From equas. (3.45)-(3.47):

$$\mathbf{I}_{fk}^{0} = a\mathbf{I}_{fk}^{1} = a^{2}\mathbf{I}_{fk}^{2} \tag{3.48}$$

Meanwhile, for fault voltage:

$$\mathbf{V}_{fk}^{c} = \mathbf{0} = \mathbf{V}_{fk}^{0} + a\mathbf{V}_{fk}^{1} + a^{2}\mathbf{V}_{fk}^{2} \tag{3.49}$$

Therefore, from equas. (3.48) and (3.49) for phase-'c'-to-earth fault, the interconnection of the symmetrical component networks is as shown in Figure 3-7.

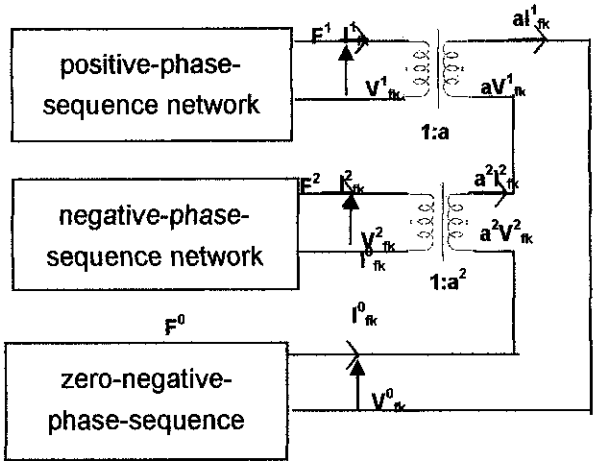

Figure 3-7: Interconnection of sequence networks at fault location k in single-phase-to-earth fault on phase 'c'

Similarly, the analysis for phase-'a'-to-earth fault is also applied to phase-'c'-to-earth fault and produces the same directional property as that in (3.31) and (3.32).

CHAPTER 4
RESULTS AND DISCUSSION

4.1. SIMULATION CIRCUIT

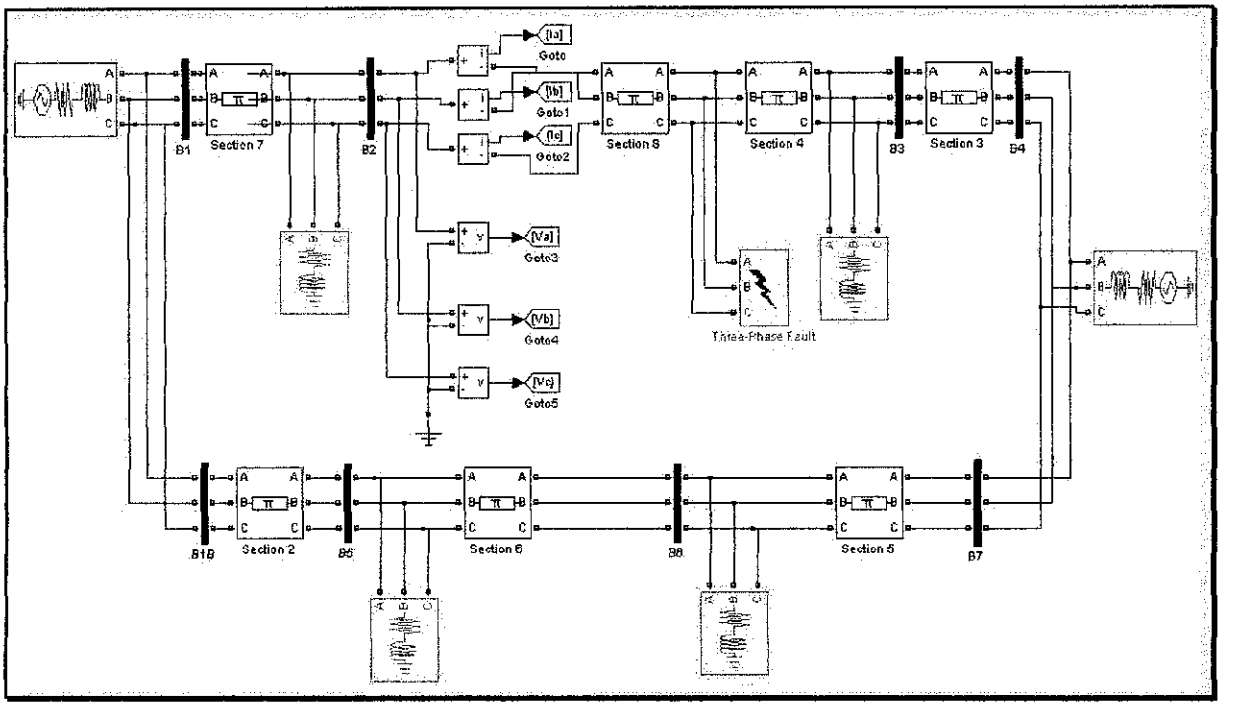

Figure 4-1: Shows the simulation circuit diagram of the parallel distribution system for three-phase fault

The diagram above showing on the connection of the parallel distribution system, which consist of two generators, eight busbar in parallel, loads and the type of fault that has been set early. The line section lengths for each Three-Phase PI Section Line have been set to 50km and can be change depends on the analysis required. Frequency during transmit this voltage are set to 60Hz. The details for a few types of blocks are shown below:

Table 4-1: Shows the Three-Phase PI Section Line

	Criterion	Value
1	Frequency used for RLC specification (Hz)	60
2	Line section length (km)	50
3	Positive-sequence and zero-sequence resistances (Ohms/km) [R1 R0]	[0.01273 0.3864]
4	Positive-sequence and zero-sequence inductances (Ohms/km) [L1 L0]	[0.9337e-3 4.1264e-3]
5	Positive-sequence and zero-sequence capacitances (Ohms/km) [C1 C0]	[12.74e-9 7.751e-9]

Table 4-2: Shows the Three-Phase Source 11kv 100MVA and 132kV 100MVA.

	Criterion	Value
1	Phase-to-phase rms voltage (V)	132e3
2	Phase angle of phase A (degree)	0
3	Frequency (Hz)	50
4	Internal Connection	Yg
5	Source Resistance (Ohms)	25^2/1000/10
6	Source Inductance (H)	25^2/1000/377

Table 4-3: Shows the Three-Phase Fault

	Criterion	Value
1	Fault resistance	0.0001
2	Ground resistance	0.001
3	Transition Status	[1 0]
4	Transition Times	[0.3 0.5]
5	Snubbers Resistance Rp (Ohms)	inf
6	Snubbers Capacitance Cp (Farad)	inf

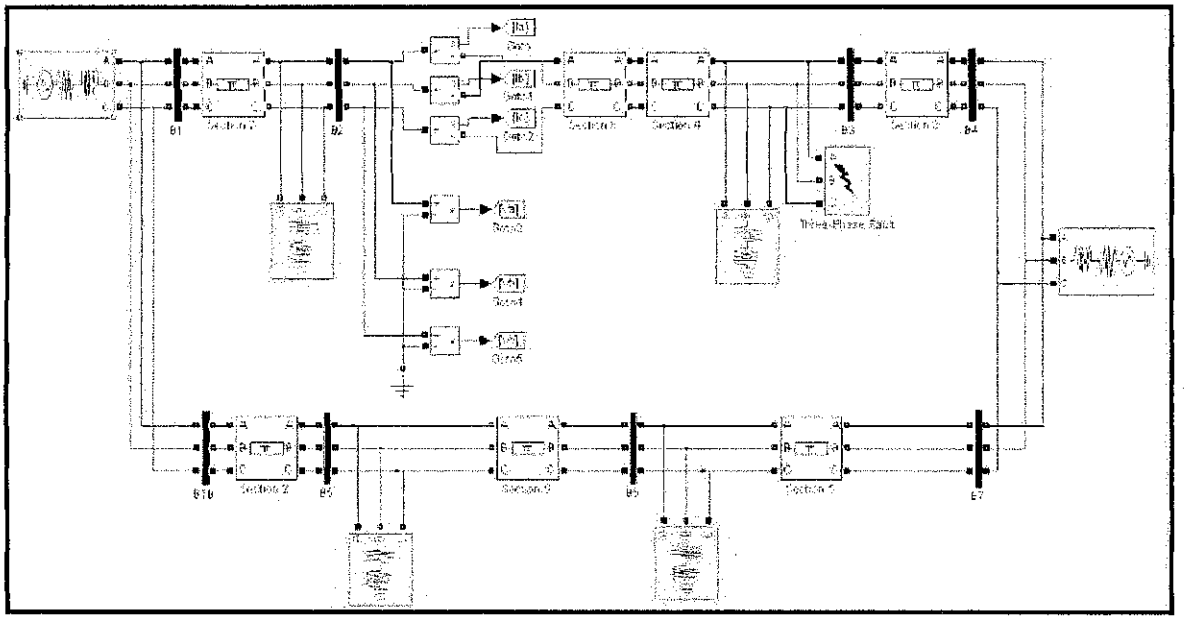

Figure 4-2: Shows the simulation circuit diagram of the parallel distribution system for close-up fault

Based on Figure 4-2, close-up fault is the same as three-phase fault, but the different is in term of location of the fault itself. This type of fault normally occurred near to the busbar.

4.2. RESULTS

Table 4-4: Results are base on type of faults

	Type of Faults	Forward Direction (°)	Reverse Direction (°)
1	Phase-to-phase fault.		
	Distance: 10km	87.4	-92.7
	50km	87.5	-93
	100km	87.5	-93
2	Earth Fault:		
	Distance: 10km	-178.3	87.8
	50km	-178.4	87.5
	100km	-178.3	87.6

4.3. DISCUSSION

Results achieved here basically are within the range. For the phase-to-phase fault, the range for forward direction is mainly around $0^{\circ} \leq \theta_z < 90^{\circ}$. θ_z is derived from the basic equation (2.28), where is value of voltage divided with value of current. And for voltage phase angel θ_v, will minus current phase angle θ_i to get the impedance phase angle, θ_z. The result from the minus equation must be positive 0° to positive 90°, but for the reverse direction of fault the degree are not the same. The range of impedance angle for the reverse is normally within $-180^{\circ} \leq \theta_Z < -90^{\circ}$. This because θ_i is much smaller than θ_v when the fault occurred in reverse direction for phase-to-phase fault.

Based on the table, results are almost the same whether the system is increased it distance of fault or not. This shown that distance cannot give an influence to the value of impedance angle, and how far the fault occurred from the circuit breaker the system can detect and discriminate it.

Earth fault occurred when one connection out of three phases is short circuit to ground. The range for forward direction is $-180^{\circ} < \theta_z^{o} < -90^{\circ}$, while for the reverse direction is $0^{\circ} \leq \theta_z < 90^{\circ}$. Data result those obtained, are all within the range, meaning that the algorithm derived in chapter 2 are proven and meet the result expectation. On the other hand, distance not a significant factor to affect the result, because based on three varied distance the θ_z still give a consistent value.

CHAPTER 5
CONCLUSION AND RECOMMENDATION

Drawing on the supply-frequency impedance characteristics of a power system and its responses, expressed in symmetrical-phase-sequences, to short-circuit faults, the project has developed reliable algorithms for distinguishing between forward faults and reverse faults. The particular situation of a balanced fault close-up to the protection location is catered for by using the memory voltage. Test studies for a wide range of fault operating conditions verify that the algorithms can be combined directly with that for the standard overcurrent protection to form the numerical directional overcurrent protection system. The combination of inverse-time characteristic and directional element completes the directional overcurrent protection system. Therefore, the faulty section or zone of the power system network needs to be isolated while leaving the rest of the system uninterrupted or remaining in operation following fault clearance, in this case focus on parallel line transmission.

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[2] T.T Nguyen & W. Derek Humpage, *Computer Applications in Power*, Energy Systems Centre, Department of Electrical and Electronic Engineering, The University of Western Australia, 1992, ch.4&5, pp 4.1-5.38