PC-BASED BLOOD PRESSURE AND PULSE RATE MONITORING SYSTEM

By

LAWRENCE VANDER SLOTT

DISSERTATION

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

Universiti Teknologi Petronas
Bandar Seri Iskandar
31750 Tronoh
Perak Darul Ridzuan

CERTIFICATION OF APPROVAL

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Approved:

Dr. Nazir Ahmed Arian
Project Supervisor

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK

June 2007

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Lawrence Vander Slott

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Thank you.

ABSTRACT

This report describes the application of the biomedical theory and communication theory. This project "PC Based Blood Pressure and Pulse Rate Monitoring System" is proposed as it can take the place of the conventional blood pressure monitoring systems that are currently available in the market (example: the mercury tube blood pressure monitors and electronic blood pressure monitors). The traditional method of measuring blood pressure using the mercury tube and stethoscope requires an individual who is skillful in order to get accurate measurements. The electronic blood pressure monitor makes this task much easier as a person only needs to place it on the arm and activate it. No expert personnel are needed. This project would be an update of the electronic blood pressure monitor as it would be controlled by the Personal Computer. The Personal Computer (PC) is chosen as the base platform for this project because the majority of people have PC's. A LabVIEW software interface will be used to display the readings and control the blood pressure monitor. The readings are sent to the PC from the blood pressure monitor unit via the PC Serial Port.

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INTRODUCTION

1.1 Project Background

The PC-Based Blood Pressure and Pulse Rate Monitoring System utilizes the personal computer to monitor blood pressure and pulse rate. The system is interfaced to the PC through the serial port to monitor the blood pressure and pulse rate. The pressure sensor senses these parameters and produces an analog voltage level that is amplified and digitized before the computer is able to read it.

An interface circuit is designed in order to convert the analog voltage produced by the pressure sensor to digital data using a PIC in order to allow the data to be read from the serial port. The analog to digital converter will be connected to the personal computer via the serial port.

The task of the personal computer is now to acquire the digital signals that are obtained from the serial port. The programming language that is being used in this project is LabVIEW.

1.2 Project Layout

Figure 1 shows the block diagram of the system. How the system works is the inflatable cuff is first attached to a persons arm. It is then inflated to a level above the systolic pressure so as to obstruct the movement of blood in the artery. The second tube from the inflatable cuff is attached to the nozzle of the pressure sensor. As the air is slowly released from the inflatable cuff, the pressure sensor gives a differential output voltage reading. Because the output of the pressure sensor is fairly small, it is therefore amplified by an amplifier to increase it to a legible level for processing.

After that, the signal is sent to an Analog to Digital Converter to enable the personal computer to acquire the data via serial port (RS232) to be processed and displayed on the monitor the parameters of systolic pressure, diastolic pressure and pulse rate.

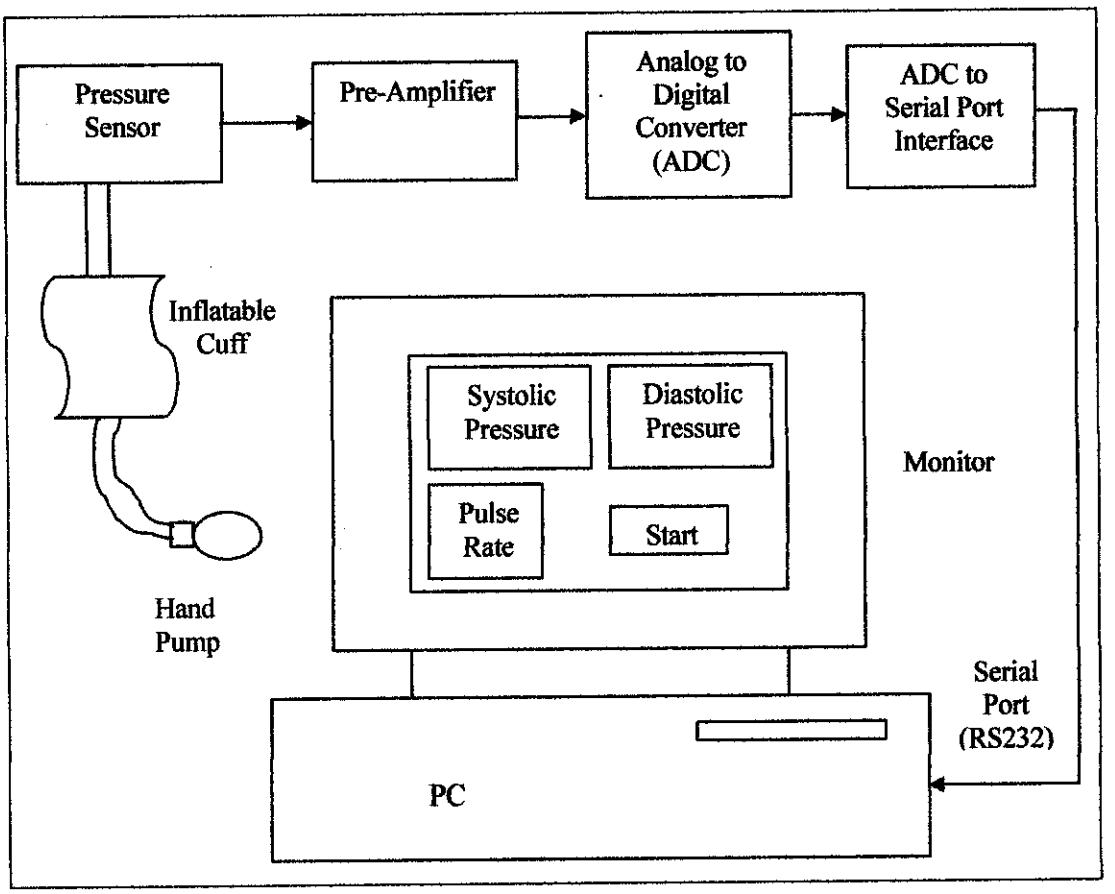

***Figure 1:** Project block diagram*

1.3 Problem Statement

The idea of using a personal computer comes from the fact that most people own computers nowadays and it would reduce the hassle of specially going to a medical center to carry out blood pressure monitoring. The relevance of monitoring blood pressure from home is because the very act of going to a medical center can increase blood pressure as it involves various activities such as driving or walking. Some people also become nervous when they enter a medical center. This is called "White Coat Syndrome". This means that blood pressure measured is unusually high in the

medical center but normal at other times [4]. The comforts of home where the mood is relaxed would be the ideal place to monitor ones blood pressure.

The design of the PC-Based Blood Pressure and Pulse Rate Monitoring System will also be a more cost effective alternative to Digital Blood Pressure Monitors as the product only involves buying of the necessary hardware components that will be interfaced to the PC by serial port. The system will be controlled and readings displayed using a programming language. As compared to a Digital Blood Pressure Monitor, costs are lower. The Digital Blood Pressure Monitor contains a small microprocessor that will carry out all the necessary calculations and readings. The costs are also elevated due to engineering costs.

1.4 Significance of Project

Blood pressure is deemed to be high when the Systolic pressure is or above 140 mm Hg and the Diastolic pressure is or above 90 mm Hg (140/90). When blood pressure increases, there is an indication that the blood flow is blocked in some way. High blood pressure has a direct link with the increase of risk for coronary heart disease (will lead to a heart attack) and also stroke when presented with other risk factors. Elevated blood pressure levels have also been known to cause kidney disease. Very often people are unaware they are suffering from it until they start suffering the side effects. This is one of the reasons why high blood pressure is called the "silent killer" [10]. It is very important for people above the age of 35 to get regular blood pressure check ups.

If detected early, hypertension can often be reversed through diet, exercise, and pharmaceuticals. This reduces the likelihood of catastrophic disease, hospitalization, and death. The most ideal scenario is to have everyone own their own personal blood pressure monitor at home to keep track of blood pressure levels.

CHAPTER 2
LITERATURE REVIEW

2.1 Measurement Concept

A medical practitioner measures blood pressure by first pumping air into the inflatable arm cuff to a level that is above the systolic level so blood flow in the artery will stop momentarily. He then uses his stethoscope and listens to the movement of blood in the patients arm. At this pressure, he hears nothing as blood is unable to move. Pressure is then slowly released, and when it reaches a certain pressure, blood begins to flow and the doctor will hear a "tapping" sound in time with the heart beat. This is the ***systolic pressure***. As the pressure is further released, the "tapping" sound slowly fades away before becoming louder again and completely disappearing. The pressure at which the sound disappears is the ***diastolic pressure.*** The sounds heard while measuring blood pressure are called the Korotkoff sounds.

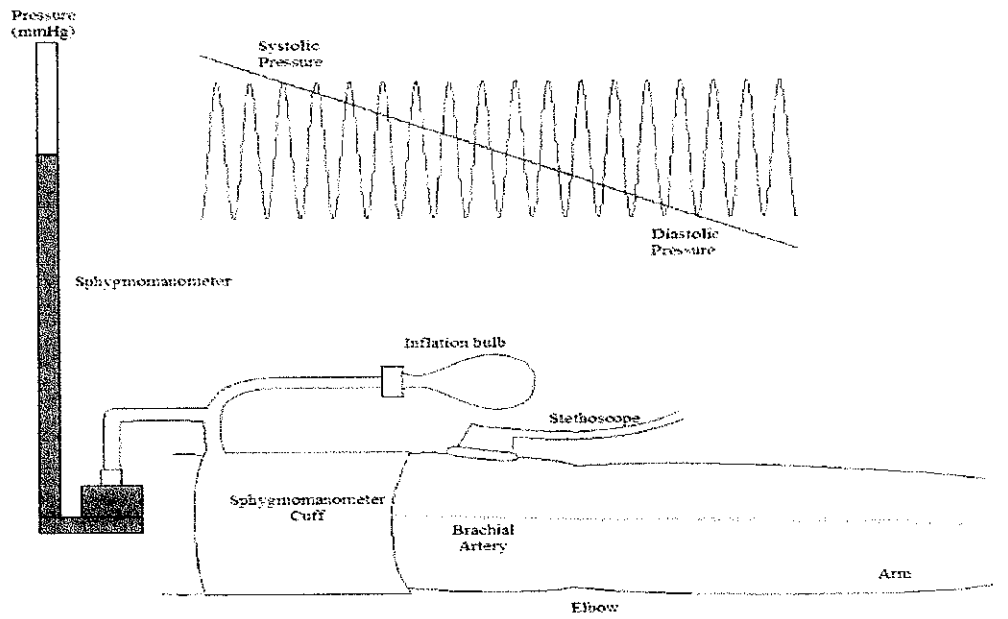

Figure 2: *Standard Blood Pressure Measurement Setup.*
Source: http://www.medphys.ucl.ac.uk

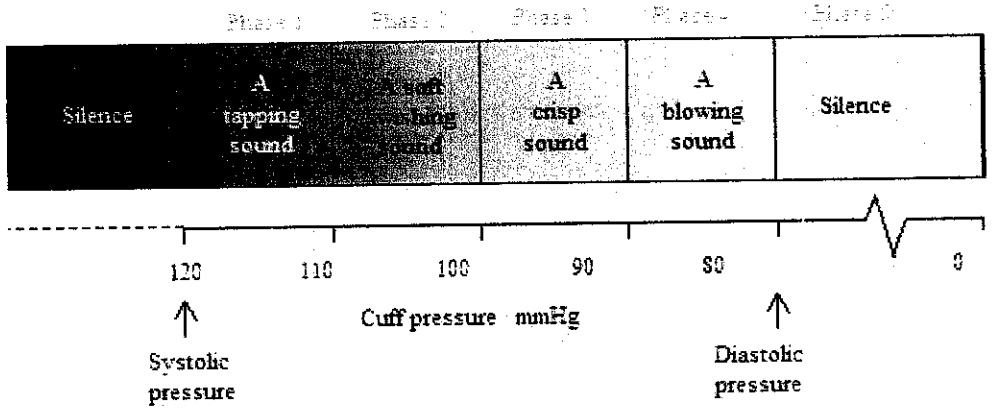

***Figure 3:** 5 Phases of Korotkoff Sounds. Source: http://www.medphys.ucl.ac.uk*

2.2 Oscillometric Measurement

The method to perform measurement for this system is by using the **"Oscillometric"** method. The term "oscillometric" refers to any measurement of the oscillations caused by the arterial pressure pulse. The air is pumped into the cuff to a value above the systolic pressure. The basic principle behind the Oscillometric Method is the measurement of the amplitude of the change in pressure as the cuff is deflated from the value above the systolic pressure. Amplitude suddenly grows larger as pulse suddenly breaks through its obstruction. The pressure at this moment is very close to the systolic pressure. As the cuff pressure is further reduced, there is a great increase in pulse amplitude where it reaches a maximum value and then would quickly diminish. The diastolic pressure is taken when the peak starts to diminish. The systolic blood pressure and diastolic blood pressure are obtained by identifying the region where there is rapid increase then decrease in the amplitude of the pulses. To sum up, the systolic pressure will be the pressure at which the pulsation starts to occur, and the diastolic pressure will be the pressure when the pulses start to disappear [1] [2].

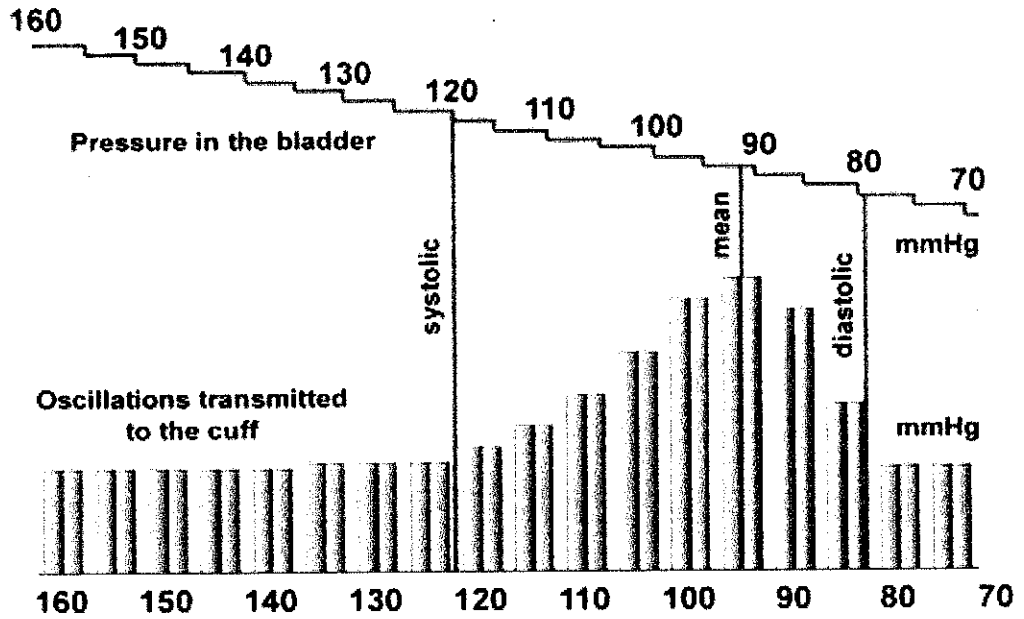

Figure 4: *Oscillation of signal obtained from the inflatable cuff [2].*

CHAPTER 3
SYSTEM DESIGN

3.1 Introduction

The overall design for the "PC Based Blood Pressure and Pulse Rate Monitoring System" is broken up into 3 modules.

I. **Module 1:** Blood Pressure Sensor Module
   Main hardware comprising of inflatable cuff, rubber bulb, pressure sensor and instrumentation amplifier.

II. **Module 2:** Analog to Digital Converter Module
   Consists of the PIC 16F877A which will be used as an Analog to Digital Converter and is connected to the serial port (RS232 D-Type 9 pin).

III. **Module 3:** Graphical User Interface Module
   Consists of the Serial Port interface and the programming language where the readings that have been obtained from the pressure sensor will be displayed on the monitor.

The system is broken up into several modules in order to simplify the order of the system development work. Figure 5 shows the block diagram of the project divided up into 3 modules.

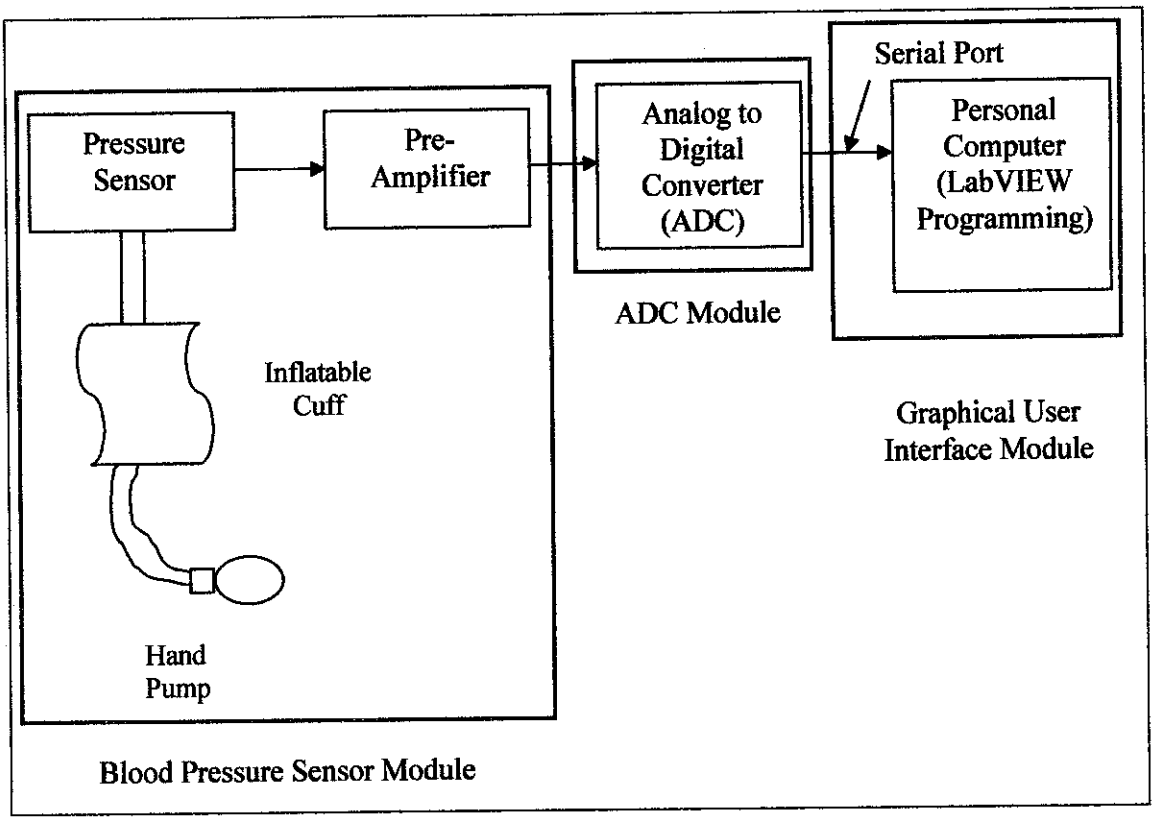

***Figure 5:** Project Divided into 3 Modules*

3.1.1 Blood Pressure Sensor Module

3.1.1-a Inflatable Cuff and Rubber Bulb

The inflatable cuff is used to restrict blood flow for blood pressure measurement. The cuff is placed around the upper arm, around the height of the heart. The inflatable cuff is filled with air by using the rubber bulb attached to it. The cuff is filled with air until the artery is completely occluded. Air is then slowly released from the cuff via the valve on the rubber bulb. The second tube on the inflatable cuff is attached to the pressure sensor.

3.1.1-b Pressure Sensor

The pressure sensor chosen for this project is a Motorola MPX50GP. This pressure sensor is a silicon piezoresistive pressure sensor that provides accurate and linear voltage outputs that are proportional to the pressure applied. How this works is when pressure is applied to the piezoresistive material, it either stretches or compresses. When the piezoresistive material becomes deformed, it generates electrical charges with one face becoming negatively charged and the other face becoming positively charged. The net charge q on a surface is proportional to the amount x by which the charges have been displaced given by the equation $q = kx = SF$, where F is the applied force, k is a constant and S a constant termed the charge sensitivity. The voltage induced is proportional to the applied pressure [6]. A tube from the cuff is attached to the nozzle of the pressure sensor. This way, the changes in pressure in the cuff will be directly proportional to the output voltage from the pressure sensor.

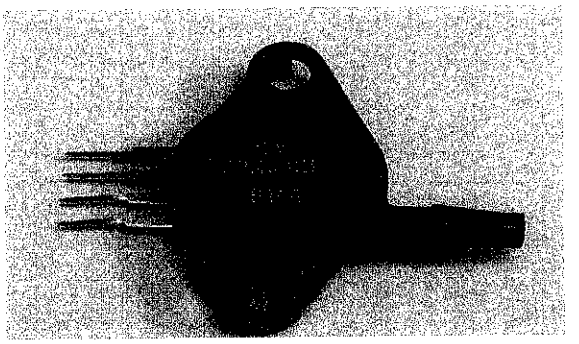

Figure 6: *Motorola MPX50GP Pressure Sensor*

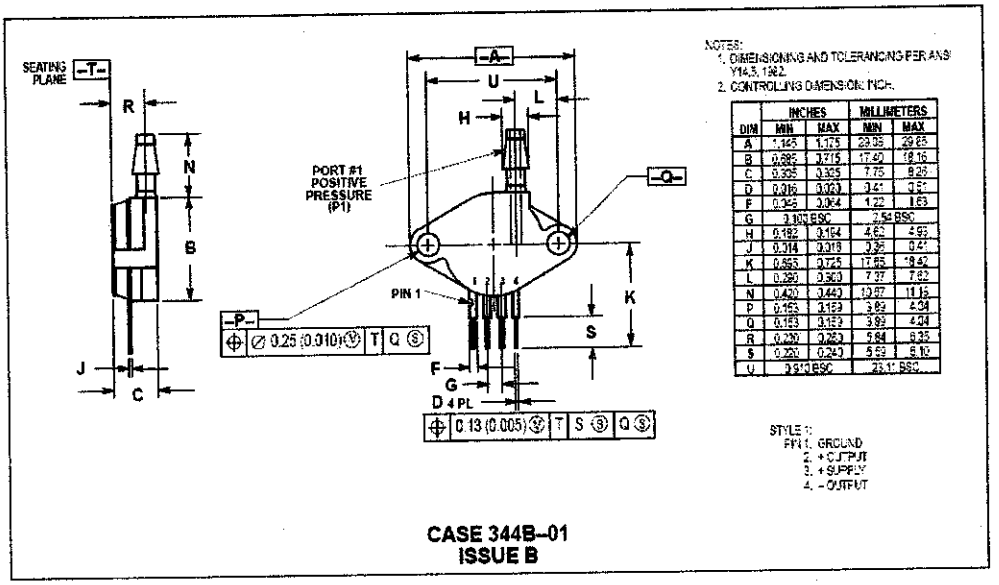

***Figure 7:** Motorola MPX50GP Pressure Sensor Dimensions [6]*

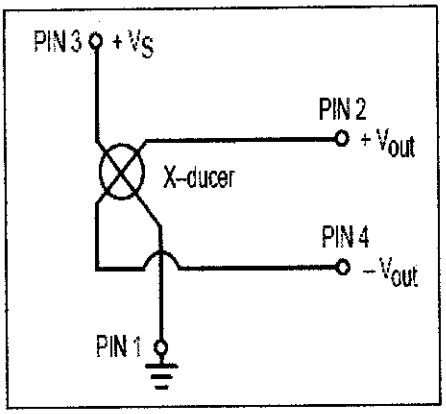

***Figure 8:** Uncompensated Pressure Sensor Schematic [6]*

PIN NUMBER			
1	Gnd	3	V_S
2	$+V_{out}$	4	$-V_{out}$

***Table 1:** Pin Configuration*

3.1.1-c Pre-Amplifier.

The pressure sensor that is being used produces a very low voltage (18mV to 60mV), so the signal needs to be amplified for legible readings. An instrumentation amplifier is the best type of amplifier to be used for signal processing application. An instrumentation amplifier is a type of differential amplifier that is specially designed to have characteristics suitable for measurement and test equipment. Among the characteristics are low DC offset, low noise, high open loop gain, and high input impedance.

Instrumentation amplifiers can be made using the traditional 2 or 3 op amp design or using a single dedicated designed amplifier. The amplifier chosen for the project is a single dedicated IC chip from Analog Devices. The reason why a single dedicated IC amplifier is chosen is because it gives a clean and low error signal which is important for obtaining a proper value. The model chosen is the AD620 Instrumentation Amplifier from Analog Devices. This amplifier is a high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 10,000 [11]. G here in this context refers to "gain" or the amplification value of the amplifier. The term gain refers to the value of the output voltage/input voltage ratio. Gain does not have any unit of measurement. R_G refers to the "gain resistor". This resistor is used to determine the gain of the amplifier by the equation:

$$G = \frac{49.4k\Omega}{R_G} + 1$$

For a specific value of Gain or *G*, the value of the gain resistor can be determined by the equation:

$$R_G = \frac{49.4k\Omega}{G-1}$$

CONNECTION DIAGRAM

8-Lead Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages

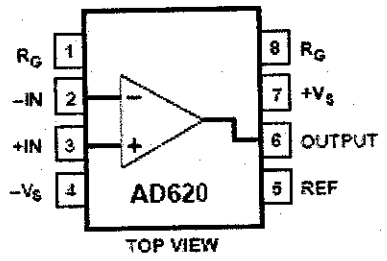

Figure 9: *Pin layout of AD620 [7]*

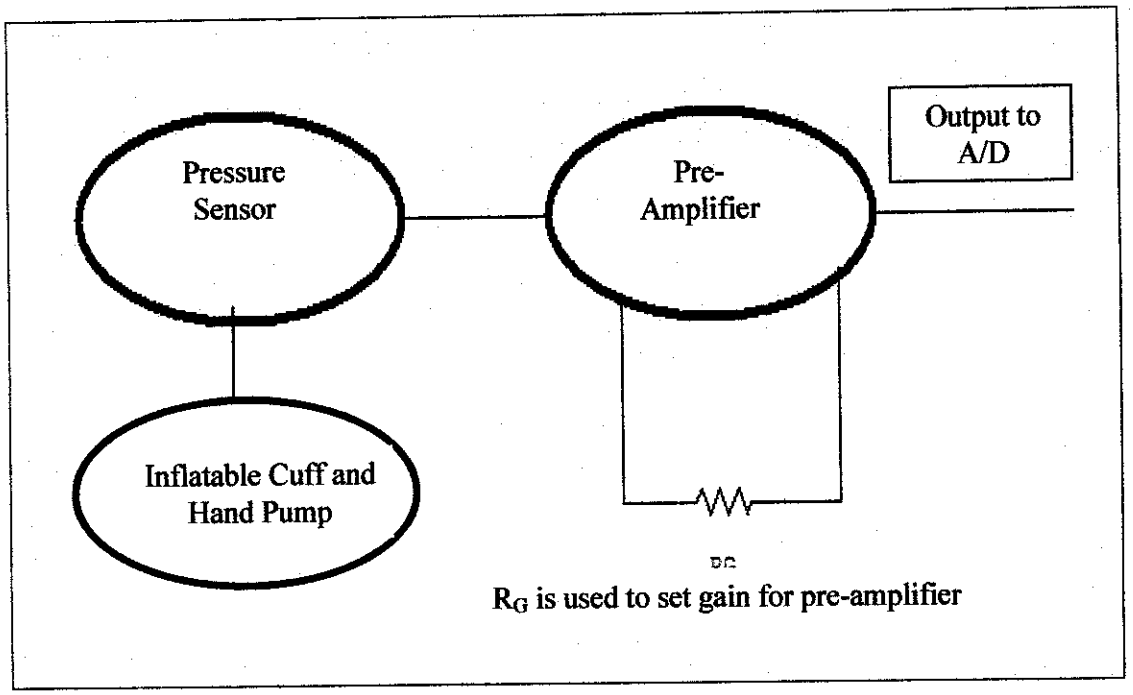

Figure 10: *Block diagram for Blood Pressure Sensor Module*

3.1.2 Analog-to-Digital Converter Module

3.1.2-a Introduction to Analog to Digital Conversion

Real world signals outside the computer exist in an analog form. A computer is not able to read these analog values and must therefore be converted into digital or binary form that consists of "0" and "1". An analog to Digital Converter (ADC) converts the analog voltage value to a digital number. The output of an ADC is a quantized representation of the original analog signal. Quantization refers to the process of approximating a range of values to a finite set of values, or in other words to round off the value. Quantization error is an inaccuracy that can occur as a result of this.

Resolutions define the number of possible analog to digital converter output states. For an 8 bit converter, there are a total of 256 possible states (0 to 255). The higher the resolution an ADC has the less quantization error occurs because the range of values are divided into smaller steps.

3.1.2-b PIC16F877A as Analog to Digital converter

The PIC16F877A is a powerful microcontroller that can be used for many purposes. The PIC16F877A has a large program memory for storing written programs and it can be cleared more than once. These features make it an ideal tool for system development. The PIC also has an EEPROM data memory that is used for storing data that must not be lost if there is a sudden interruption of the supply. Other features include RAM, free run timer and CPU. RAM is the data memory used during execution of a program while the CPU plays an important role of coordinating work of other blocks an also executes the users program.

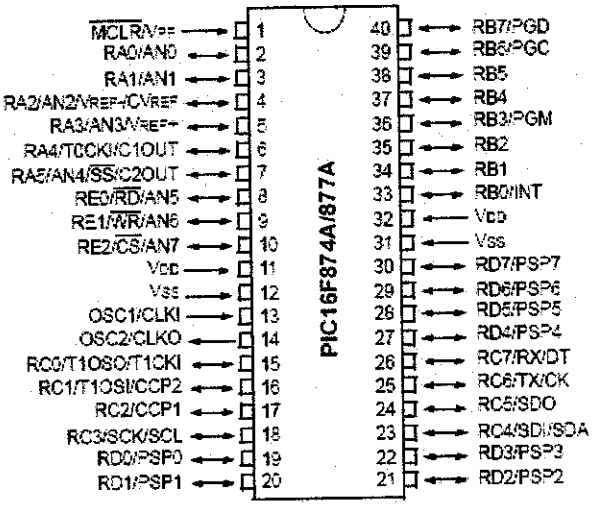

***Figure 11:** PIC16F877A Connection Diagram [5]*

The microcontroller can perform a lot of applications and one of them is analog to digital conversion. The ADC is used to convert analog data to digital data so it can be fed into the computer. Several steps need to be taken in order to setup the microcontroller as an ADC. First the I/O pins that will be used for the analog to digital conversion need to be configured as analog inputs. The next step is to select the channels for conversion and the modules are configured and enabled. A delay for acquisition time is provided after which the conversion is initiated. Once conversion is completed, the output signal can be read.

3.1.2-b-i PIC16F877A Pin-Out Description

The PIC16F877A has a total of 40 pins. There are a few different configurations such as PDIP (Plastic Dual In-line Package), TQFP (Thin Quad Flat Pack), MQFP (Metric Quad Flat Pack) and PLCC (Plastic Leaded Chip Carrier). For the project, the 40 pin PDIP version will be used. The table below shows the descriptions of the pins for the 16F877A.

PIN NAME	PIN NUMBER	DESCRIPTION
OSC1/CLKIN	13	Oscillator crystal or external clock input
OSC2/CLKOUT	14	Oscillator crystal or clock output.

		Connects to crystal or resonator in crystal oscillator mode.
MCLR/VPP	1	Master Clear (Reset) input or Programming voltage input. This pin is an active low RESET to the device.
PORT A	2, 3, 4, 5, 6, 7	PORT A is a bidirectional I/O port.
PORT B	33, 34, 35, 36, 37, 38, 39, 40	PORT B is a bidirectional I/O port. PORT B can be software programmed for internal weak pull-up on all inputs
PORT C	15, 16, 17, 18, 23, 24, 25, 26	PORT C is a bidirectional I/O port.
PORT D	19, 20, 21, 22, 27, 28, 29, 30	PORT D is a bidirectional I/O port or parallel slave port when interfacing to a microprocessor bus.
PORT E	8, 9, 10	PORT E is a bidirectional I/O port.
VSS	12, 31	Ground reference for logic and I/O pins.
VDD	11, 32	Positive supply for logic and I/O pins.

Table 2: *PIC16F877A Pin-Out [5]*

3.1.2-c MAX232 Chip

In order for data to be transmitted serially via the serial port, it is necessary to be able to communicate serially. The MAX232 is one of the chips contained in the family of line drivers and receivers that is intended for protocol EIA/TIA-232E communication interfaces. The MAX232 is especially useful to be used in low powered systems and power dissipation of less than 5μW can be achieved [12].

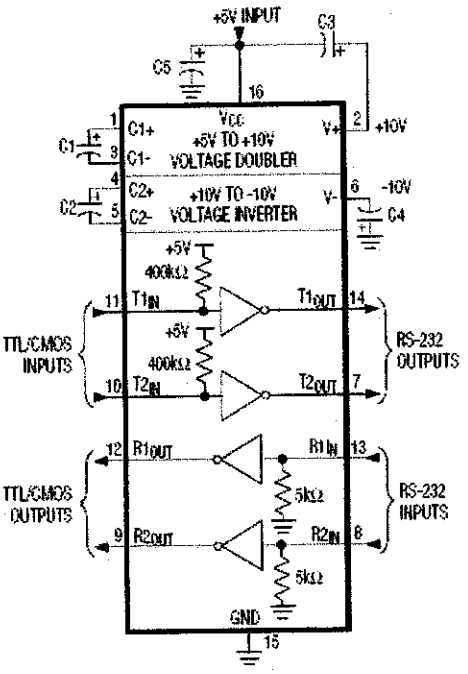

Figure 12: Internal View of MAX232 Chip [12]

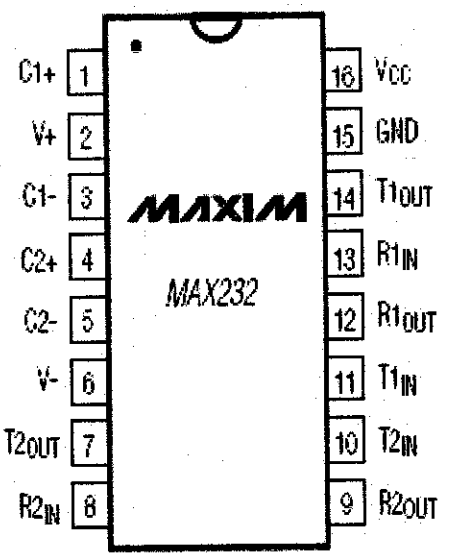

Figure 13: Pin Layout of MAX232 Chip [12]

3.1.3 PC-Serial Port Interface and Graphical User Interface Module

3.1.3-a Serial Port

3.1.3-a-i Introduction

Currently the most common used serial port for transmitting data and communication interfaces is the RS-232. It is found on almost all desktop systems. The serial port is harder to program compared to the parallel port but requires less hardware and wiring, thus cost is significantly reduced. In order to carry out communication using the serial port, only 3 data lines need to be used that is TxD (transmit data), RxD (receive data) and Ground (common ground). The reduced cost makes the serial port an excellent and effective method for data transmission [11].

The RS-232 connection to be used is the D-type 9 pin (DB 9) which is the most common. It was originally a 25 pin configuration (DB 25). But for simple standard communications, only pins 1 through to 8 and pin 20 are important. Thus IBM developed the D-type 9 pin configuration which is found on most computer systems.

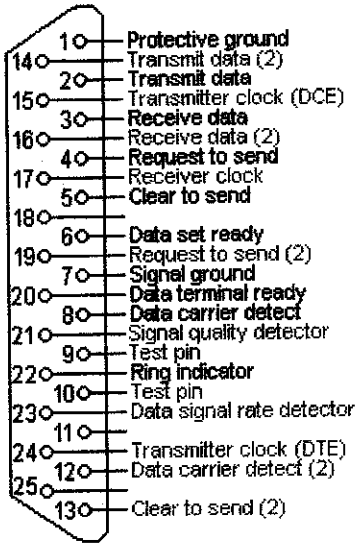

Figure 14: *DB 25 Serial Port [11]*

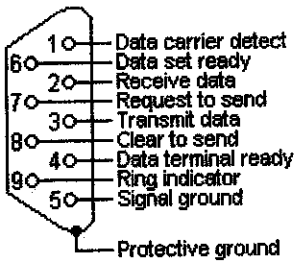

Figure 15: *DB 9 Serial Port [11]*

Serial data communication has a number of advantages compared to parallel data communication. The length of serial cables can be longer compared to parallel data cables without significant signal loss. The serial port transmits "1" as -3 to -25 volts and "0" as +3 to +25 volts. The parallel port transmits "0" as 0 volts and "1" as 5 volts. Thus the serial port has a maximum swing of 50 volts compared to the parallel port which has a maximum swing of only 5 volts. Microcontrollers (such as the PIC16F877A used in the project) have built in Serial Communication Interfaces (SCI) that is used to communicate. The use of serial communication greatly reduces the pin count for microprocessor units. Only two pins are used for data communication which is the TxD (Transmit Data) and RxD (Receive Data) pins compared to the use of 8 pins for an 8 bit parallel communication method.

3.1.3-a-ii Serial Port Hardware Properties

There are two categories in which serial communication is split into, Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). Data Communication Equipment refers to devices such as modems, adapters and plotters. Data Terminal Equipment refers to equipment like a computers and data terminals.

The electrical specifications of serial ports are contained in the Electronics Industry Association (EIA) RS232 standard. The following are some of the parameters that are included:

- A "space" (logic 0) is between +3 volts and +25 volts.
- A "mark" (logic 1) is between -3 volts and -25 volts.
- The region between -3 volts and +3 volts is undefined.
- An open circuit voltage should never exceed 25 volts (in reference to GND).
- A short circuit current should not exceed 500 mA. The driver should be able to handle this without damage.

The serial port has two sizes which is the D-Type 25 pin connector and the D-Type 9 pin connector which come in male configuration on the back of the PC. The connector that is being used in the project is the D-Type 9 pin. Below is the description of the pins in the D-Type 9 pin serial port:

Pin No.	Pin Outs	Function
1	DCD	Data Carrier detect (This line is active when modem detects a carrier)
2	RXD	Receive Data (Serial data input)
3	TXD	Transmit Data (Serial data output)
4	DTR	Data Terminal Ready
5	GND	Signal ground
6	DSR	Data ready state (UART establishes a link)
7	RTS	Request to send (acknowledge to modem that UART is ready to exchange data)
8	CTS	Clear to send (modem is ready to exchange data)
9	RI	Ring Indicator (Becomes active when modem detects ringing signal from PSTN)

***Table 3:** DB 9 Serial Port Pin Functions [11]*

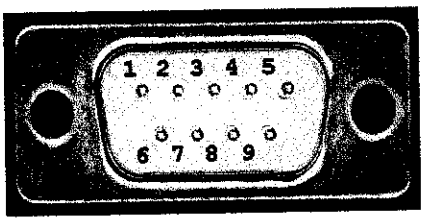

Figure 16: DB 9 Male connector fitted on PC [11]

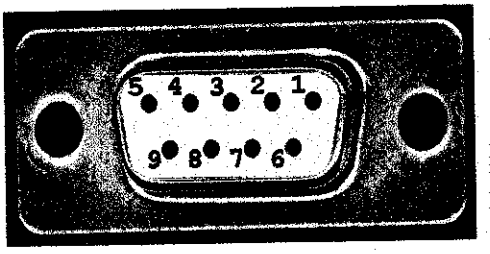

Figure 17: DB 9 Female connector, found on plug to be connected to PC [11]

Although there are many data pins on the serial port, all of them are only necessary if communication between PC's or terminals need to take place involving continuous data transfer. For simple data transfers that involve just inputs and outputs of voltage values, only the said 3 pins; TxD, RxD and GND; are needed.

3.1.3-b Graphical User Interface

The graphical user interface is the main system that the user will use to control the PC Based Blood Pressure and Pulse Rate Monitoring System. The developed system will display the Systolic and Diastolic blood pressure values as well as the pulse rate on the monitor for easy viewing. The author has opted to use LabVIEW as it is the ideal programming platform to be used for the project. LabVIEW will be used to read and interpret the input signal as well as work as the graphical interface that will be used to control the circuits. LabVIEW is a whole package as it does not need to be linked to any other software.

3.1.4 Explanation on how system works

The arm cuff is fitted to the user and is pumped. The LabVIEW software is then run, and air is slowly released from the arm cuff using the release valve. The voltage value from the pressure sensor is run through the instrumentation amplifier and is amplified. The signal is then sent to the ADC to be digitized. The signal will then be sent to the PC via RS-232 to be processed by LabVIEW. In LabVIEW, the signal is constantly monitored throughout the measurement process. As the cuff pressure is slowly released, the pulse would suddenly break out of its occlusion and would cause pulsations. The pressure at which the pulsations start to occur is the Systolic Pressure. The DC component voltage value would then be measured at that point and it will be used to calculate the pressure value in mmHg based on a set of calculations involving the voltage gain and the slope of the pressure sensors voltage-pressure characteristics. After the Systolic Pressure measurement, the pulsations would reach a peak and slowly diminish. The point at which the peak starts to diminish is the Diastolic Pressure. To be able to start measurements, a certain value of threshold voltage will be set. The amplitude of oscillations further reduces as air is further released. When the threshold voltage drops to below a certain value, it is monitored for a time interval of 2 seconds, and if it does not go above the value this would mean that it is below the threshold voltage value and the DC component signal can be measured according to the peak value using the same calculations as the Systolic Pressure. LabVIEW would then proceed to measure the pulse rate. The pulse rate is measured at this point because the oscillations are still strong and stable. LabVIEW would measure the number of peaks in the voltage value for a time interval of 5 seconds. The number of peaks would then be converted for a reading of 1 minute. All the values are then displayed on the monitor to be viewed by the user.

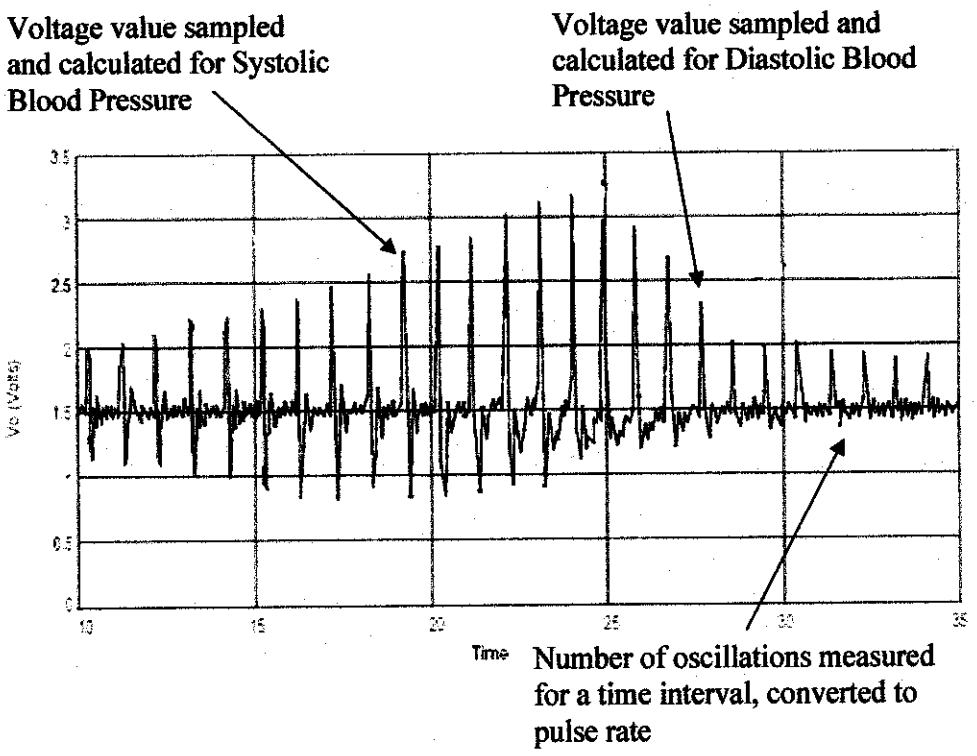

Figure 18: *Typical Oscillometric Method waveform; points of where pulses should be measured are indicated [1].*

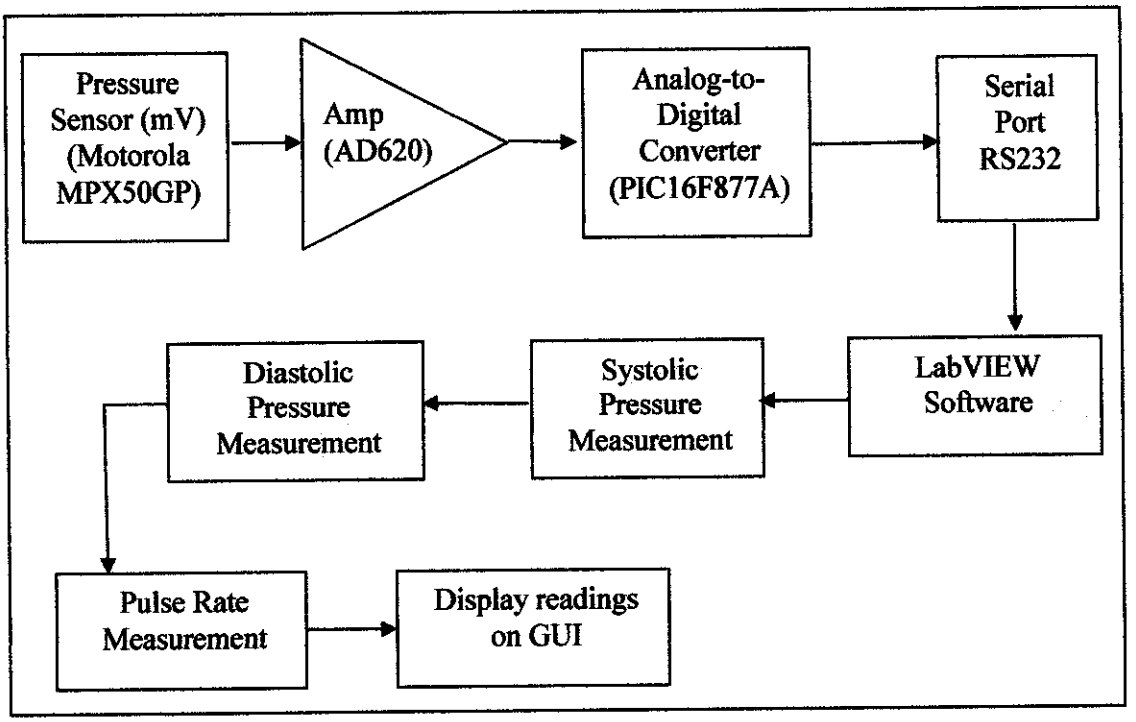

Figure 19: *Process Flow Diagram of how the system works*

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Results

4.1.1 Module 1: Blood Pressure Sensor Module

4.1.1-a Pressure Sensor and Instrumentation Amplifier.

The output of the Motorola MPX50GP pressure sensor gives a differential output in mV value. In order to get the right value to enable proper sampling, the voltage value needs to be amplified. The pressure sensor is supplied with 3 Volts DC voltage and GND.

The MPX50GP gives an output voltage reading of 18mV in idle condition where no pressure is applied. This reading is rather small and needs to be amplified to achieve legible readings. The value chosen for amplification is 100 to achieve readings between the ranges of approximately 2V to 4V.

To test if the value of a 100 chosen for the project is appropriate, some calculations are carried out using the equation below:

$$\mathrm{Pr}essure\_mmHg = \frac{DC\_Voltage}{100} \times 6251$$

6251 is the equation constant calculated from the slope of the pressure sensor and the kPa to mmHg conversion factor. (The calculations are shown in section 4.1.3-b).

Example: Using 125 mmHg as a base value

$$125 = \frac{DC\_Voltage}{100} \times 6251$$

$$DC\_Voltage = 2.0V$$

From the calculations obtained, the gain value of 100 satisfies the criteria. So the gain for the AD620 instrumentation Amplifier is chosen to be 100.

The Analog Devices AD620 Instrumentation Amplifier is given the task of amplifying the signal. The Instrumentation Amplifier is supplied with +/- 5 Volts DC voltages. The amplification value is determined by the Gain Resistor (R_G). In order to get the desired value, the equation below is used:

$$R_G = \frac{49.4k\Omega}{G-1}$$

To obtain a gain of 100, the calculations below are done:

$$R_G = \frac{49.4k\Omega}{100-1}$$
$$R_G = \frac{49.4k\Omega}{99}$$
$$R_G = 498.9\Omega$$

So in order to achieve a gain of at least100, a resistance of 498.9Ω needs to be applied. The Rg value chosen for the Instrumentation Amplifier from testing is chosen to be 500Ω as it gives the voltage gain that we need. Through real time testing using the Instrumentation Amplifier, the amplification value obtained is approximately 121 times. This value is still tolerable.

Calculation of voltage with gain of 121

18 mV x 121 = 2.178 V

23 mV x 121 = 2.783 V

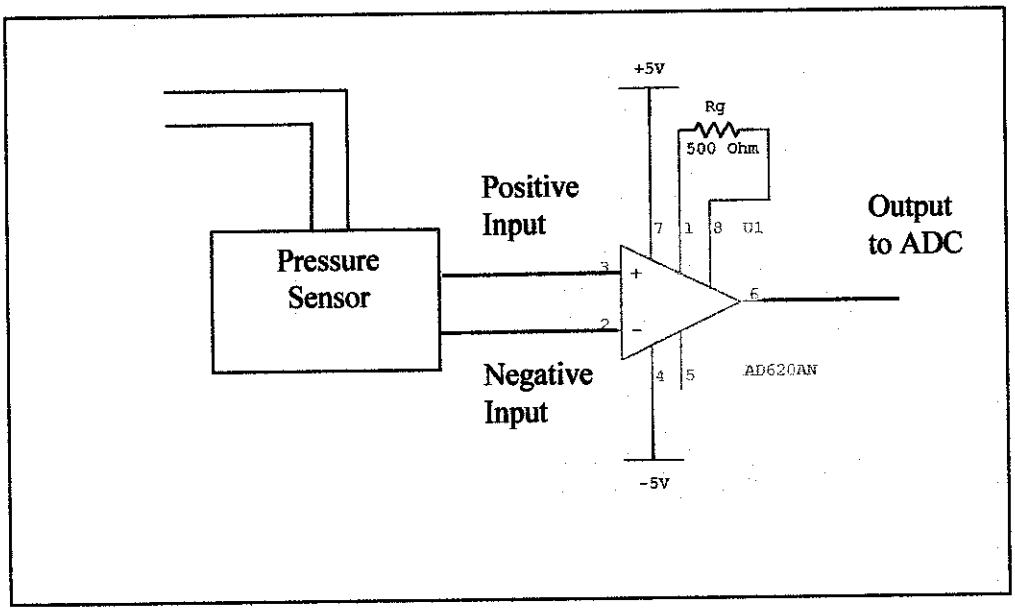

***Figure 20:** Pressure sensor and instrumentation amplifier module*

4.1.2 Module 2: Analog to Digital Converter Module Results

In order for the PIC16F877A to be used as an ADC, it needs to be programmed first. The program used for the PIC is in appendix I. PIC C Compiler software is used to compile and create the hex file. Microchip MPLAB software is then used to download the program into the PIC16F877A using the programming board available in the lab. The software will set all the I/O ports of the microcontroller to perform analog to digital conversion corresponding to the program that has been designed.

Port AN0 is used as the input for the amplified analog signal that is obtained from the pressure sensor. The PIC is supplied with 5V nominal voltage and a 10MHz crystal

oscillator. The oscillator is used to supply a clock to the microcontroller in order for it to execute a program of instructions. The output for the ADC uses pin 25, which is the RC6/TX pin. As the ADC would be using the Serial Port (RS 232) to communicate with the PC, it is necessary to use the MAX 232 chip in order for it to function. This is because the Serial Port requires negative logic. The MAX 232 acts as a converter for the right voltage logic value. The MAX 232 is supplied with 5V nominal voltage and needs 4 external 1μF capacitors. The output from the MAX232 chip is connected to pin 2 on the RS232 DB 9 connector which corresponds to "Receive Data" on the PC side. The circuit for the ADC converter is as below:

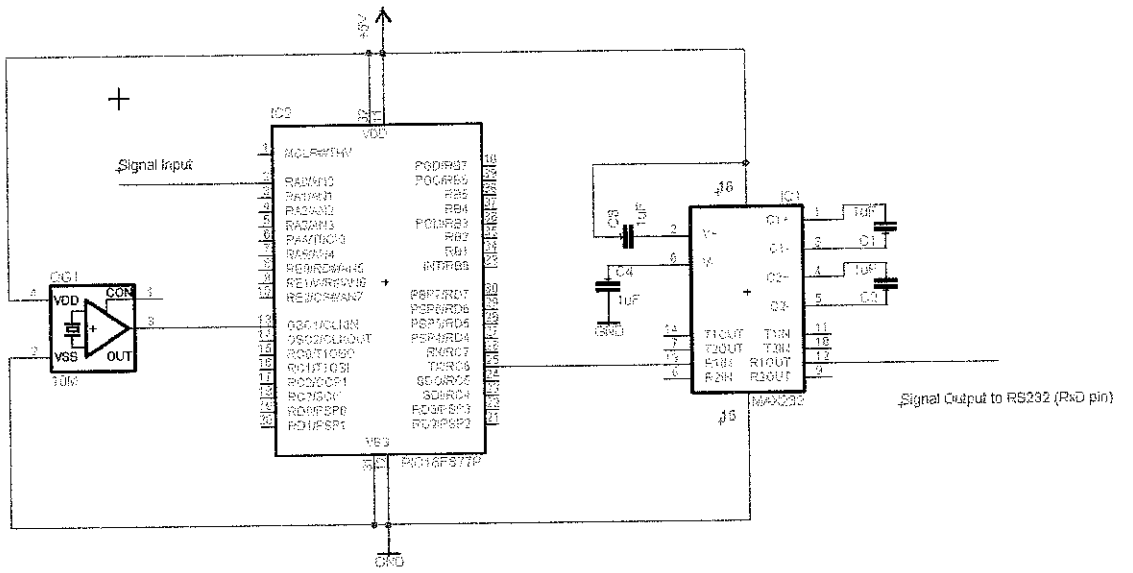

***Figure 21:** Schematic Diagram of ADC*

Tests were carried out on the ADC to ensure it functions correctly. Tests were carried out using Hyper Terminal Software available in Windows XP. Hyper Terminal is the ideal platform to test the ADC converter. Hyper Terminal is setup by setting 9600 baud rate, 8 data bits, No parity, 1 stop bit and Hardware flow control. The Com port associated with the serial port needs to be setup also, which is Com 3 for the computer that was used. Below are the results from testing the ADC with various voltage inputs from 2V to 5V with the digitized voltage reading shown on the Hyper Terminal interface.

Laboratory Power Supply	HyperTerminal Results
2.0 V	2.0034 V
2.5 V	2.5012 V
3.0 V	3.0107 V
3.5 V	3.5028 V
4.0 V	4.0019 V
4.5 V	4.5081 V
5.0 V	5.0000 V

Table 4: *Comparison of Voltage values between Laboratory Power Supply and Hyper Terminal*

From the results obtained, it can be seen that the Analog to Digital Converter is working with fairly good accuracy and can be used for the project purposes. The values obtained in Hyper Terminal is rounded off to 4 decimal points.

As the method used is the Oscillometric method, the signal is sampled every 40 milliseconds in order to get an accurate reading. The resulting waveform is similar to an oscillatory signal, where the spikes for the Systolic and Diastolic are visible.

4.1.4 Module 3: Graphical User Interface Module

4.1.4-a LabVIEW Programming

4.1.4-a-i Reading voltage from Serial Port

To sample the signal that has been sent from the ADC to the Serial Port, the VISA virtual instrument is used. VISA in LabVIEW is a set of library functions that is used to communicate with GPIB, serial, VXI, and computer-based instruments. The first part is to accurately obtain the signal from the serial port and display it as a waveform chart. To use LabVIEW VISA, it first needs to be configured for the specific input source that is being used. For this project, the input is the Serial Port. So VISA Serial is used and it needs to be configured using the proper settings. Settings that need to be done are:

Setting Name	**Configuration**
VISA Resource	The COM Port that the serial port uses (example: COM 1, COM 2)
Baud Rate	9600
Data Bits	8
Parity	No Parity
Stop Bits	1
Flow Control	0

***Table 5:** Settings for VISA Serial*

It is important that the settings done in VISA Serial match the settings for the Serial Port. The above stated configuration is used for the project data transfer. If any values do not match, LabVIEW will not detect the input signal.

The signal is then sent to the array function in order to get values in the proper order. The data values, in the case of this project the voltage values, are sorted into a row. The values are the read and plotted on a graph using the Graph function.

4.1.4-a-ii Peak Detector VI

The main function that will be used in the LabVIEW Programming will be the Peak Detector VI (virtual instrument) as the main scope of the project is to detect the amplitudes of the peaks of the oscillatory signal. The Peak Detector VI can be used to detect peaks or valleys, the amplitudes, widths of the signal, locations and also number of peaks or valleys that are present in a certain period or time. For the project, for the Systolic Calculation, the Peak Detector will be set to a certain voltage threshold and the peak that rises above the threshold will be evaluated. As for Diastolic Pressure measurement, the peaks below the threshold will be evaluated in order to determine the pressure value. For Pulse Rate, the # *found* function on the Peak Detector VI will be used to count the number of pulses that occurs in a time interval and it would be converted to pulse rate per minute.

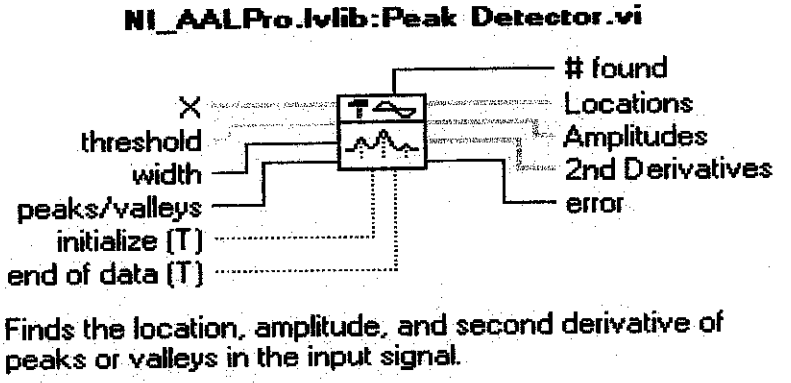

***Figure 22:** Peak Detector.vi (Source: www.ni.com)*

4.1.4-b Determining the Threshold Voltage for the Systolic Pressure

In order to determine the proper threshold voltage to be set for the Peak Detector VI, the voltage value was measured manually. How this was done was to attach the pressure cuff to the pressure sensor and the instrumentation amplifier. The output from the instrumentation amplifier is then hooked up to the oscilloscope in order to see the changes in voltage value. As known from previous calculation and testing using the pressure sensor, in idle state the voltage value obtained is approximately 2.178 V amplified. The pressure cuff is pumped to obstruct the flow of blood in the artery. In order to measure, the air from the arm cuff is slowly released using the release valve on the hand pump. As the pulse breaks from the occlusion, the changes in voltage value can be seen on the oscilloscope. The systolic pressure voltage value can be seen and the value can be used for setting the threshold voltage. In order for better accuracy, the system was tested on 3 different people in order to get a better picture of the value of the threshold voltage.

Subject	Voltage
Person 1	2.35 Volts
Person 2	2.51 Volts
Person 3	2.44 Volts

***Table 6:** Value of voltage obtained when testing 3 different subjects*

So, it can be seen that the value of voltage does not go below 2.3 Volts. So the threshold voltage can be set to 2.3 Volts, where it will only measure peaks that are above 2.3 volts for calculation.

4.1.4-c Calculation for Systolic and Diastolic Pressure

After the pulse has been sampled and the DC voltage value is obtained, the voltage value would go through a few calculations in order to obtain the correct pressure reading. In order to perform the calculations, the pressure-voltage slope value of the pressure sensor needs to be obtained. This is done by taking 2 points and calculating the slope value.

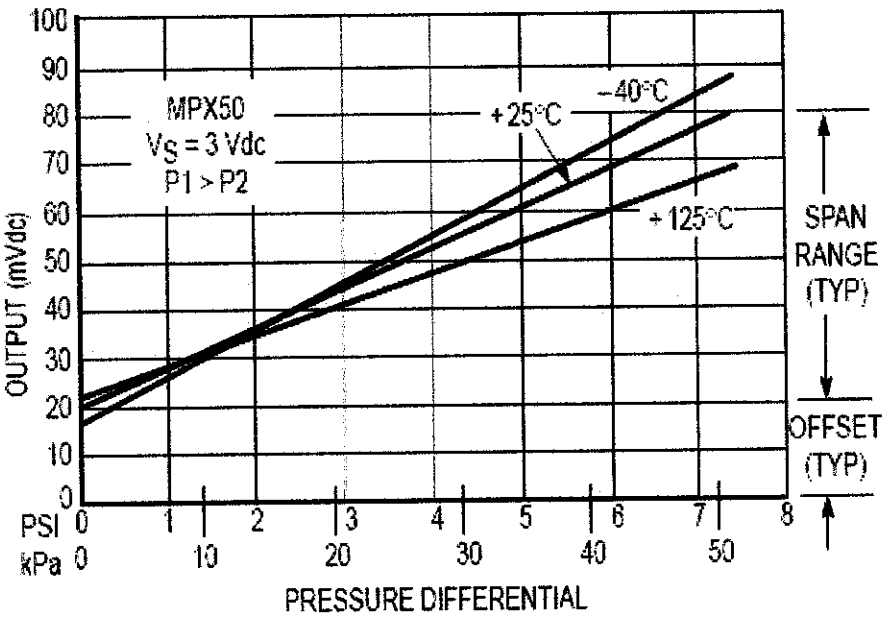

Figure 23: *Voltage output versus pressure differential for the Motorola MPX50GP Pressure Sensor [6].*

Points at 10 kPa and 50 kPa are chosen to calculate the slope. At 10 kPa, the voltage value is 30 mV and for 50 kPa it is 78 mV.

$$Slope = \frac{78mV - 30mV}{50kPa - 10kPa} = 1.2 \times 10^{-3} V / kPa$$

As calculated earlier, the gain of the amplifier is approximately 121. Because the output voltage versus the differential pressure slope is in mV, the voltage value needs to be divided again by the amplification value.

$$Sensor\_Voltage = \frac{Voltage\_after\_amplification}{Gain\_Value}$$

$$Sensor\_Voltage = \frac{Voltage\_after\_amplification}{121}$$

After that, the voltage value is divided by the slope value in order to obtain the pressure value in kPa.

$$kPa\_reading = \frac{Sensor\_Voltage}{Slope}$$

$$kPa\_reading = \frac{Sensor\_Voltage}{1.2\times10^{-3}V/kPa}$$

To convert the pressure from kPa to mmHg,

$$kPa\_to\_mmHg\_pressure = \frac{760mmHg}{101.325kPa} = 7.5006168\,mmHg/kPa$$

So the readings in mmHg will be:

$$mmHg\_reading = kPa\_reading \times 7.5006168mmHg/kPa$$

In order to obtain a reading in mmHg, the conversion value is divided by the slope

$$\frac{7.5006168mmHg/kPa}{1.2\times10^{-3}V/kPa} = 6250.51mmHg/V$$

To get the final value in mmHg, the voltage value is multiplied with the value obtained.

$$Sensor\_Voltage \times 6250.51mmHg/V = \Pr essure\_mmHg$$

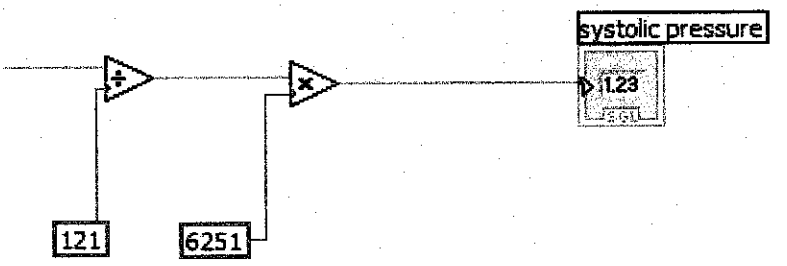

Figure 24: Sub-VI to convert the voltage value to mmHg pressure.

4.1.4-d Determining Pulse Rate Measurement

The Pulse Rate is chosen to be determined right after the Diastolic Pressure Measurement. The Pulse Rate is also determined using the Peak Detector. How this is done is for a time interval of 5 seconds, the number of oscillation peaks found is measured using the *# found* function. The numbers of peaks that are found are then calculated for a one minute interval to get the pulse rate per minute value.

4.1.4-e User Interface

The user interface for the project is to incorporate the readings of Systolic Pressure, Diastolic Pressure and Pulse Rate measurements for easy viewing. It also acts as the main interface between the user and the computer in terms of starting and stopping the program from running.

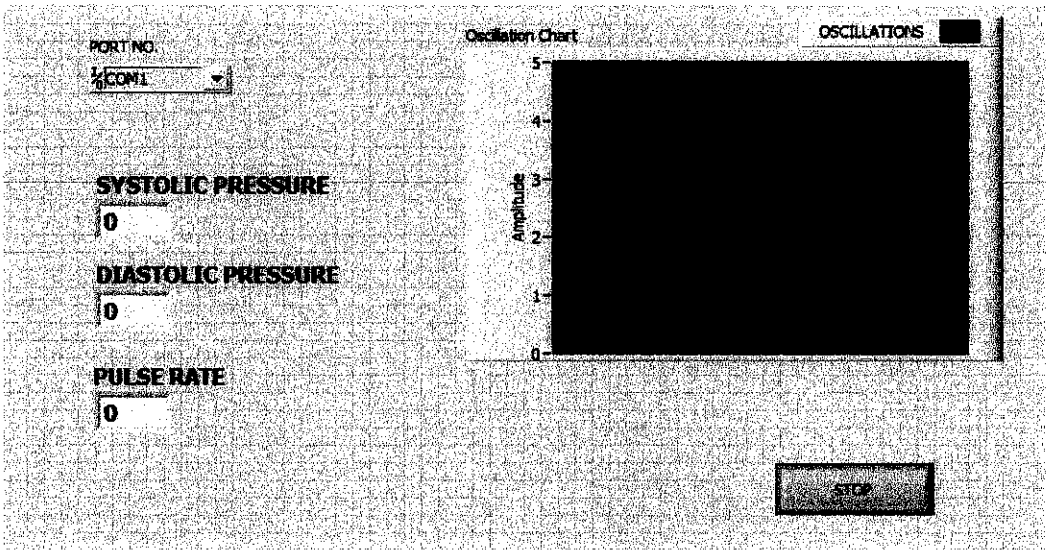

Figure 25: *Front Panel showing Systolic Pressure, Diastolic Pressure and Pulse Rate.*

4.2 Discussion

The hardware of the system comprising of the Pressure Sensor, Instrumentation Amplifier and the Analog-to-Digital Converter are working properly. However there are problems with the LabVIEW software in terms of the manipulation and processing of the signal. The system reads the signal well and the waveform can be seen as it is displayed on the graphical user interface. The problems that are present involve the processing to obtain the Systolic and Diastolic Pressure and also the Pulse Rate.

CHAPTER 5
CONCLUSION AND RECOMMENDATIONS

The PC Based Blood Pressure and Pulse Rate Monitor is believed to be a very useful device in order to assist people in carrying out measurement by themselves. It uses the PC which is found in most households. This would encourage people to monitor their health as it can be a hassle to go all the way to a medical practitioner for blood pressure monitoring. The system is based on the oscillometric method. The Oscillometric Method is the measurement of the amplitude of the change in pressure as the cuff is deflated from the value above the systolic pressure. Amplitude suddenly grows larger as pulse suddenly breaks through its obstruction. The pressure at this moment is very close to the systolic pressure. As the cuff pressure is further reduced, there is a great increase in pulse amplitude where it reaches a maximum value and then would quickly diminish. The diastolic pressure is taken when the peak starts to diminish. The systolic blood pressure and diastolic blood pressure are obtained by identifying the region where there is rapid increase the decrease in the amplitude of the pulses.

Recommendations that can be done for the project is to have a proper working model. The next student to take over this project should carry out some fine tuning and maybe change or redesign certain aspects of the hardware, as the initial groundwork has already been carried out. It is also recommended that a motorized pump be incorporated into the system so as to make it a fully automatic system. On the programming side of the project, the software can be changed to either Visual Basic or C++, depending on the suitability.

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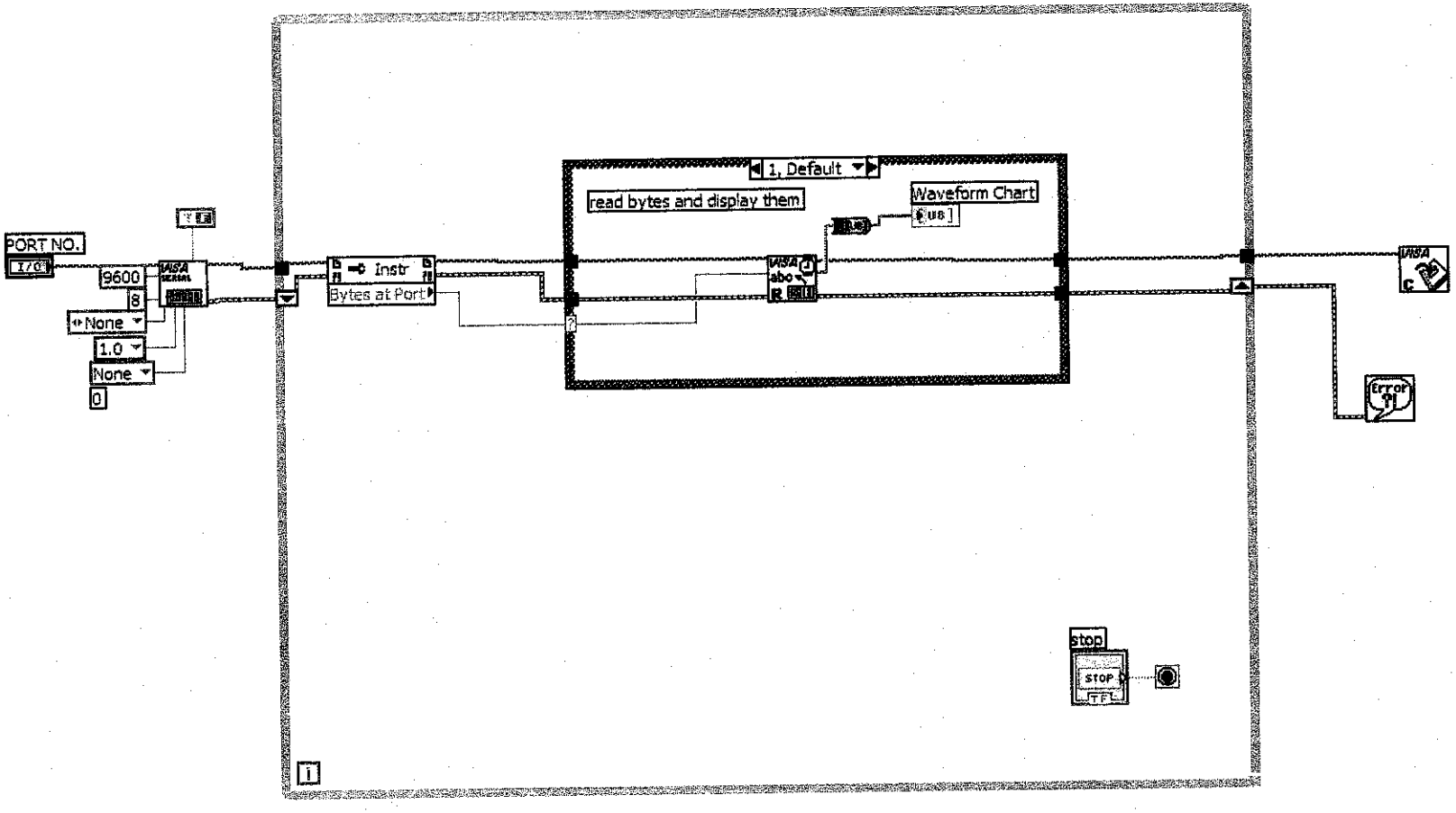
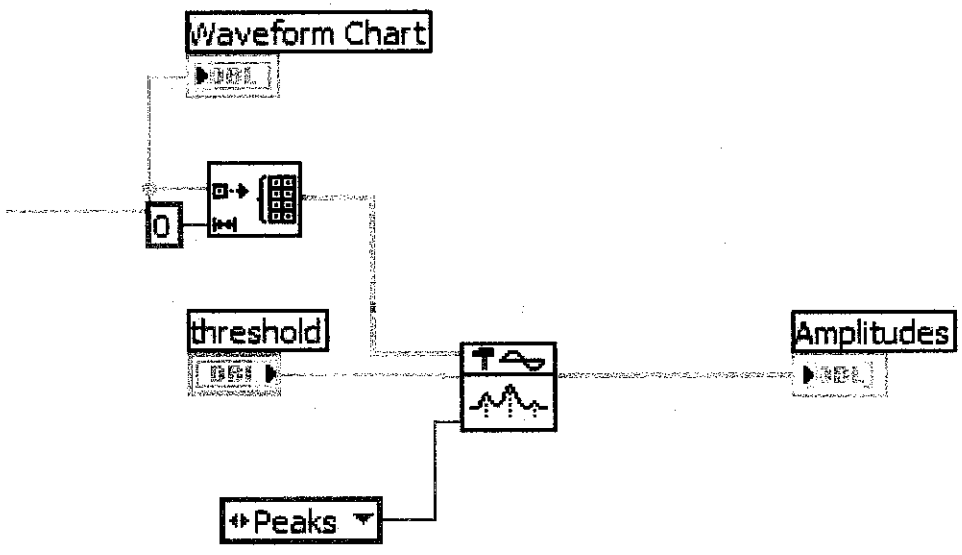
http://www.people.cornell.edu/pages/ws62/

APPENDIX A

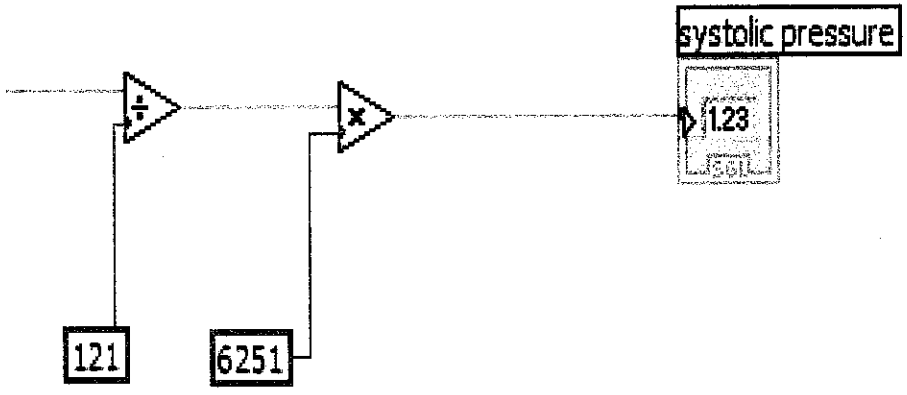
PIC16F877A ANALOG TO DIGITAL CONVERTER PROGRAM



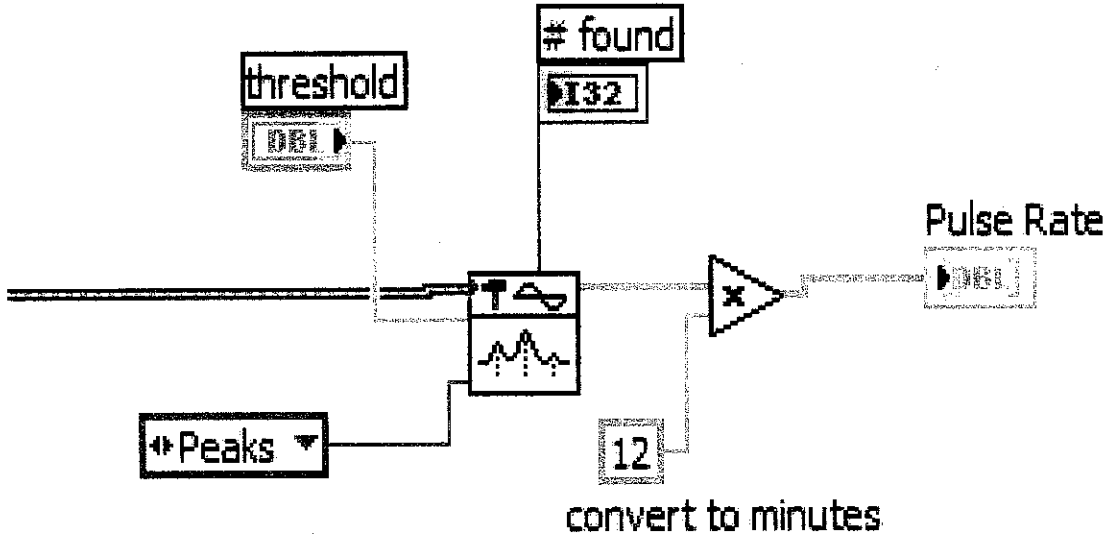
LabVIEW VISA Serial VI



Detecting peaks using Peak Detector.VI



Mathematical Equations for Systolic and Diastolic Pressure Calculation



Using Peak Detector.VI to obtain pulse rate

APPENDIX C
DATASHEETS

senseon

50 kPa Uncompensated Silicon Pressure Sensors

MPX50 SERIES

0 to 50 kPa (0–7.25 psi)
60 mV FULL SCALE SPAN
(TYPICAL)

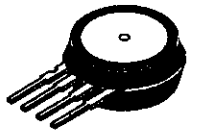
The MPX50 silicon piezoresistive pressure sensor provides a very accurate and linear voltage output — directly proportional to the applied pressure. This standard, low cost, uncompensated sensor permits manufacturers to design and add their own external temperature compensating and signal conditioning networks. Compensation techniques are simplified because of the predictability of Motorola's single element strain gauge design.

Features

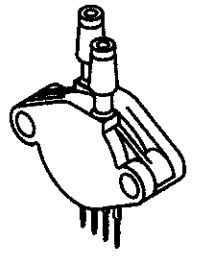
- Low Cost
- Patented Silicon Shear Stress Strain Gauge Design
- Ratiometric to Supply Voltage
- Easy to Use Chip Carrier Package Options
- 60 mV Span (Typ)
- Differential and Gauge Options
- ±0.25% (Max) Linearity

Application Examples

- Air Movement Control
- Environmental Control Systems
- Level Indicators
- Leak Detection
- Medical Instrumentation
- Industrial Controls
- Pneumatic Control Systems
- Robotics



BASIC CHIP CARRIER ELEMENT
CASE 344–15, STYLE 1



DIFFERENTIAL PORT OPTION
CASE 344C–01, STYLE 1

NOTE: Pin 1 is the notched pin.

PIN NUMBER			
1	Gnd	3	V_S
2	$+V_{out}$	4	$-V_{out}$

Figure 1 shows a schematic of the internal circuitry on the stand–alone pressure sensor chip.

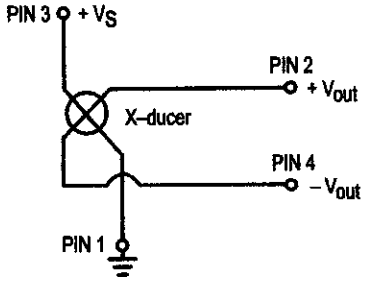


Figure 1. Uncompensated Pressure Sensor Schematic

VOLTAGE OUTPUT versus APPLIED DIFFERENTIAL PRESSURE

The differential voltage output of the X–ducer is directly proportional to the differential pressure applied.

The output voltage of the differential or gauge sensor increases with increasing pressure applied to the pressure side (P1) relative to the vacuum side (P2). Similarly, output voltage increases as increasing vacuum is applied to the vacuum side (P2) relative to the pressure side (P1).

Senseon and X–ducer are trademarks of Motorola, Inc.

REV 5

MOTOROLA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Overpressure(8) (P1 > P2)	P_{max}	200	kPa
Burst Pressure(8) (P1 > P2)	P_{burst}	500	kPa
Storage Temperature	T_{stg}	–40 to +125	°C
Operating Temperature	T_A	–40 to +125	°C

OPERATING CHARACTERISTICS (V_S = 3.0 Vdc, T_A = 25°C unless otherwise noted, P1 > P2)

Characteristic	Symbol	Min	Typ	Max	Unit
Pressure Range(1)	P_{OP}	0	—	50	kPa
Supply Voltage(2)	V_S	—	3.0	6.0	Vdc
Supply Current	I_o	—	6.0	—	mAdc
Full Scale Span(3)	V_{FSS}	45	60	90	mV
Offset(4)	V_{off}	0	20	35	mV
Sensitivity	$\Delta V/\Delta P$	—	1.2	—	mV/kPa
Linearity(5)	—	–0.25	—	0.25	$\%V_{FSS}$
Pressure Hysteresis(5) (0 to 50 kPa)	—	—	±0.1	—	$\%V_{FSS}$
Temperature Hysteresis(5) (– 40°C to +125°C)	—	—	±0.5	—	$\%V_{FSS}$
Temperature Coefficient of Full Scale Span(5)	TCV_{FSS}	–0.22	—	–0.16	$\%V_{FSS}$/°C
Temperature Coefficient of Offset(5)	TCV_{off}	—	±15	—	µV/°C
Temperature Coefficient of Resistance(5)	TCR	0.21	—	0.27	$\%Z_{in}$/°C
Input Impedance	Z_{in}	400	—	550	Ω
Output Impedance	Z_{out}	750	—	1800	Ω
Response Time(6) (10% to 90%)	t_R	—	1.0	—	ms
Warm–Up	—	—	20	—	ms
Offset Stability(9)	—	—	±0.5	—	$\%V_{FSS}$

MECHANICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Weight (Basic Element Case 344–15)	—	—	2.0	—	Grams
Common Mode Line Pressure(7)	—	—	—	690	kPa

NOTES:

1. 1.0 kPa (kiloPascal) equals 0.145 psi.
2. Device is ratiometric within this specified excitation range. Operating the device above the specified excitation range may induce additional error due to device self–heating.
3. Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.
4. Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
5. Accuracy (error budget) consists of the following:
   - Linearity: Output deviation from a straight line relationship with pressure, using end point method, over the specified pressure range.
   - Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.
   - Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the minimum or maximum rated pressure, at 25°C.
   - TcSpan: Output deviation at full rated pressure over the temperature range of 0 to 85°C, relative to 25°C.
   - TcOffset: Output deviation with minimum rated pressure applied, over the temperature range of 0 to 85°C, relative to 25°C.
   - TCR: Z_{in} deviation with minimum rated pressure applied, over the temperature range of –40°C to +125°C, relative to 25°C.
6. Response Time is defined as the time for the incremental change in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.
7. Common mode pressures beyond specified may result in leakage at the case–to–lead interface.
8. Exposure beyond these limits may cause permanent damage or degradation to the device.
9. Offset stability is the product's output deviation when subjected to 1000 hours of Pulsed Pressure, Temperature Cycling with Bias Test.

TEMPERATURE COMPENSATION

Figure 2 shows the typical output characteristics of the MPX50 series over temperature.

The X–ducer piezoresistive pressure sensor element is a semiconductor device which gives an electrical output signal proportional to the pressure applied to the device. This device uses a unique transverse voltage diffused semiconductor strain gauge which is sensitive to stresses produced in a thin silicon diaphragm by the applied pressure.

Because this strain gauge is an integral part of the silicon diaphragm, there are no temperature effects due to differences in the thermal expansion of the strain gauge and the diaphragm, as are often encountered in bonded strain gauge pressure sensors. However, the properties of the strain gauge itself are temperature dependent, requiring that the device be temperature compensated if it is to be used over an extensive temperature range.

Temperature compensation and offset calibration can be achieved rather simply with additional resistive components, or by designing your system using the MPX2050 series sensors.

Several approaches to external temperature compensation over both −40 to +125°C and 0 to +80°C ranges are presented in Motorola Applications Note AN840.

LINEARITY

Linearity refers to how well a transducer's output follows the equation: $V_{out} = V_{off}$ + sensitivity x P over the operating pressure range (see Figure 3). There are two basic methods for calculating nonlinearity: (1) end point straight line fit or (2) a least squares best line fit. While a least squares fit gives the "best case" linearity error (lower numerical value), the calculations required are burdensome.

Conversely, an end point fit will give the "worst case" error (often more desirable in error budget calculations) and the calculations are more straightforward for the user. Motorola's specified pressure sensor linearities are based on the end point straight line method measured at the midrange pressure.

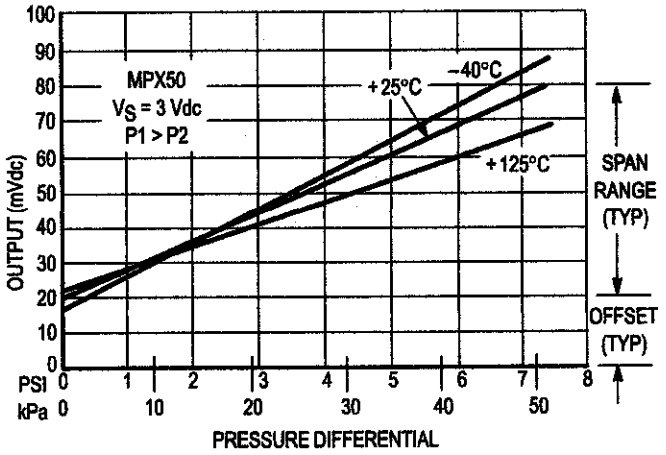


Figure 2. Output versus Pressure Differential

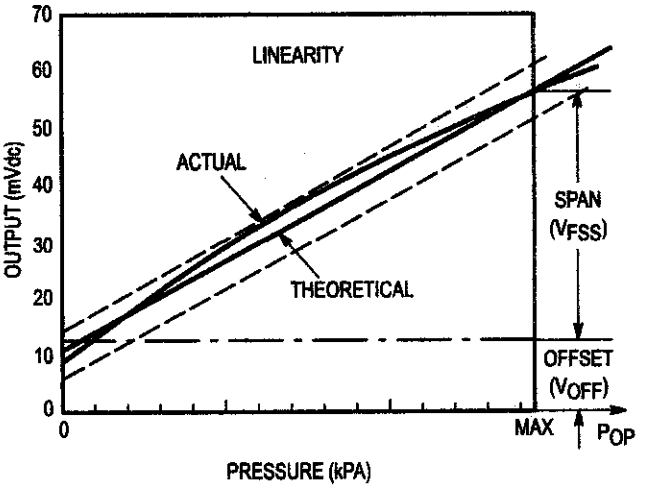


Figure 3. Linearity Specification Comparison

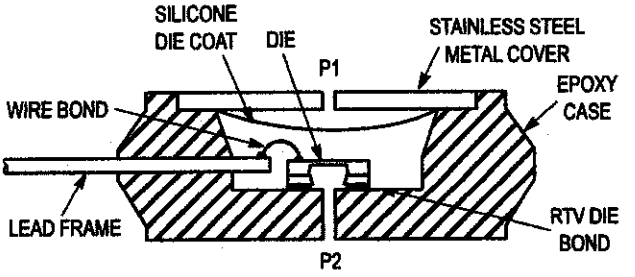


Figure 4. Cross–Sectional Diagram (not to scale)

Figure 4 illustrates the differential or gauge configuration in the basic chip carrier (Case 344–15). A silicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

The MPX50 series pressure sensor operating characteristics and internal reliability and qualification tests are based on use of dry air as the pressure media. Media other than dry air may have adverse effects on sensor performance and long term reliability. Contact the factory for information regarding media compatibility in your application.

PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

Motorola designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing silicone gel which isolates the die from the environment. The Motorola MPX pressure sensor is designed to operate with positive differential pressure applied, P1 > P2.

The Pressure (P1) side may be identified by using the table below:

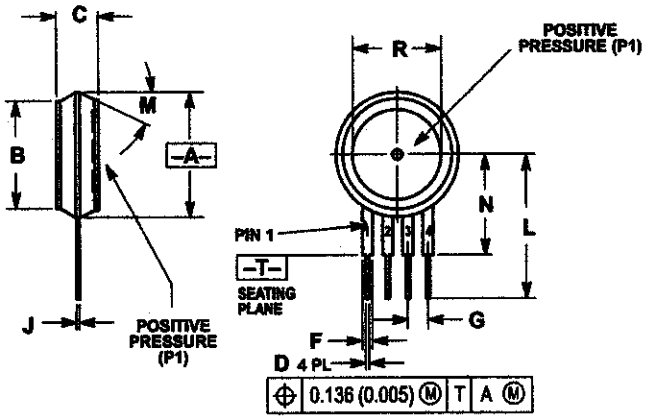
Part Number	Case Type	Pressure (P1) Side Identifier
MPX50D	344–15	Stainless Steel Cap
MPX50DP	344C–01	Side with Part Marking
MPX50GP	344B–01	Side with Port Attached
MPX50GVP	344D–01	Stainless Steel Cap
MPX50GS	344E–01	Side with Port Attached
MPX50GVS	344A–01	Stainless Steel Cap
MPX50GSX	344F–01	Side with Port Attached
MPX50GVSX	344G–01	Stainless Steel Cap

ORDERING INFORMATION

MPX50 series pressure sensors are available in differential and gauge configurations. Devices are available with basic element package or with pressure port fittings which provide printed circuit board mounting ease and barbed hose pressure connections.

Device Type	Options	Case Type	MPX Series	
			Order Number	Device Marking
Basic Element	Differential	Case 344–15	MPX50D	MPX50D
Ported Elements	Differential	Case 344C–01	MPX50DP	MPX50DP
	Gauge	Case 344B–01	MPX50GP	MPX50GP
	Gauge Vacuum	Case 344D–01	MPX50GVP	MPX50GVP
	Gauge Stovepipe	Case 344E–01	MPX50GS	MPX50D
	Gauge Vacuum Stovepipe	Case 344A–01	MPX50GVS	MPX50D
	Gauge Axial	Case 344F–01	MPX50GSX	MPX50D
	Gauge Vacuum Axial	Case 344G–01	MPX50GVSX	MPX50D

PACKAGE DIMENSIONS

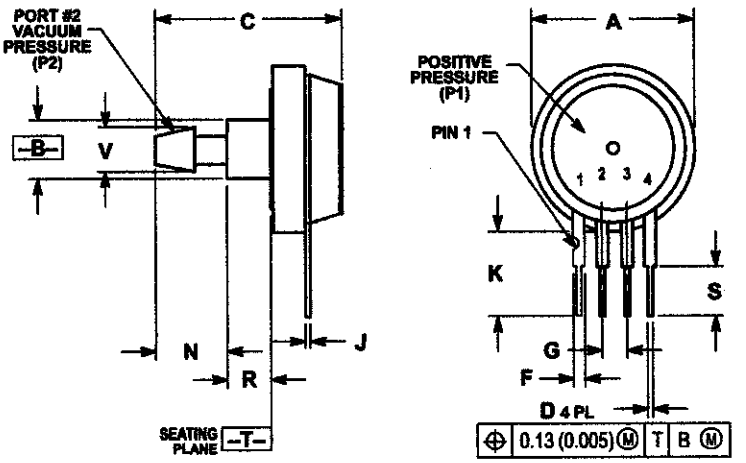


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION –A– IS INCLUSIVE OF THE MOLD STOP RING. MOLD STOP RING NOT TO EXCEED 16.00 (0.630).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.595	0.630	15.11	16.00
B	0.514	0.534	13.06	13.56
C	0.200	0.220	5.08	5.59
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.40
L	0.695	0.725	17.65	18.42
M	30° NOM		30° NOM	
N	0.475	0.495	12.07	12.57
R	0.430	0.450	10.92	11.43

STYLE 1:
PIN 1. GROUND
2. + OUTPUT
3. + SUPPLY
4. – OUTPUT

CASE 344–15
ISSUE W



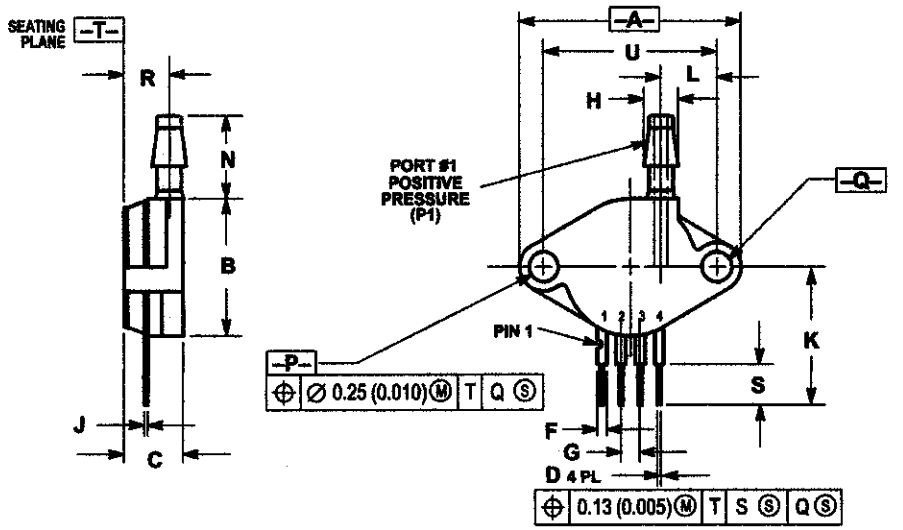
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.690	0.720	17.53	18.28
B	0.245	0.255	6.22	6.48
C	0.780	0.820	19.81	20.82
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.345	0.375	8.76	9.53
N	0.300	0.310	7.62	7.87
R	0.178	0.186	4.52	4.72
S	0.220	0.240	5.59	6.10
V	0.182	0.194	4.62	4.93

STYLE 1:
PIN 1. GROUND
2. + OUTPUT
3. + SUPPLY
4. – OUTPUT

CASE 344A–01
ISSUE B

PACKAGE DIMENSIONS — CONTINUED

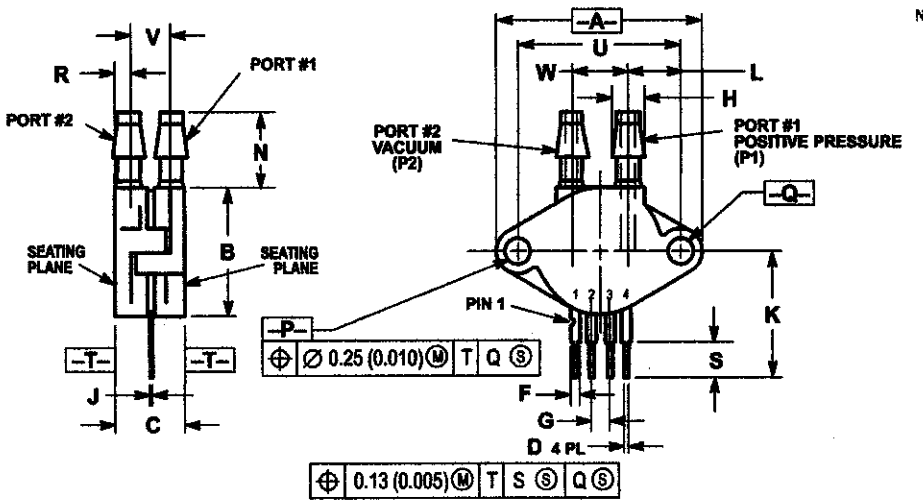


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.145	1.175	29.08	29.85
B	0.685	0.715	17.40	18.16
C	0.305	0.325	7.75	8.26
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
H	0.182	0.194	4.62	4.93
J	0.014	0.016	0.36	0.41
K	0.695	0.725	17.65	18.42
L	0.290	0.300	7.37	7.62
N	0.420	0.440	10.67	11.18
P	0.153	0.159	3.89	4.04
Q	0.153	0.159	3.89	4.04
R	0.230	0.250	5.84	6.35
S	0.220	0.240	5.59	6.10
U	0.910 BSC		23.11 BSC	

STYLE 1:
PIN 1. GROUND
2. + OUTPUT
3. + SUPPLY
4. – OUTPUT

CASE 344B–01
ISSUE B



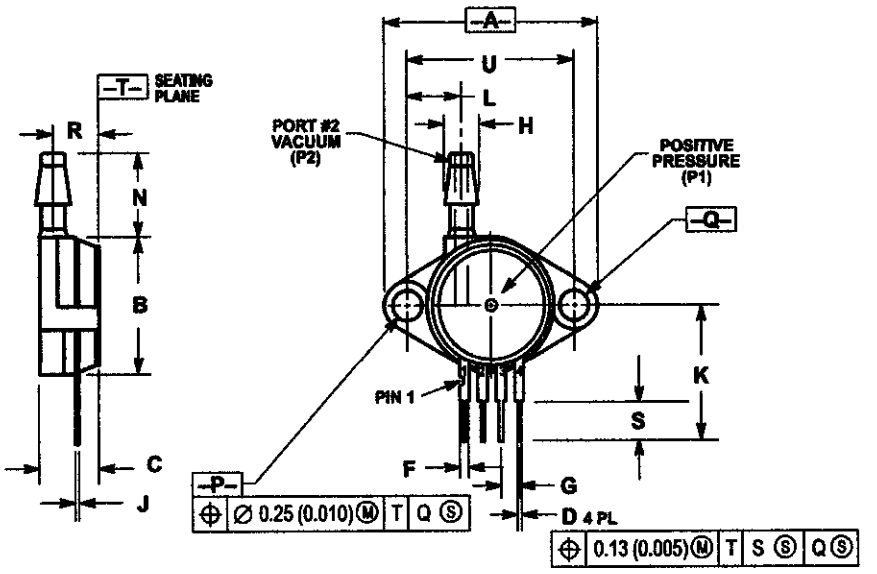
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.145	1.175	29.08	29.85
B	0.685	0.715	17.40	18.16
C	0.405	0.435	10.29	11.05
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
H	0.182	0.194	4.62	4.93
J	0.014	0.016	0.36	0.41
K	0.695	0.725	17.65	18.42
L	0.290	0.300	7.37	7.62
N	0.420	0.440	10.67	11.18
P	0.153	0.159	3.89	4.04
Q	0.153	0.159	3.89	4.04
R	0.063	0.083	1.60	2.11
S	0.220	0.240	5.59	6.10
U	0.910 BSC		23.11 BSC	
V	0.248	0.278	6.30	7.06
W	0.310	0.330	7.87	8.38

STYLE 1:
PIN 1. GROUND
2. + OUTPUT
3. + SUPPLY
4. – OUTPUT

CASE 344C–01
ISSUE B

PACKAGE DIMENSIONS — CONTINUED



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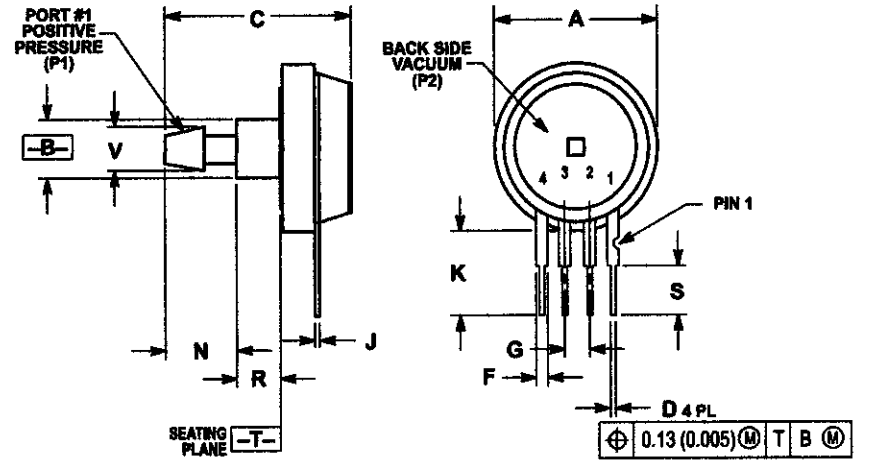
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.145	1.175	29.08	29.85
B	0.685	0.715	17.40	18.16
C	0.305	0.325	7.75	8.26
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
H	0.182	0.194	4.62	4.93
J	0.014	0.016	0.36	0.41
K	0.695	0.725	17.65	18.42
L	0.290	0.300	7.37	7.62
N	0.420	0.440	10.67	11.18
P	0.153	0.159	3.89	4.04
Q	0.153	0.158	3.89	4.04
R	0.230	0.250	5.84	6.35
S	0.220	0.240	5.59	6.10
U	0.910 BSC		23.11 BSC	

STYLE 1:
PIN 1. GROUND
2. + OUTPUT
3. + SUPPLY
4. – OUTPUT

CASE 344D–01
ISSUE B



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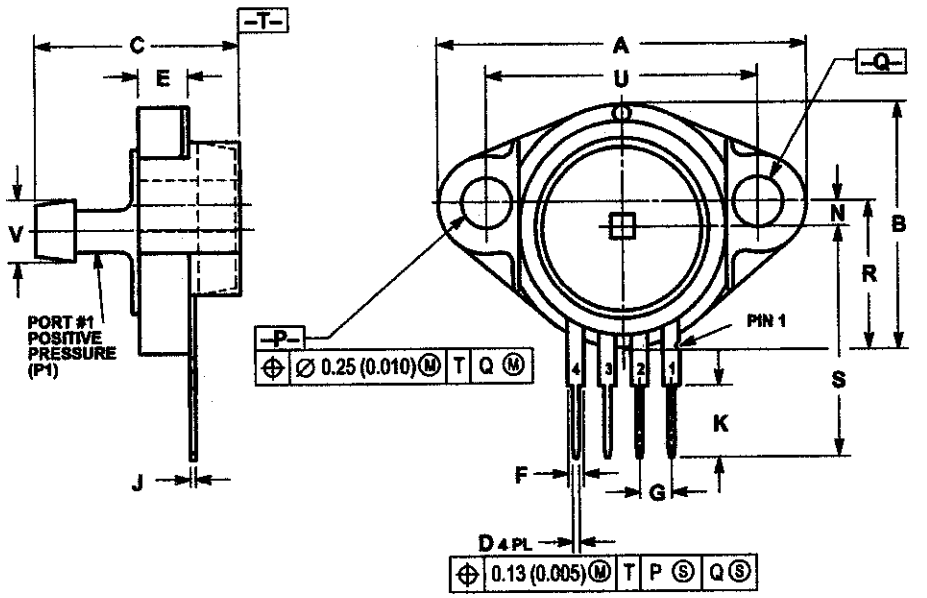
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.690	0.720	17.53	18.28
B	0.245	0.255	6.22	6.48
C	0.780	0.820	19.81	20.82
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.345	0.375	8.76	9.53
N	0.300	0.310	7.62	7.87
R	0.178	0.186	4.52	4.72
S	0.220	0.240	5.59	6.10
V	0.182	0.194	4.62	4.93

STYLE 1:
PIN 1. GROUND
2. + OUTPUT
3. + SUPPLY
4. – OUTPUT

CASE 344E–01
ISSUE B

PACKAGE DIMENSIONS — CONTINUED

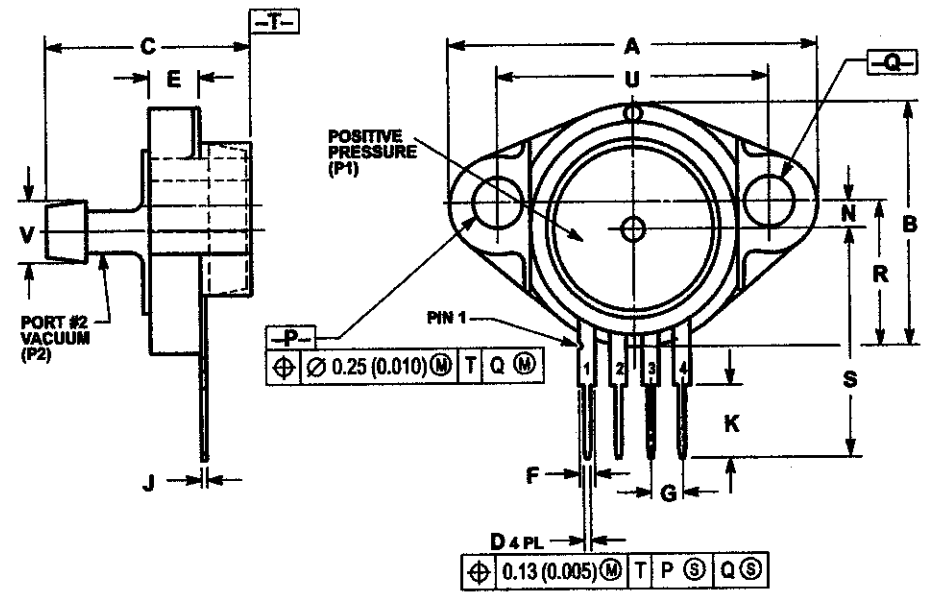


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.080	1.120	27.43	28.45
B	0.740	0.760	18.80	19.30
C	0.630	0.650	16.00	16.51
D	0.016	0.020	0.41	0.51
E	0.160	0.180	4.06	4.57
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.220	0.240	5.58	6.10
N	0.070	0.080	1.78	2.03
P	0.150	0.160	3.81	4.06
Q	0.150	0.160	3.81	4.06
R	0.440	0.460	11.18	11.68
S	0.695	0.725	17.65	18.42
U	0.840	0.860	21.34	21.84
V	0.182	0.194	4.62	4.92

STYLE 1:
PIN 1. GROUND
2. V (+) OUT
3. V SUPPLY
4. V (–) OUT

CASE 344F–01
ISSUE B



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D	0.016	0.020	0.41	0.51
E	0.160	0.180	4.06	4.57
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.220	0.240	5.58	6.10
N	0.070	0.080	1.78	2.03
P	0.150	0.160	3.81	4.06
Q	0.150	0.160	3.81	4.06
R	0.440	0.460	11.18	11.68
S	0.695	0.725	17.65	18.42
U	0.840	0.860	21.34	21.84
V	0.182	0.194	4.62	4.92

STYLE 1:
PIN 1. GROUND
2. V (+) OUT
3. V SUPPLY
4. V (–) OUT

CASE 344G–01
ISSUE B

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3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

Low Cost Low Power Instrumentation Amplifier

AD620

FEATURES

Easy to use
- Gain set with one external resistor (Gain range 1 to 10,000)
- Wide power supply range (±2.3 V to ±18 V)
- Higher performance than 3 op amp IA designs
- Available in 8-lead DIP and SOIC packaging
- Low power, 1.3 mA max supply current

Excellent dc performance (B grade)
- 50 µV max, input offset voltage
- 0.6 µV/°C max, input offset drift
- 1.0 nA max, input bias current
- 100 dB min common-mode rejection ratio (G = 10)

Low noise
- 9 nV/√Hz @ 1 kHz, input voltage noise
- 0.28 µV p-p noise (0.1 Hz to 10 Hz)

Excellent ac specifications
- 120 kHz bandwidth (G = 100)
- 15 µs settling time to 0.01%

APPLICATIONS

Weigh scales
ECG and medical instrumentation
Transducer interface
Data acquisition systems
Industrial process controls
Battery-powered and portable equipment

CONNECTION DIAGRAM

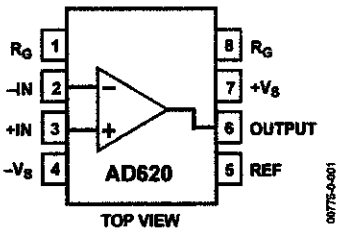

Figure 1. 8-Lead PDIP (N), CERDIP (Q), and SOIC (R) Packages

PRODUCT DESCRIPTION

The AD620 is a low cost, high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 10,000. Furthermore, the AD620 features 8-lead SOIC and DIP packaging that is smaller than discrete designs and offers lower power (only 1.3 mA max supply current), making it a good fit for battery-powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 µV max, and offset drift of 0.6 µV/°C max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications, such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superβeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/√Hz at 1 kHz, 0.28 µV p-p in the 0.1 Hz to 10 Hz band, and 0.1 pA/√Hz input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 µs to 0.01%, and its cost is low enough to enable designs with one in-amp per channel.

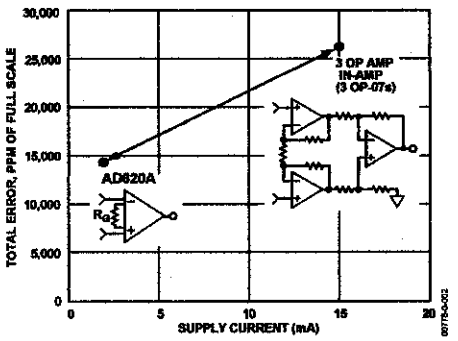

Figure 2. Three Op Amp IA Designs vs. AD620

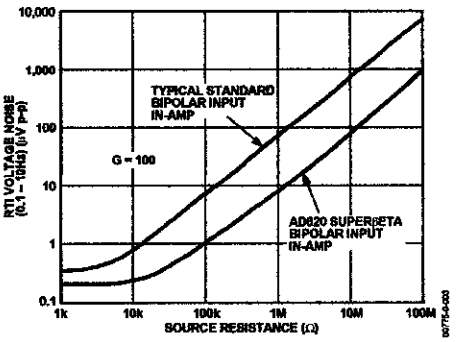

Figure 3. Total Voltage Noise vs. Source Resistance

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703

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SPECIFICATIONS

Typical @ 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

Table 1.

Parameter	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Unit
GAIN	G = 1 + (49.4 kΩ/R_G)										
Gain Range		1		10,000	1		10,000	1		10,000	
Gain Error[2]	V_{OUT} = ±10 V										
G = 1			0.03	0.10		0.01	0.02		0.03	0.10	%
G = 10			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 100			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
Nonlinearity	V_{OUT} = −10 V to +10 V										
G = 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
G = 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
Gain vs. Temperature											
	G = 1			10			10			10	ppm/°C
	Gain >1[2]			−50			−50			−50	ppm/°C
VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
Input Offset, V_{OSI}	V_S = ±5 V to ± 15 V		30	125		15	50		30	125	µV
Overtemperature	V_S = ±5 V to ± 15 V			185			85			225	µV
Average TC	V_S = ±5 V to ± 15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Output Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
	V_S = ± 5 V			1500			750			1500	µV
Overtemperature	V_S = ±5 V to ± 15 V			2000			1000			2000	µV
Average TC	V_S = ±5 V to ± 15 V		5.0	15		2.5	7.0		5.0	15	µV/°C
Offset Referred to the Input vs. Supply (PSR)	V_S = ±2.3 V to ±18 V										
G = 1		80	100		80	100		80	100		dB
G = 10		95	120		100	120		95	120		dB
G = 100		110	140		120	140		110	140		dB
G = 1000		110	140		120	140		110	140		dB
INPUT CURRENT											
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Overtemperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
Overtemperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10‖2			10‖2			10‖2		GΩ_pF
Common-Mode			10‖2			10‖2			10‖2		GΩ_pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	V
Overtemperature		$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	V
	V_S = ± 5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	V
Overtemperature		$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.1		$+V_S$ + 2.1	$-V_S$ + 2.3		$+V_S$ − 1.4	V

Parameter	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Unit
Common-Mode Rejection											
Ratio DC to 60 Hz with											
1 kΩ Source Imbalance	V_{CM} = 0 V to ± 10 V										
G = 1		73	90		80	90		73	90		dB
G = 10		93	110		100	110		93	110		dB
G = 100		110	130		120	130		110	130		dB
G = 1000		110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ										
	V_S = ±2.3 V to ± 5 V	$-V_S$ + 1.1		$+V_S$ – 1.2	$-V_S$ + 1.1		$+V_S$ – 1.2	$-V_S$ + 1.1		$+V_S$ – 1.2	V
Overtemperature		$-V_S$ + 1.4		$+V_S$ – 1.3	$-V_S$ + 1.4		$+V_S$ – 1.3	$-V_S$ + 1.6		$+V_S$ – 1.3	V
	V_S = ±5 V to ± 18 V	$-V_S$ + 1.2		$+V_S$ – 1.4	$-V_S$ + 1.2		$+V_S$ – 1.4	$-V_S$ + 1.2		$+V_S$ – 1.4	V
Overtemperature		$-V_S$ + 1.6		$+V_S$ – 1.5	$-V_S$ + 1.6		$+V_S$ – 1.5	$-V_S$ + 2.3		$+V_S$ – 1.5	V
Short Circuit Current			±18			±18			±18		mA
DYNAMIC RESPONSE											
Small Signal –3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step										
G = 1–100			15			15			15		µs
G = 1000			150			150			150		µs
NOISE											
Voltage Noise, 1 kHz	$Total\ RTI\ Noise = \sqrt{(e^2_{ni}) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/√Hz
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	µV p-p
G = 10			0.55			0.55	0.8		0.55	0.8	µV p-p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			10			10			10		pA p-p
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		50	60		50	60		50	60	µA
Voltage Range		$-V_S$ + 1.6		$+V_S$ – 1.6	$-V_S$ + 1.6		$+V_S$ – 1.6	$-V_S$ + 1.6		$+V_S$ – 1.6	V
Gain to Output		1 ± 0.0001			1 ± 0.0001			1 ± 0.0001			
POWER SUPPLY											
Operating Range[4]		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Overtemperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance		–40 to +85			–40 to +85			–55 to +125			°C

[1] See Analog Devices military data sheet for 883B tested specifications.
[2] Does not include effects of external resistor R_G.
[3] One input grounded. G = 1.
[4] This is defined as the same supply range that is used to specify PSR.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation[1]	650 mW
Input Voltage (Common-Mode)	$\pm V_S$
Differential Input Voltage	25 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range (Q)	−65°C to +150°C
Storage Temperature Range (N, R)	−65°C to +125°C
Operating Temperature Range	
AD620 (A, B)	−40°C to +85°C
AD620 (S)	−55°C to +125°C
Lead Temperature Range	
(Soldering 10 seconds)	300°C

[1] Specification is for device in free air:
8-Lead Plastic Package: θ_{JA} = 95°C
8-Lead CERDIP Package: θ_{JA} = 110°C
8-Lead SOIC Package: θ_{JA} = 155°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

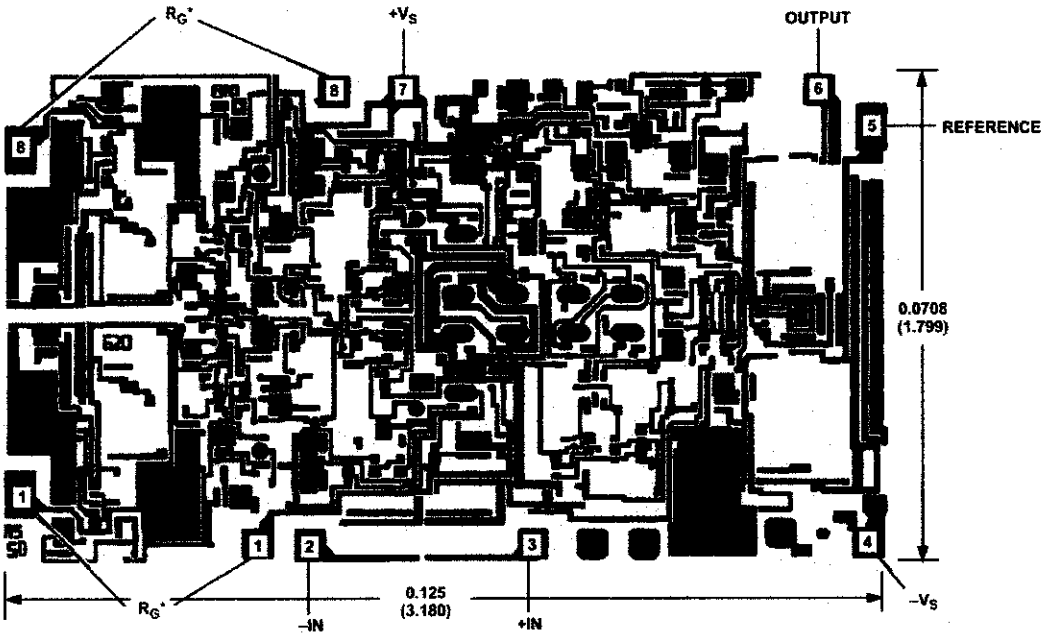


Figure 4. Metallization Photograph.
Dimensions shown in inches and (mm).

Contact sales for latest dimensions.

YPICAL PERFORMANCE CHARACTERISTICS

@ 25°C, V_S = ±15 V, R_L = 2 kΩ, unless otherwise noted.)

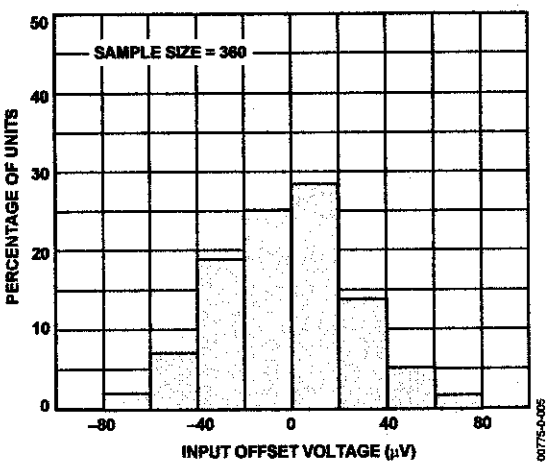


Figure 5. Typical Distribution of Input Offset Voltage

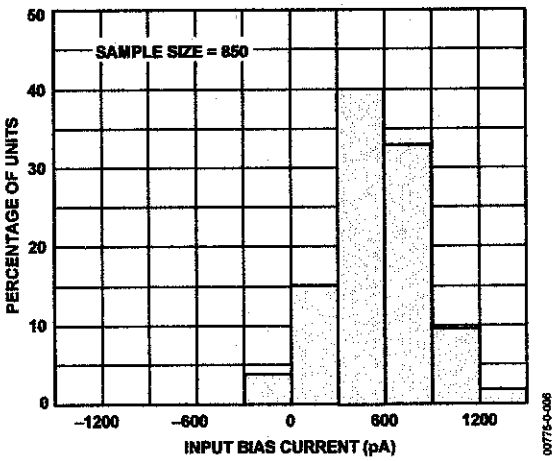


Figure 6. Typical Distribution of Input Bias Current

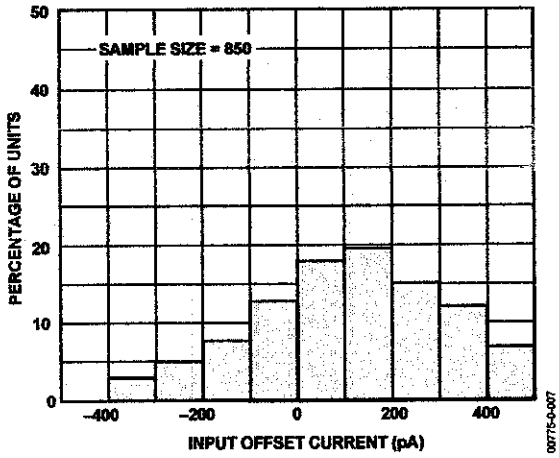


Figure 7. Typical Distribution of Input Offset Current

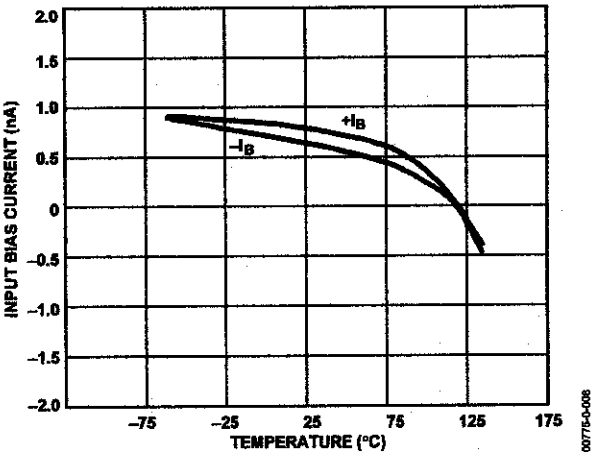


Figure 8. Input Bias Current vs. Temperature

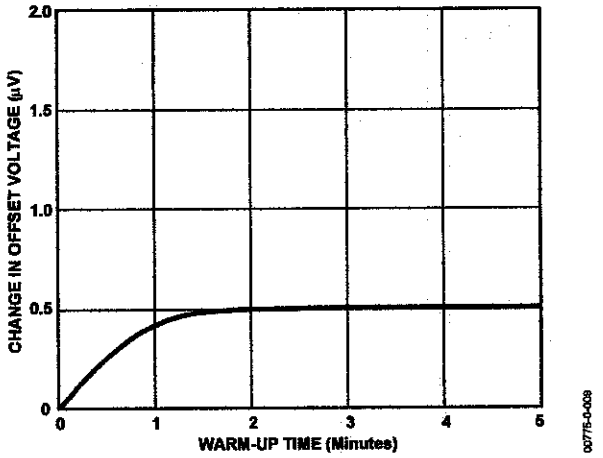


Figure 9. Change in Input Offset Voltage vs. Warm-Up Time

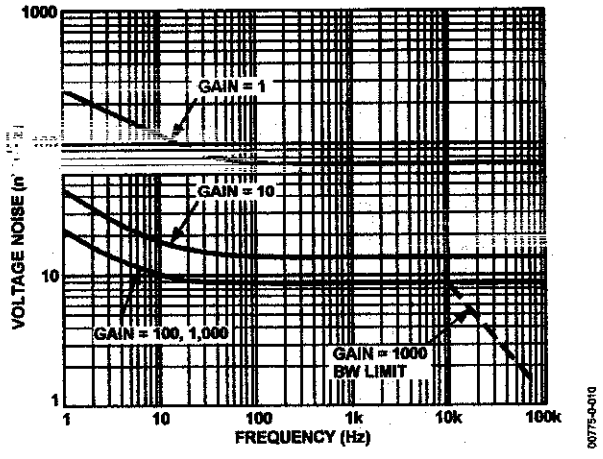


Figure 10. Voltage Noise Spectral Density vs. Frequency (G = 1–1000)

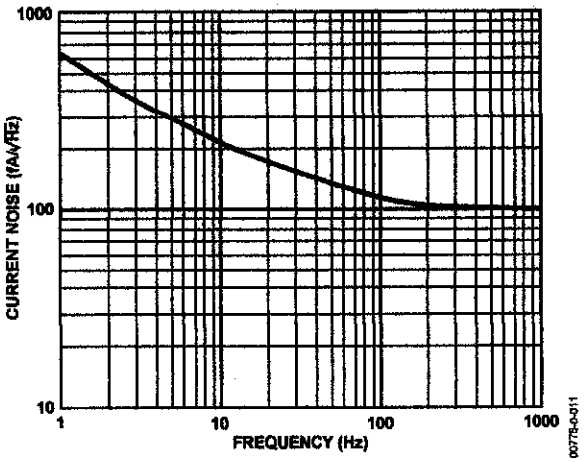


Figure 11. Current Noise Spectral Density vs. Frequency

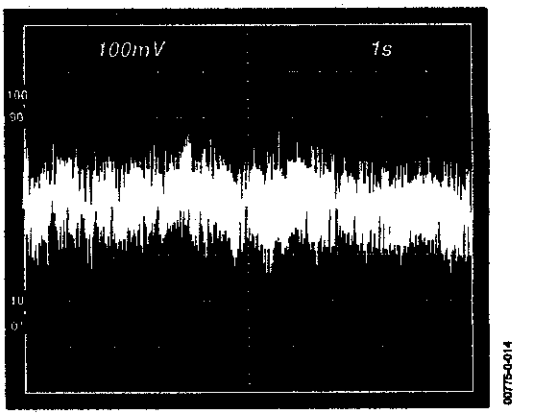


Figure 14. 0.1 Hz to 10 Hz Current Noise, 5 pA/Div

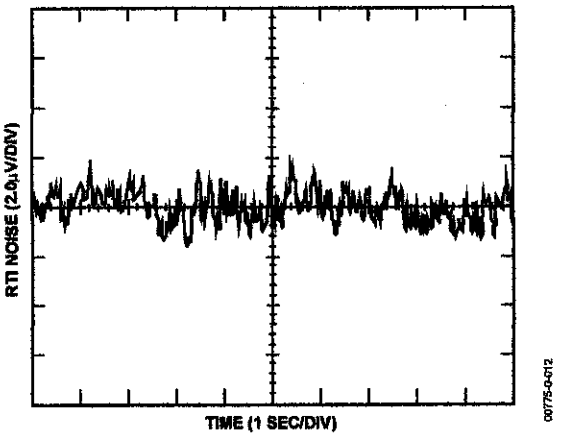


Figure 12. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

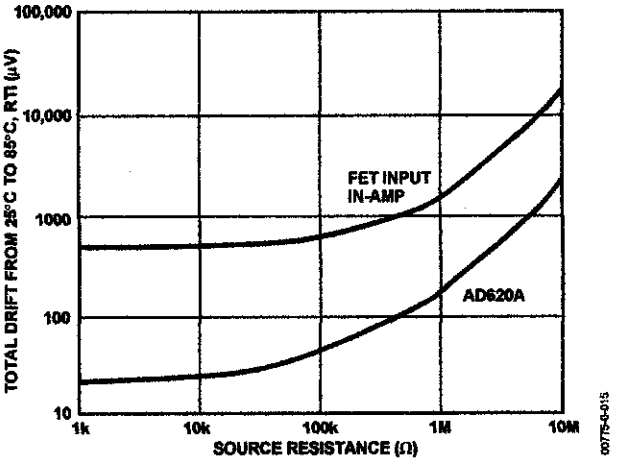


Figure 15. Total Drift vs. Source Resistance

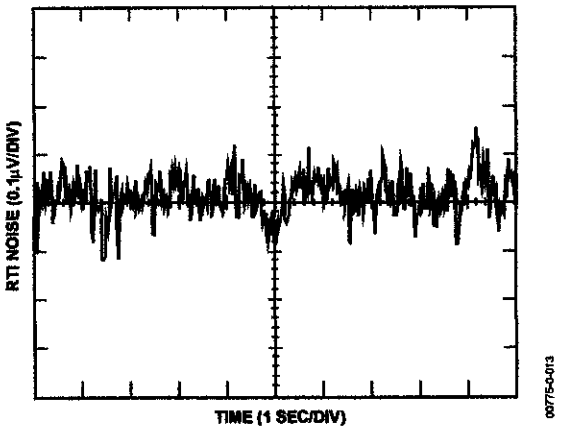


Figure 13. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

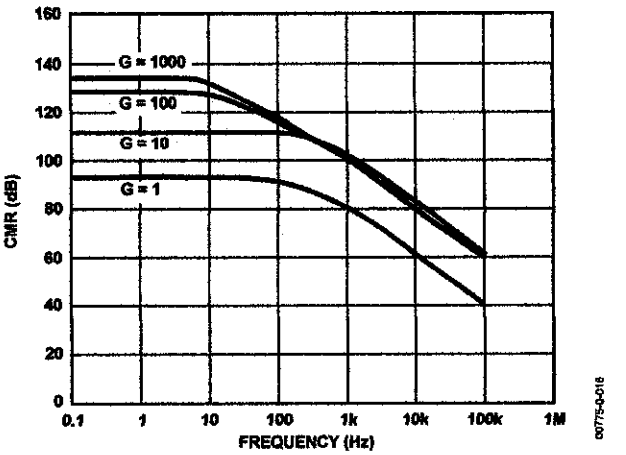


Figure 16. Typical CMR vs. Frequency, RTI, Zero to 1 kΩ Source Imbalance

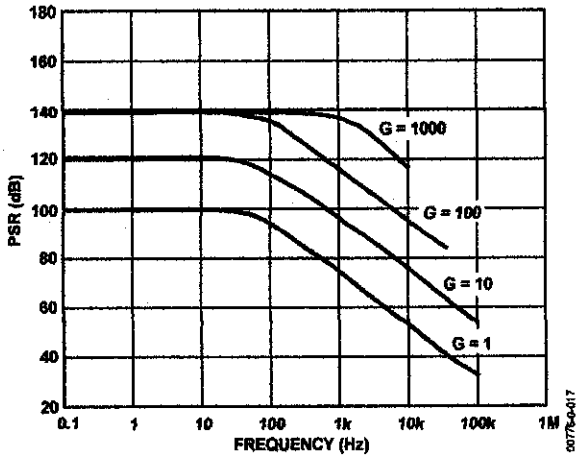


Figure 17. Positive PSR vs. Frequency, RTI (G = 1–1000)

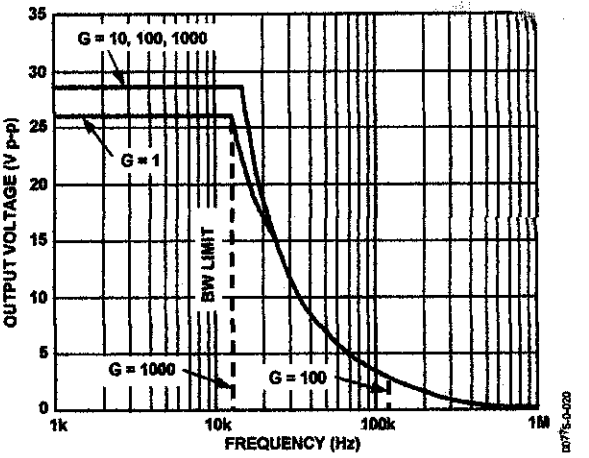


Figure 20. Large Signal Frequency Response

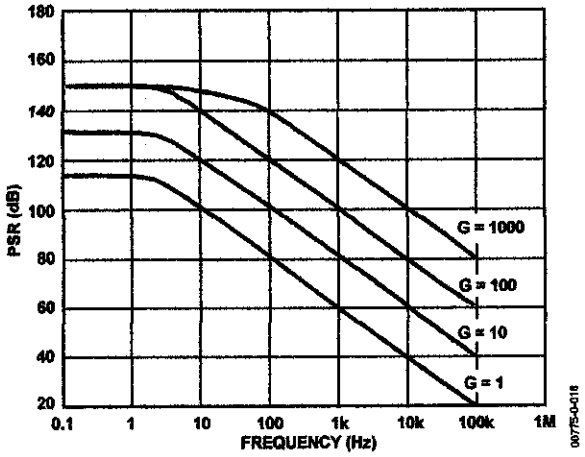


Figure 18. Negative PSR vs. Frequency, RTI (G = 1–1000)

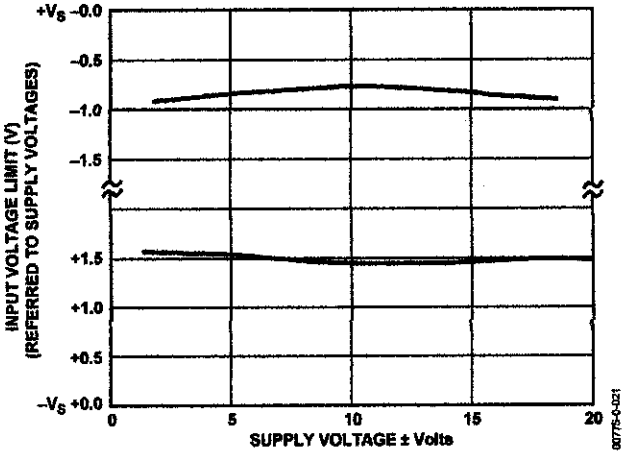


Figure 21. Input Voltage Range vs. Supply Voltage, G = 1

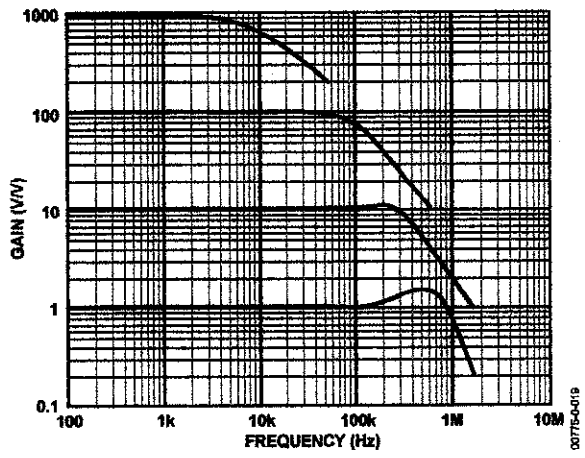


Figure 19. Gain vs. Frequency

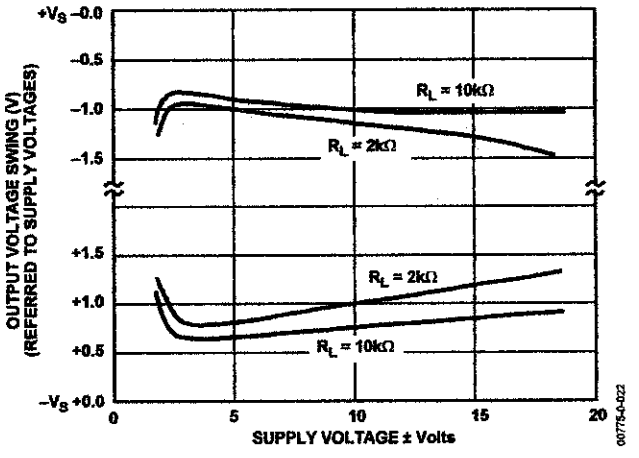


Figure 22. Output Voltage Swing vs. Supply Voltage, G = 10

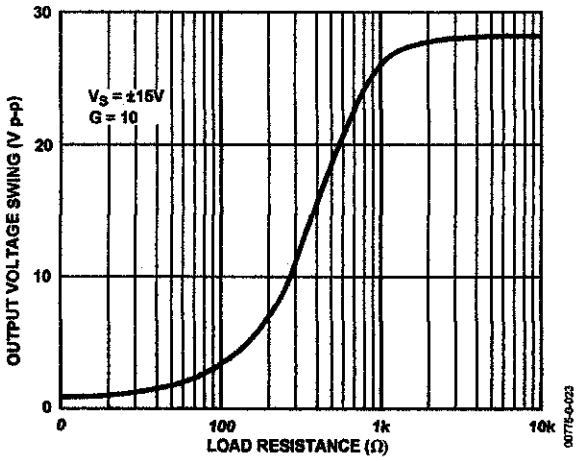


Figure 23. Output Voltage Swing vs. Load Resistance

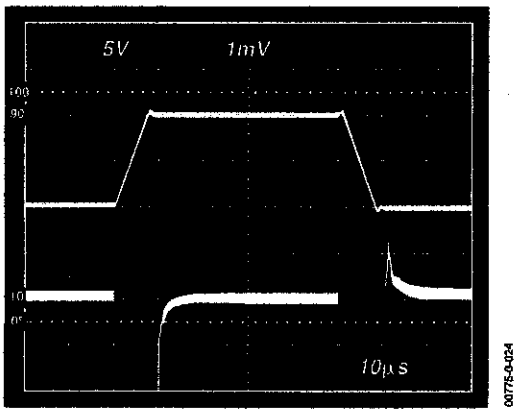


Figure 24. Large Signal Pulse Response and Settling Time G = 1 (0.5 mV = 0.01%)

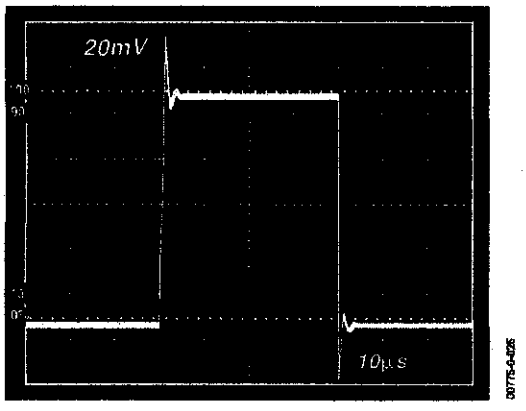


Figure 25. Small Signal Response, G = 1, R_L = 2 kΩ, C_L = 100 pF

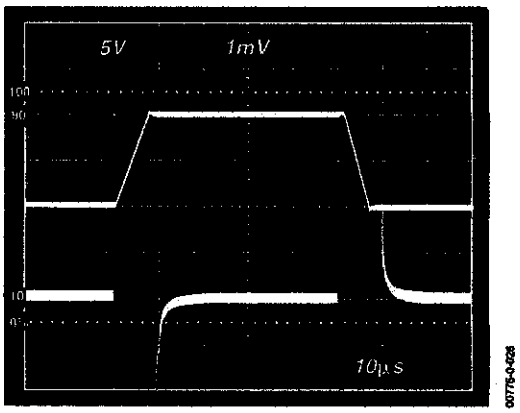


Figure 26. Large Signal Response and Settling Time, G = 10 (0.5 mV = 0.01%)

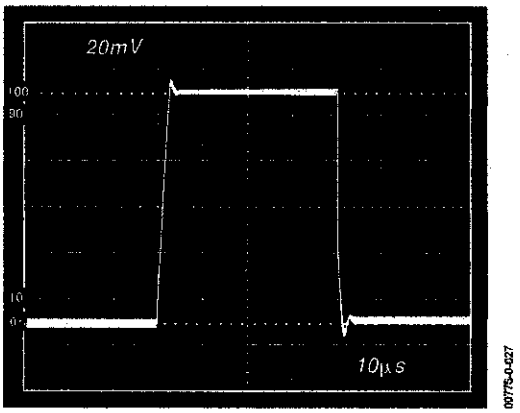


Figure 27. Small Signal Response, G = 10, R_L = 2 kΩ, C_L = 100 pF

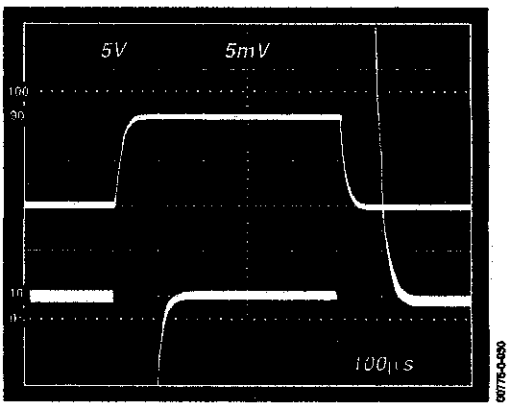


Figure 28. Large Signal Response and Settling Time, G = 100 (0.5 mV = 0.01%)

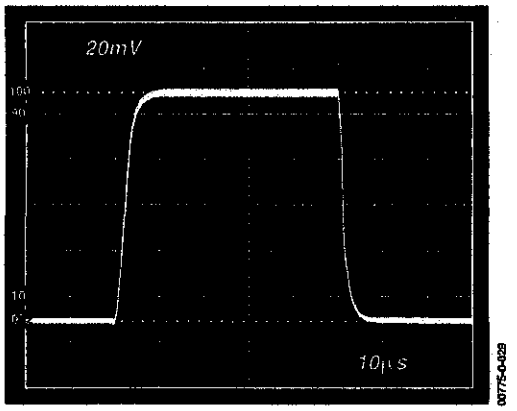


Figure 29. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, C_L = 100 pF

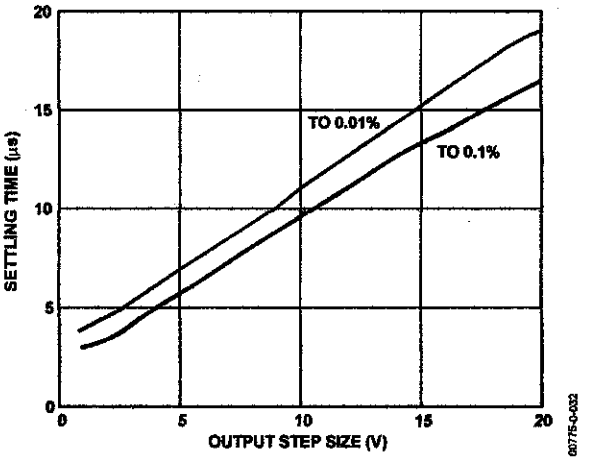


Figure 32. Settling Time vs. Step Size (G = 1)

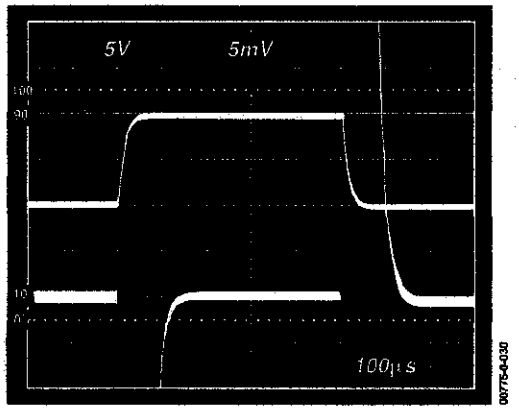


Figure 30. Large Signal Response and Settling Time, G = 1000 (0.5 mV = 0.01%)

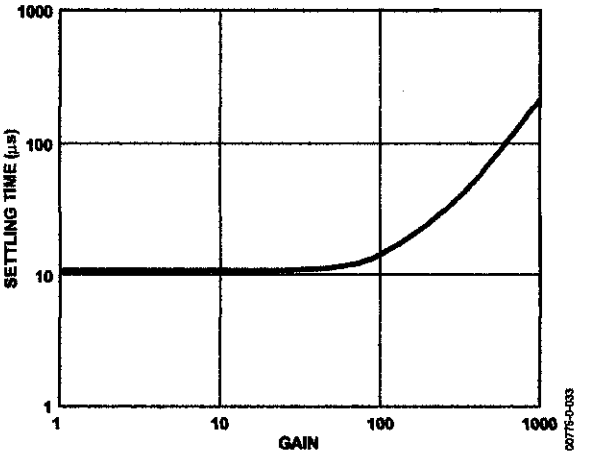


Figure 33. Settling Time to 0.01% vs. Gain, for a 10 V Step

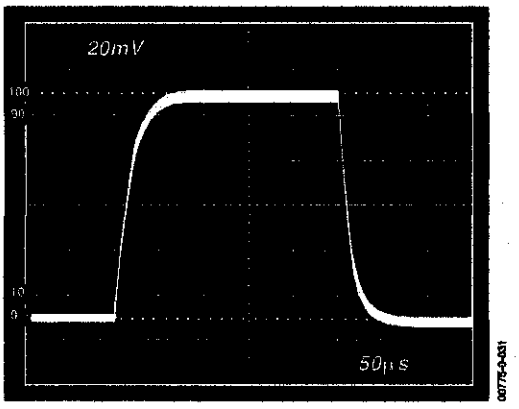


Figure 31. Small Signal Pulse Response, G = 1000, R_L = 2 kΩ, C_L = 100 pF

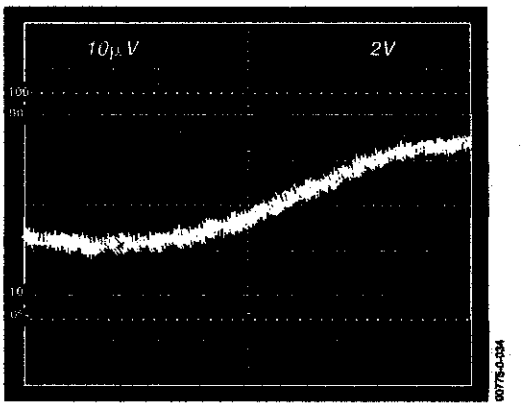


Figure 34. Gain Nonlinearity, G = 1, R_L = 10 kΩ (10 µV = 1 ppm)

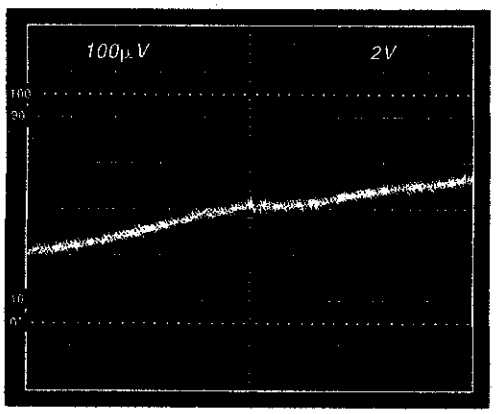


Figure 35. Gain Nonlinearity, G = 100, R_L = 10 kΩ
(100 µV = 10 ppm)

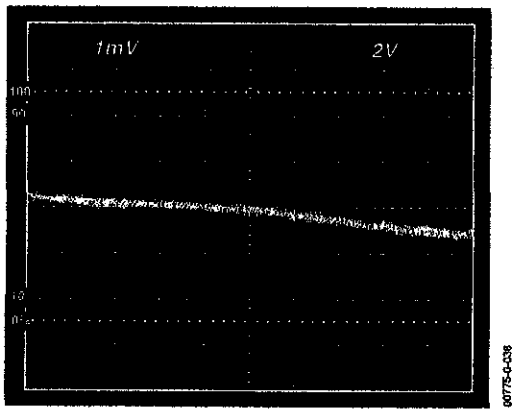


Figure 36. Gain Nonlinearity, G = 1000, R_L = 10 kΩ
(1 mV = 100 ppm)

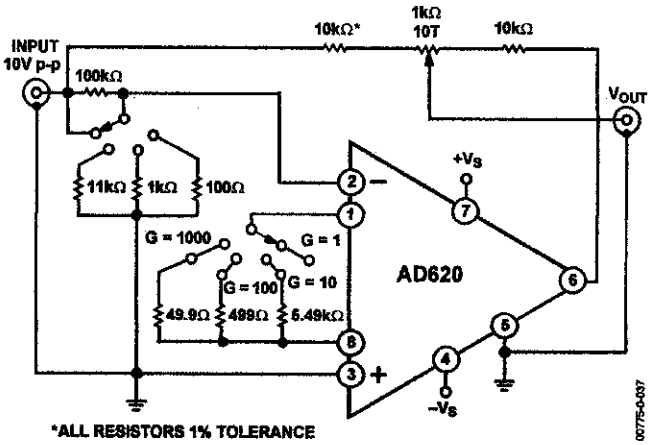


Figure 37. Settling Time Test Circuit

'HEORY OF OPERATION

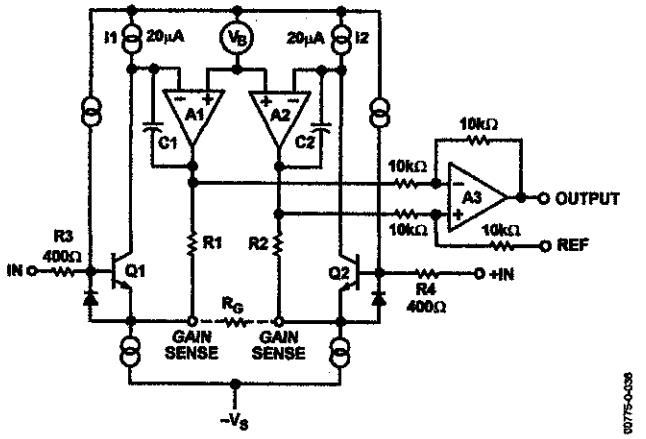


Figure 38. Simplified Schematic of AD620

'he AD620 is a monolithic instrumentation amplifier based on modification of the classic three op amp approach. Absolute alue trimming allows the user to program gain *accurately* o 0.15% at G = 100) with only one resistor. Monolithic onstruction and laser wafer trimming allow the tight matching nd tracking of circuit components, thus ensuring the high level f performance inherent in this circuit.

The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision (Figure 38), yet offer 10× lower input bias current thanks to Superβeta processing. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1 and Q2, thereby impressing the input voltage across the external gain setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by $G = (R1 + R2)/R_G + 1$. The unity-gain subtractor, A3, removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain related errors. (b) The gain-bandwidth product (determined by C1 and C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 9 nV/√Hz, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor.

The gain equation is then

$$G = \frac{49.4k\Omega}{R_G} + 1$$

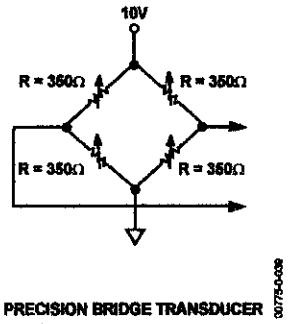
$$R_G = \frac{49.4k\Omega}{G-1}$$

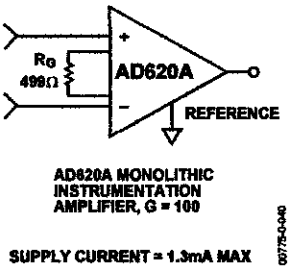
Make vs. Buy: a Typical Bridge Application Error Budget

The AD620 offers improved performance over "homebrew" three op amp IA designs, along with smaller size, fewer components, and 10× lower supply current. In the typical application, shown in Figure 39, a gain of 100 is required to amplify a bridge output of 20 mV full-scale over the industrial temperature range of −40°C to +85°C. Table 3 shows how to calculate the effect various error sources have on circuit accuracy.

Regardless of the system in which it is being used, the AD620 provides greater accuracy at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, an autogain/autozero cycle will remove all absolute accuracy and drift errors, leaving only the resolution errors of gain, nonlinearity, and noise, thus allowing full 14-bit accuracy.

Note that for the homebrew circuit, the OP07 specifications for input voltage offset and noise have been multiplied by √2. This is because a three op amp type in-amp has two op amps at its inputs, both contributing to the overall input error.





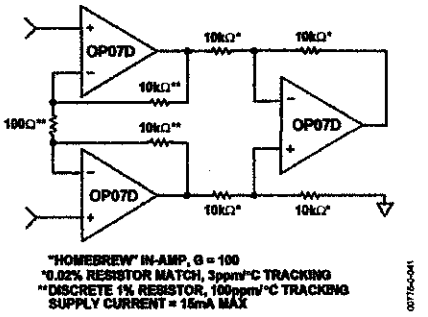


Figure 39. Make vs. Buy

Table 3. Make vs. Buy Error Budget

Error Source	AD620 Circuit Calculation	"Homebrew" Circuit Calculation	Error, ppm of Full Scale AD620	Homebrew
ABSOLUTE ACCURACY at T_A = 25°C				
Input Offset Voltage, µV	125 µV/20 mV	(150 µV × √2)/20 mV	6,250	10,607
Output Offset Voltage, µV	1000 µV/100 mV/20 mV	((150 µV × 2)/100)/20 mV	500	150
Input Offset Current, nA	2 nA ×350 Ω/20 mV	(6 nA ×350 Ω)/20 mV	18	53
CMR, dB	110 dB(3.16 ppm) ×5 V/20 mV	(0.02% Match × 5 V)/20 mV/100	791	500
		Total Absolute Error	7,559	11,310
DRIFT TO 85°C				
Gain Drift, ppm/°C	(50 ppm + 10 ppm) ×60°C	100 ppm/°C Track × 60°C	3,600	6,000
Input Offset Voltage Drift, µV/°C	1 µV/°C × 60°C/20 mV	(2.5 µV/°C × √2 × 60°C)/20 mV	3,000	10,607
Output Offset Voltage Drift, µV/°C	15 µV/°C × 60°C/100 mV/20 mV	(2.5 µV/°C × 2 × 60°C)/100 mV/20 mV	450	150
		Total Drift Error	7,050	16,757
RESOLUTION				
Gain Nonlinearity, ppm of Full Scale	40 ppm	40 ppm	40	40
Typ 0.1 Hz to 10 Hz Voltage Noise, µV p-p	0.28 µV p-p/20 mV	(0.38 µV p-p × √2)/20 mV	14	27
		Total Resolution Error	54	67
		Grand Total Error	14,663	28,134

G = 100, V_S = ±15 V.
(All errors are min/max and referred to input.)

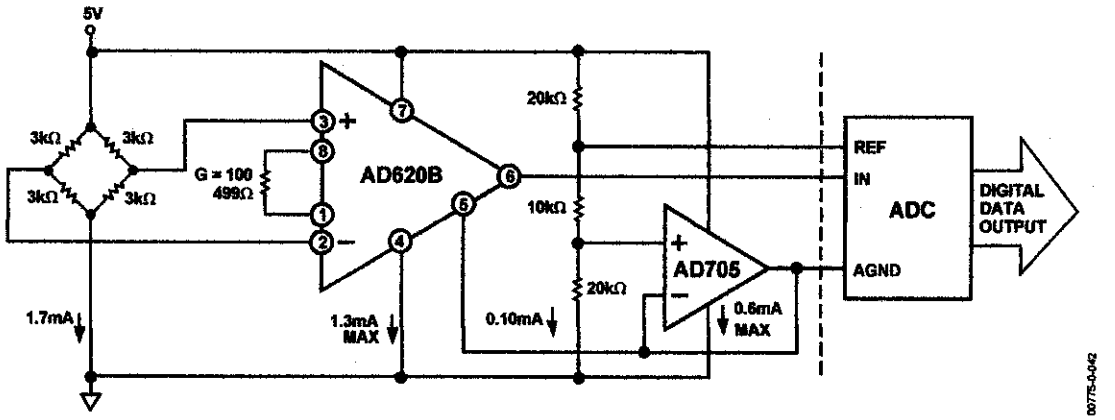


Figure 40. A Pressure Monitor Circuit that Operates on a 5 V Single Supply

'ressure Measurement

ılthough useful in many bridge applications, such as weigh cales, the AD620 is especially suitable for higher resistance ressure sensors powered at lower voltages where small size and ow power become more significant.

igure 40 shows a 3 kΩ pressure transducer bridge powered rom 5 V. In such a circuit, the bridge consumes only 1.7 mA. ıdding the AD620 and a buffered voltage divider allows the ignal to be conditioned for only 3.8 mA of total supply current.

mall size and low cost make the AD620 especially attractive for oltage output pressure transducers. Since it delivers low noise nd drift, it will also serve applications such as diagnostic oninvasive blood pressure measurement.

Medical ECG

The low current noise of the AD620 allows its use in ECG monitors (Figure 41) where high source resistances of 1 MΩ or higher are not uncommon. The AD620's low power, low supply voltage requirements, and space-saving 8-lead mini-DIP and SOIC package offerings make it an excellent choice for battery-powered data recorders.

Furthermore, the low bias currents and low current noise, coupled with the low voltage noise of the AD620, improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

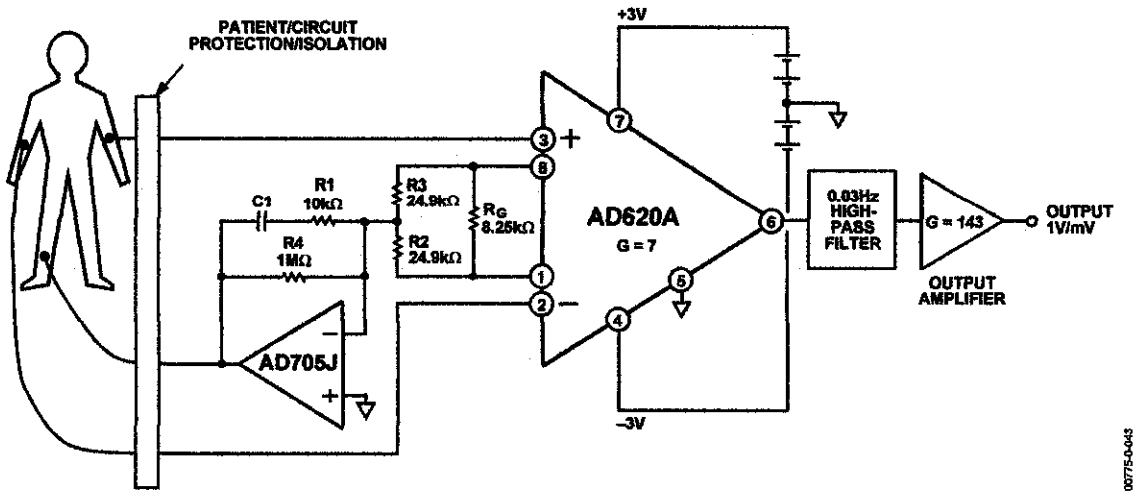


Figure 41. A Medical ECG Monitor Circuit

Precision V-I Converter

The AD620, along with another op amp and two resistors, makes a precision current source (Figure 42). The op amp buffers the reference terminal to maintain good CMR. The output voltage, V_X, of the AD620 appears across R1, which converts it to a current. This current, less only the input bias current of the op amp, then flows out to the load.

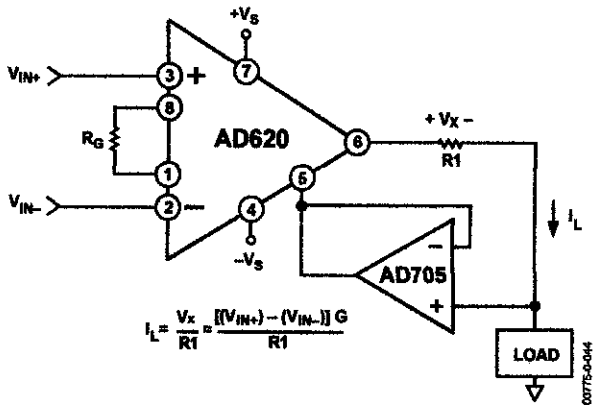


Figure 42. Precision Voltage-to-Current Converter (Operates on 1.8 mA, ±3 V)

GAIN SELECTION

The AD620's gain is resistor-programmed by R_G, or more precisely, by whatever impedance appears between Pins 1 and 8. The AD620 is designed to offer accurate gains using 0.1% to 1% resistors. Table 4 shows required values of R_G for various gains. Note that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For any arbitrary gain, R_G can be calculated by using the formula:

$$R_G = \frac{49.4k\Omega}{G-1}$$

To minimize gain error, avoid high parasitic resistance in series with R_G; to minimize gain drift, R_G should have a low TC—less than 10 ppm/°C—for the best performance.

Table 4. Required Values of Gain Resistors

1% Std Table Value of R_G(Ω)	Calculated Gain	0.1% Std Table Value of R_G(Ω)	Calculated Gain
9.9 k	1.990	49.3 k	2.002
2.4 k	4.984	12.4 k	4.984
.49 k	9.998	5.49 k	9.998
.61 k	19.93	2.61 k	19.93
.00 k	50.40	1.01 k	49.91
99	100.0	499	100.0
49	199.4	249	199.4
00	495.0	98.8	501.0
9.9	991.0	49.3	1,003.0

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD620 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains, and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as

Total Error RTI = input error + (output error/G)

Total Error RTO = (input error × G) + output error

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

INPUT PROTECTION

The AD620 features 400 Ω of series thin film resistance at its inputs and will safely withstand input overloads of up to ±15 V or ±60 mA for several hours. This is true for all gains and power on and off, which is particularly important since the signal source and amplifier may be powered separately. For longer time periods, the current should not exceed 6 mA ($I_{IN} \leq V_{IN}/400\ \Omega$). For input overloads beyond the supplies, clamping the inputs to the supplies (using a low leakage diode such as an FD333) will reduce the required resistance, yielding lower noise.

RF INTERFERENCE

All instrumentation amplifiers rectify small out of band signals. The disturbance may appear as a small dc voltage offset. High frequency signals can be filtered with a low pass R-C network placed at the input of the instrumentation amplifier. Figure 43 demonstrates such a configuration. The filter limits the input signal according to the following relationship:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$

C_D affects the difference signal. C_C affects the common-mode signal. Any mismatch in $R \times C_C$ will degrade the AD620's CMRR. To avoid inadvertently reducing CMRR-bandwidth performance, make sure that C_C is at least one magnitude smaller than C_D. The effect of mismatched C_Cs is reduced with a larger C_D:C_C ratio.

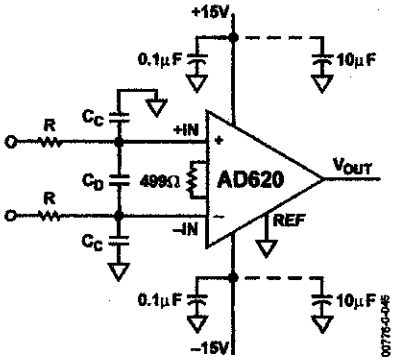


Figure 43. Circuit to Attenuate RF Interference

COMMON-MODE REJECTION

Instrumentation amplifiers, such as the AD620, offer high CMR, which is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR, the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications, shielded cables are used to minimize noise; for best CMR over frequency, the shield should be properly driven. Figure 44 and Figure 45 show active data guards that are configured to improve ac common-mode rejections by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

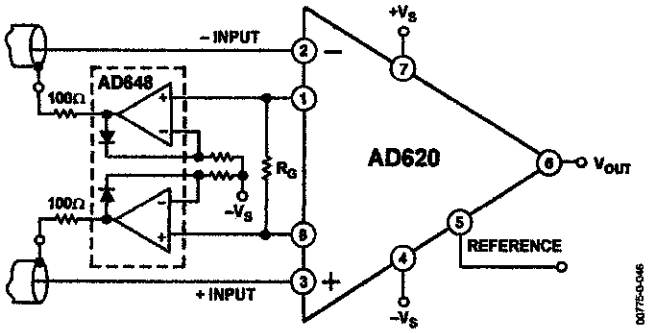


Figure 44. Differential Shield Driver

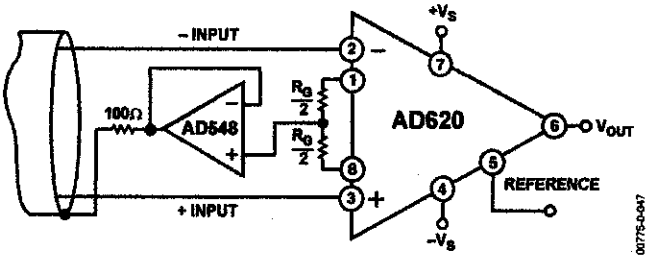


Figure 45. Common-Mode Shield Driver

GROUNDING

Since the AD620 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground."

To isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground pins (Figure 46). It would be convenient to use a single ground line; however, current through ground wires and PC runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground. These ground returns must be tied together at some point, usually best at the ADC package shown in Figure 46.

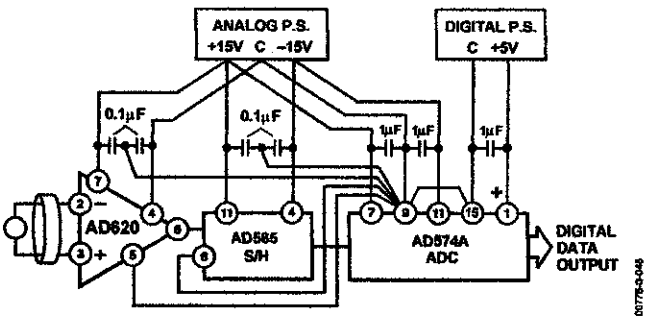


Figure 46. Basic Grounding Practice

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents. Therefore, when amplifying "floating" input sources, such as transformers or ac-coupled sources, there must be a dc path from each input to ground, as shown in Figure 47, Figure 48, and Figure 49. Refer to *A Designer's Guide to Instrumentation Amplifiers* (free from Analog Devices) for more information regarding in-amp applications.

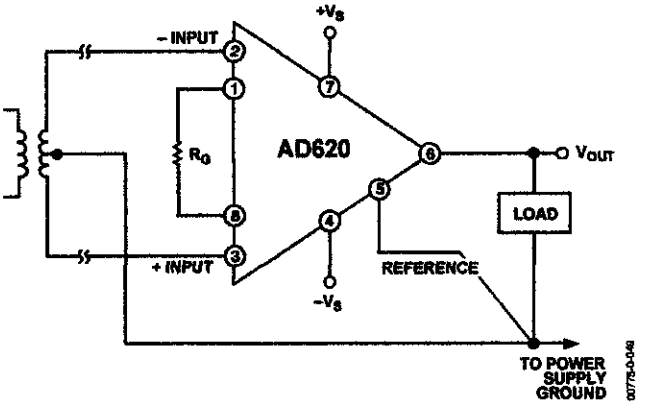


Figure 47. Ground Returns for Bias Currents with Transformer-Coupled Inputs

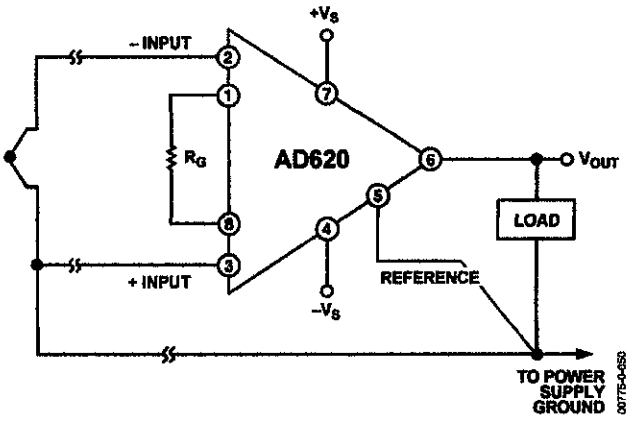


Figure 48. Ground Returns for Bias Currents with Thermocouple Inputs

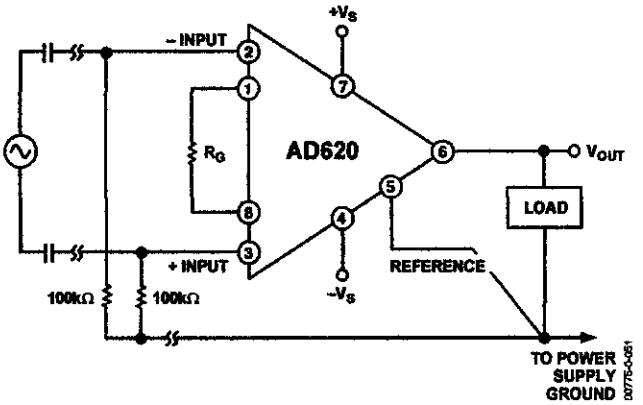
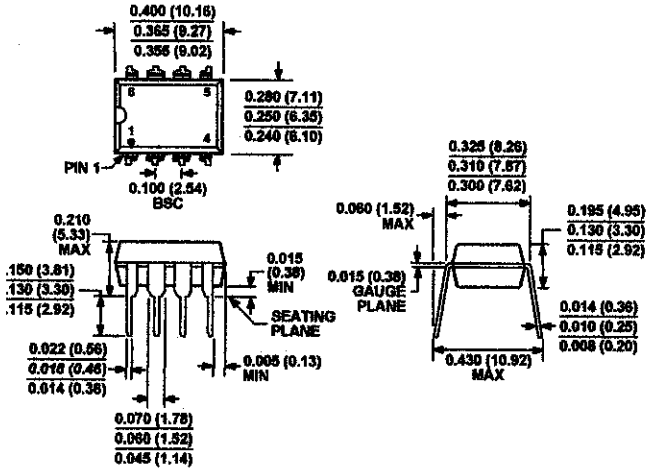


Figure 49. Ground Returns for Bias Currents with AC-Coupled Inputs

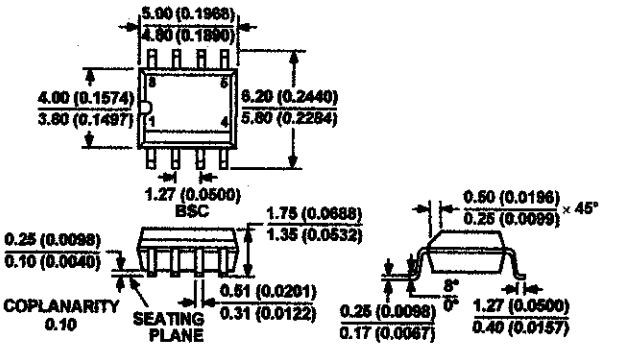
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 50. 8-Lead Plastic Dual In-Line Package [PDIP]

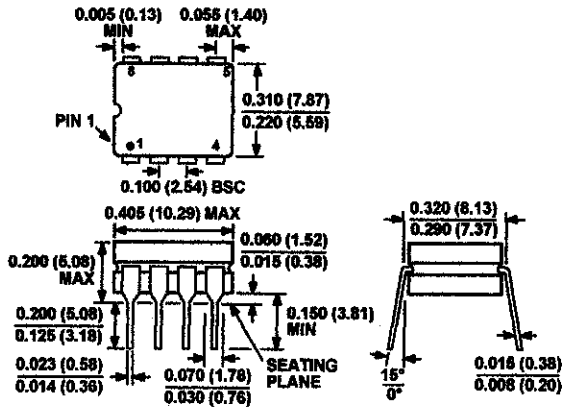
Narrow Body (N-8).
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 52. 8-Lead Standard Small Outline Package [SOIC]

Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 51. 8-Lead Ceramic Dual In-Line Package [CERDIP] (Q-8)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Option[1]
AD620AN	–40°C to +85°C	N-8
AD620ANZ[2]	–40°C to +85°C	N-8
AD620BN	–40°C to +85°C	N-8
AD620BNZ[2]	–40°C to +85°C	N-8
AD620AR	–40°C to +85°C	R-8
AD620ARZ[2]	–40°C to +85°C	R-8
AD620AR-REEL	–40°C to +85°C	13" REEL
AD620ARZ-REEL[2]	–40°C to +85°C	13" REEL
AD620AR-REEL7	–40°C to +85°C	7" REEL
AD620ARZ-REEL7[2]	–40°C to +85°C	7" REEL
AD620BR	–40°C to +85°C	R-8
AD620BRZ[2]	–40°C to +85°C	R-8
AD620BR-REEL	–40°C to +85°C	13" REEL
AD620BRZ-RL[2]	–40°C to +85°C	13" REEL
AD620BR-REEL7	–40°C to +85°C	7" REEL
AD620BRZ-R7[2]	–40°C to +85°C	7" REEL
AD620ACHIPS	–40°C to +85°C	Die Form
AD620SQ/883B	–55°C to +125°C	Q-8

N = Plastic DIP; Q = CERDIP; R = SOIC.
Z = Pb-free part.

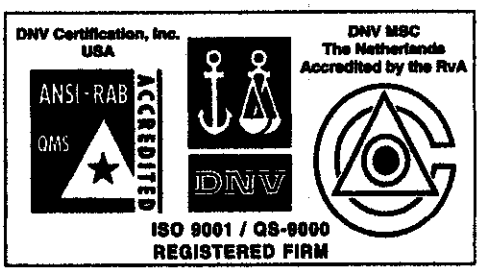
PIC16F87XA
Data Sheet

28/40/44-Pin Enhanced Flash Microcontrollers

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.

MICROCHIP

PIC16F87XA

28/40/44-Pin Enhanced Flash Microcontrollers

Devices Included in this Data Sheet:

- PIC16F873A
- PIC16F874A
- PIC16F876A
- PIC16F877A

High-Performance RISC CPU:

- Only 35 single-word instructions to learn
- All single-cycle instructions except for program branches, which are two-cycle
- Operating speed: DC – 20 MHz clock input
  DC – 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory, Up to 368 x 8 bytes of Data Memory (RAM), Up to 256 x 8 bytes of EEPROM Data Memory
- Pinout compatible to other 28-pin or 40/44-pin PIC16CXXX and PIC16FXXX microcontrollers

Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during Sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- Synchronous Serial Port (SSP) with SPI™ (Master mode) and I²C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) – 8 bits wide with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

Analog Features:

- 10-bit, up to 8-channel Analog-to-Digital Converter (A/D)
- Brown-out Reset (BOR)
- Analog Comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (V_{REF}) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs are externally accessible

Special Microcontroller Features:

- 100,000 erase/write cycle Enhanced Flash program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Data EEPROM Retention > 40 years
- Self-reprogrammable under software control
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Single-supply 5V In-Circuit Serial Programming
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving Sleep mode
- Selectable oscillator options
- In-Circuit Debug (ICD) via two pins

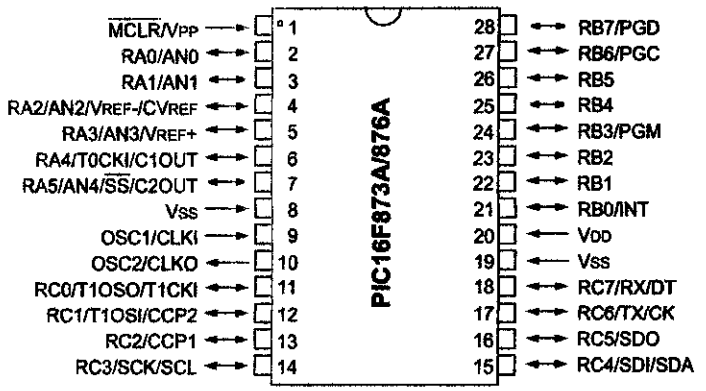
CMOS Technology:

- Low-power, high-speed Flash/EEPROM technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Commercial and Industrial temperature ranges
- Low-power consumption

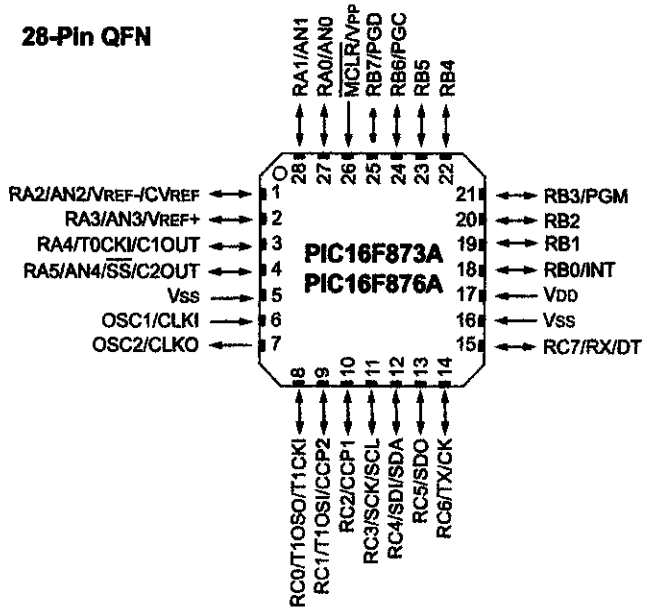
Device	Program Memory		Data SRAM (Bytes)	EEPROM (Bytes)	I/O	10-bit A/D (ch)	CCP (PWM)	MSSP		USART	Timers 8/16-bit	Comparators
	Bytes	# Single Word Instructions						SPI	Master I²C			
PIC16F873A	7.2K	4096	192	128	22	5	2	Yes	Yes	Yes	2/1	2
PIC16F874A	7.2K	4096	192	128	33	8	2	Yes	Yes	Yes	2/1	2
PIC16F876A	14.3K	8192	368	256	22	5	2	Yes	Yes	Yes	2/1	2
PIC16F877A	14.3K	8192	368	256	33	8	2	Yes	Yes	Yes	2/1	2

Pin Diagrams

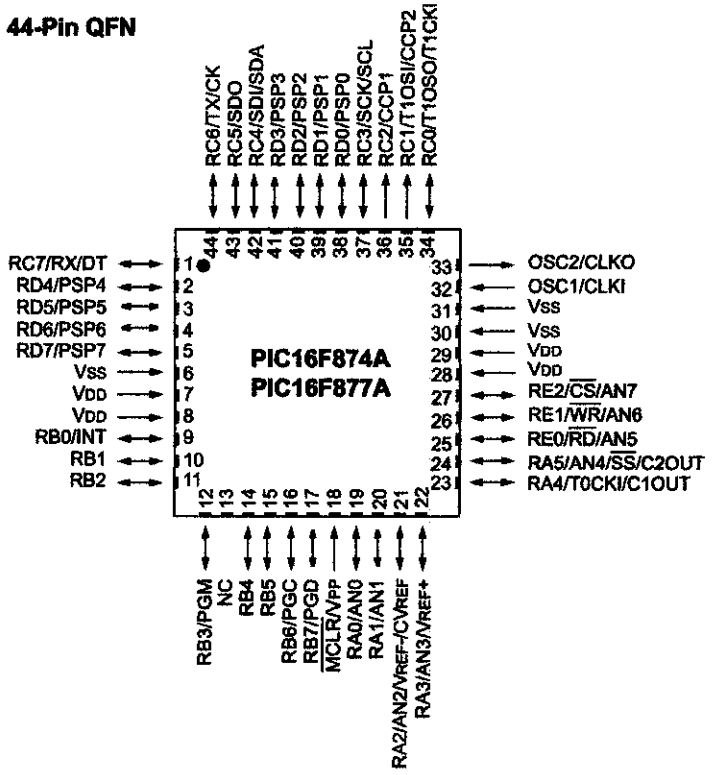
28-Pin PDIP, SOIC, SSOP



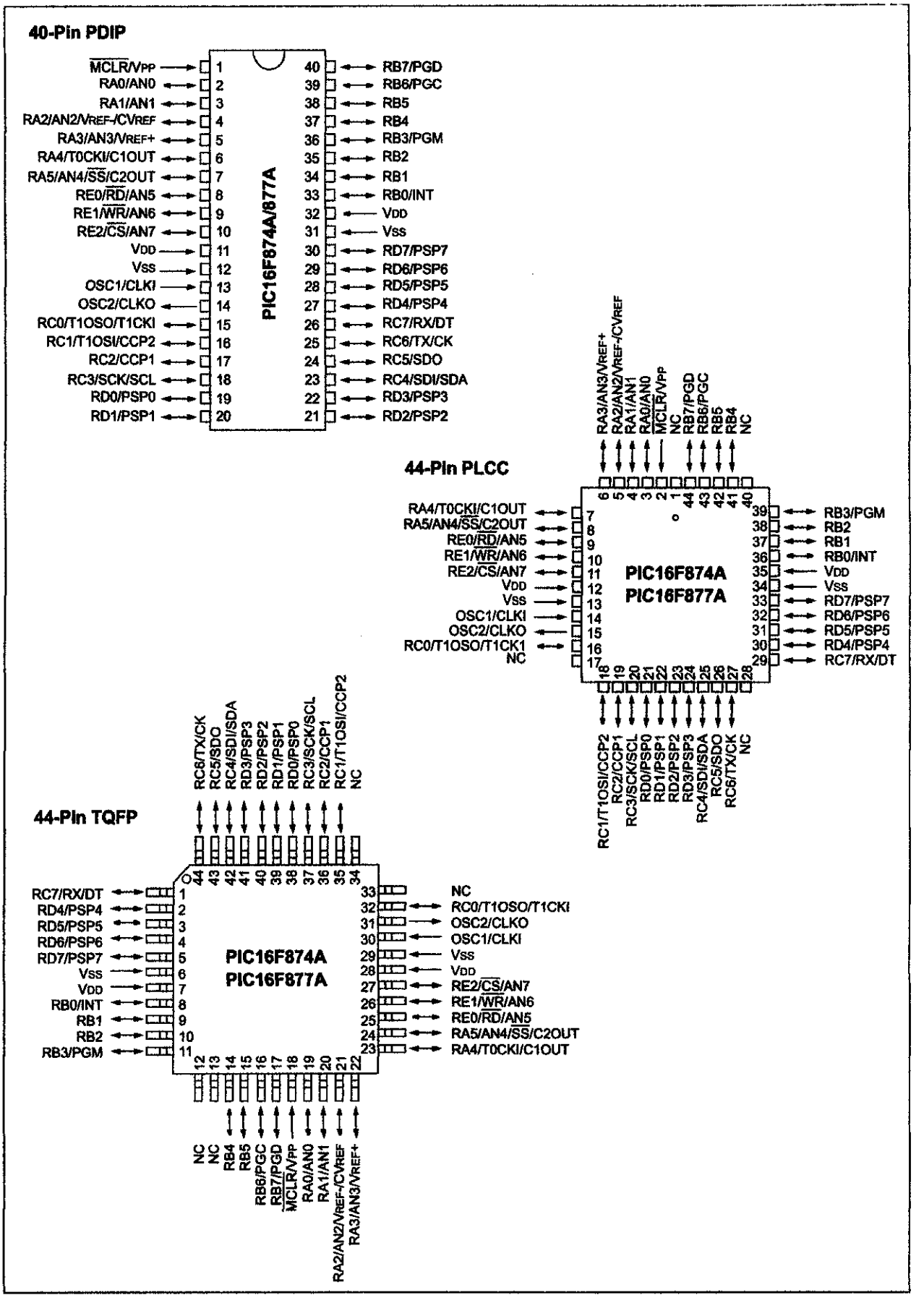
28-Pin QFN



44-Pin QFN



Pin Diagrams (Continued)



1.0 DEVICE OVERVIEW

This document contains device specific information about the following devices:

- PIC16F873A
- PIC16F874A
- PIC16F876A
- PIC16F877A

PIC16F873A/876A devices are available only in 28-pin packages, while PIC16F874A/877A devices are available in 40-pin and 44-pin packages. All devices in the PIC16F87XA family share common architecture with the following differences:

- The PIC16F873A and PIC16F874A have one-half of the total on-chip memory of the PIC16F876A and PIC16F877A
- The 28-pin devices have three I/O ports, while the 40/44-pin devices have five
- The 28-pin devices have fourteen interrupts, while the 40/44-pin devices have fifteen
- The 28-pin devices have five A/D input channels, while the 40/44-pin devices have eight
- The Parallel Slave Port is implemented only on the 40/44-pin devices

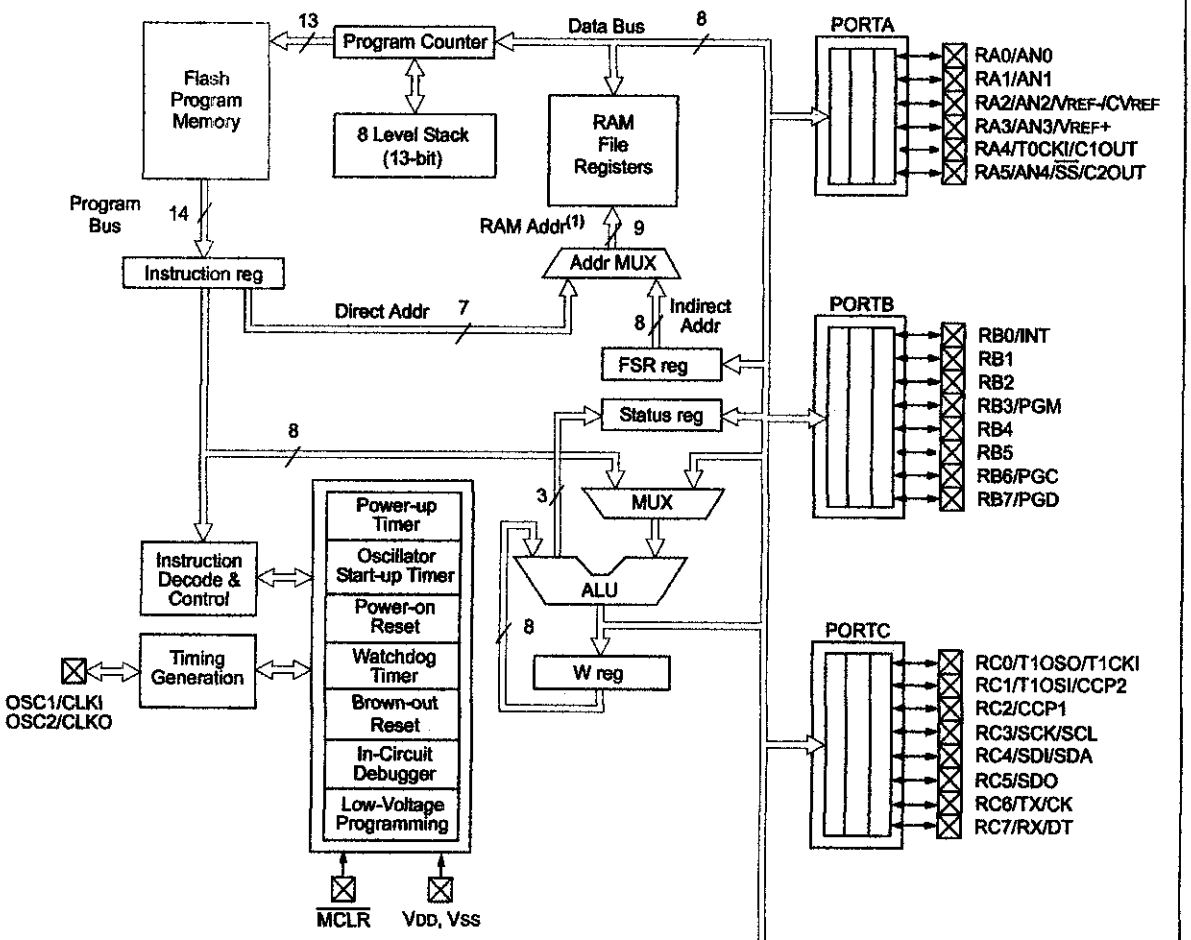
The available features are summarized in Table 1-1. Block diagrams of the PIC16F873A/876A and PIC16F874A/877A devices are provided in Figure 1-1 and Figure 1-2, respectively. The pinouts for these device families are listed in Table 1-2 and Table 1-3.

Additional information may be found in the PICmicro® Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this data sheet and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

TABLE 1-1: PIC16F87XA DEVICE FEATURES

Key Features	PIC16F873A	PIC16F874A	PIC16F876A	PIC16F877A
Operating Frequency	DC – 20 MHz	DC – 20 MHz	DC – 20 MHz	DC – 20 MHz
Resets (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
Flash Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory (bytes)	128	128	256	256
Interrupts	14	15	14	15
I/O Ports	Ports A, B, C	Ports A, B, C, D, E	Ports A, B, C	Ports A, B, C, D, E
Timers	3	3	3	3
Capture/Compare/PWM modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Analog Comparators	2	2	2	2
Instruction Set	35 Instructions	35 Instructions	35 Instructions	35 Instructions
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN

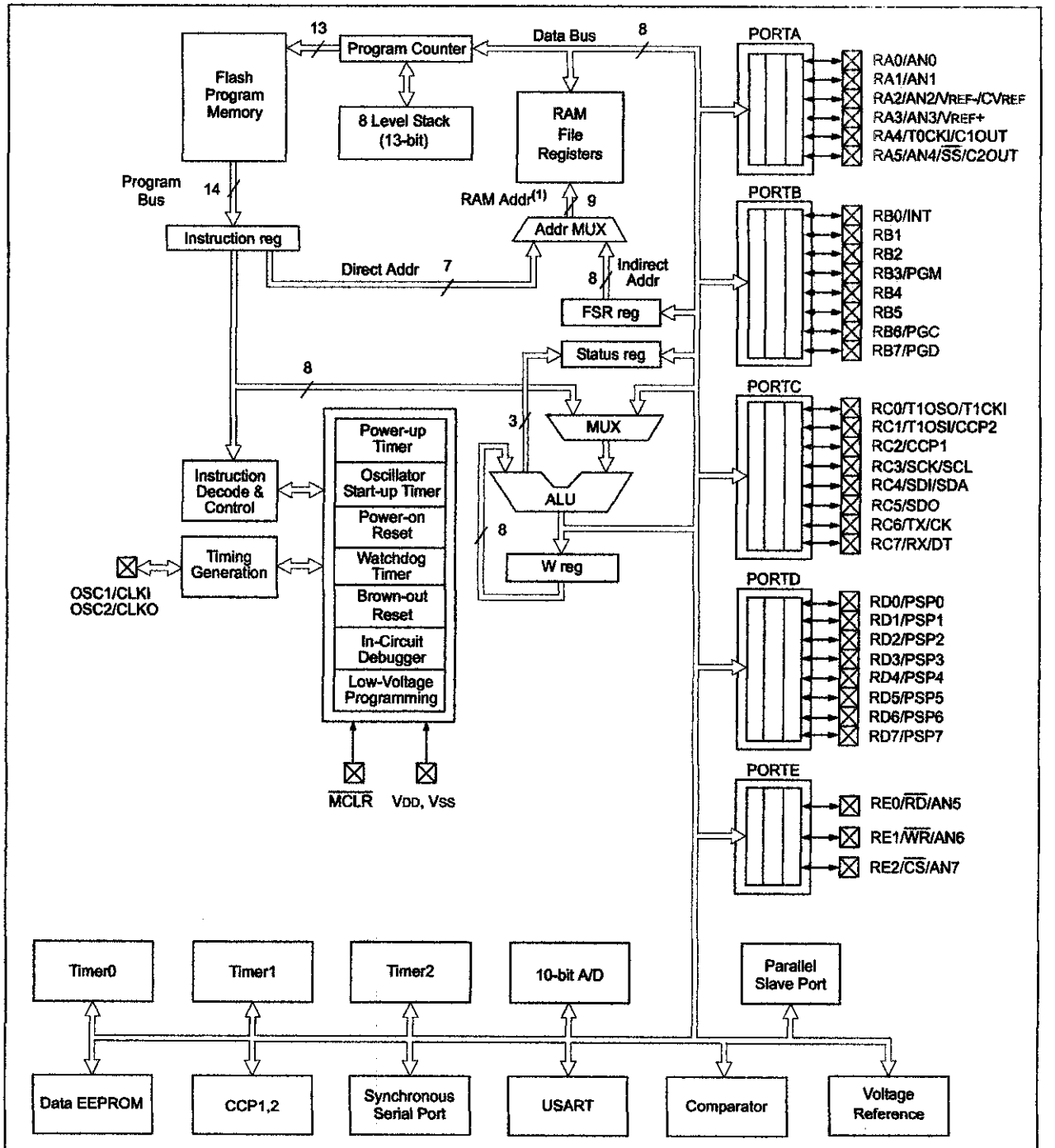
FIGURE 1-1: PIC16F873A/876A BLOCK DIAGRAM



Device	Program Flash	Data Memory	Data EEPROM
PIC16F873A	4K words	192 Bytes	128 Bytes
PIC16F876A	8K words	368 Bytes	256 Bytes

Note 1: Higher order bits are from the Status register.

FIGURE 1-2: PIC16F874A/877A BLOCK DIAGRAM



Device	Program Flash	Data Memory	Data EEPROM
PIC16F874A	4K words	192 Bytes	128 Bytes
PIC16F877A	8K words	368 Bytes	256 Bytes

Note 1: Higher order bits are from the Status register.

TABLE 1-2: PIC16F873A/876A PINOUT DESCRIPTION

Pin Name	PDIP, SOIC, SSOP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI	9	6		ST/CMOS(3)	Oscillator crystal or external clock input.
OSC1			I		Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS.
CLKI			I		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO	10	7		—	Oscillator crystal or clock output.
OSC2			O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			O		In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	26		ST	Master Clear (input) or programming voltage (output).
$\overline{MCLR}$			I		Master Clear (Reset) input. This pin is an active low Reset to the device.
VPP			P		Programming voltage input.
					PORTA is a bidirectional I/O port.
RA0/AN0	2	27		TTL	
RA0			I/O		Digital I/O.
AN0			I		Analog input 0.
RA1/AN1	3	28		TTL	
RA1			I/O		Digital I/O.
AN1			I		Analog input 1.
RA2/AN2/VREF-/ CVREF	4	1		TTL	
			I/O		Digital I/O.
RA2			I		Analog input 2.
AN2			I		A/D reference voltage (Low) input.
VREF-			O		Comparator VREF output.
CVREF					
RA3/AN3/VREF+	5	2		TTL	
RA3			I/O		Digital I/O.
AN3			I		Analog input 3.
VREF+			I		A/D reference voltage (High) input.
RA4/T0CKI/C1OUT	6	3		ST	
RA4			I/O		Digital I/O – Open-drain when configured as output.
T0CKI			I		Timer0 external clock input.
C1OUT			O		Comparator 1 output.
RA5/AN4/$\overline{SS}$/C2OUT	7	4		TTL	
RA5			I/O		Digital I/O.
AN4			I		Analog input 4.
$\overline{SS}$			I		SPI slave select input.
C2OUT			O		Comparator 2 output.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-2: PIC16F873A/876A PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP, SOIC, SSOP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
					PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT	21	18		TTL/ST(1)	
RB0			I/O		Digital I/O.
INT			I		External interrupt.
RB1	22	19	I/O	TTL	Digital I/O.
RB2	23	20	I/O	TTL	Digital I/O.
RB3/PGM	24	21		TTL	
RB3			I/O		Digital I/O.
PGM			I		Low-voltage (single-supply) ICSP programming enable pin.
RB4	25	22	I/O	TTL	Digital I/O.
RB5	26	23	I/O	TTL	Digital I/O.
RB6/PGC	27	24		TTL/ST(2)	
RB6			I/O		Digital I/O.
PGC			I		In-circuit debugger and ICSP programming clock.
RB7/PGD	28	25		TTL/ST(2)	
RB7			I/O		Digital I/O.
PGD			I/O		In-circuit debugger and ICSP programming data.
					PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	11	8		ST	
RC0			I/O		Digital I/O.
T1OSO			O		Timer1 oscillator output.
T1CKI			I		Timer1 external clock input.
RC1/T1OSI/CCP2	12	9		ST	
RC1			I/O		Digital I/O.
T1OSI			I		Timer1 oscillator input.
CCP2			I/O		Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	13	10		ST	
RC2			I/O		Digital I/O.
CCP1			I/O		Capture1 input, Compare1 output, PWM1 output.
RC3/SCK/SCL	14	11		ST	
RC3			I/O		Digital I/O.
SCK			I/O		Synchronous serial clock input/output for SPI mode.
SCL			I/O		Synchronous serial clock input/output for I^2C mode.
RC4/SDI/SDA	15	12		ST	
RC4			I/O		Digital I/O.
SDI			I		SPI data in.
SDA			I/O		I^2C data I/O.
RC5/SDO	16	13		ST	
RC5			I/O		Digital I/O.
SDO			O		SPI data out.
RC6/TX/CK	17	14		ST	
RC6			I/O		Digital I/O.
TX			O		USART asynchronous transmit.
CK			I/O		USART1 synchronous clock.
RC7/RX/DT	18	15		ST	
RC7			I/O		Digital I/O.
RX			I		USART asynchronous receive.
DT			I/O		USART synchronous data.
VSS	8, 19	5, 6	P	—	Ground reference for logic and I/O pins.
VDD	20	17	P	—	Positive supply for logic and I/O pins.

Legend: I = *input* O = *output* I/O = *input/output* P = *power*
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F874A/877A PINOUT DESCRIPTION

Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI	13	14	30	32		ST/CMOS(4)	Oscillator crystal or external clock input.
OSC1					I		Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS.
CLKI					I		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO	14	15	31	33		—	Oscillator crystal or clock output.
OSC2					O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO					O		In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	2	18	18		ST	Master Clear (input) or programming voltage (output).
$\overline{MCLR}$					I		Master Clear (Reset) input. This pin is an active low Reset to the device.
VPP					P		Programming voltage input.
							PORTA is a bidirectional I/O port.
RA0/AN0	2	3	19	19		TTL	
RA0					I/O		Digital I/O.
AN0					I		Analog input 0.
RA1/AN1	3	4	20	20		TTL	
RA1					I/O		Digital I/O.
AN1					I		Analog input 1.
RA2/AN2/VREF-/CVREF	4	5	21	21		TTL	
RA2					I/O		Digital I/O.
AN2					I		Analog input 2.
VREF-					I		A/D reference voltage (Low) input.
CVREF					O		Comparator VREF output.
RA3/AN3/VREF+	5	6	22	22		TTL	
RA3					I/O		Digital I/O.
AN3					I		Analog input 3.
VREF+					I		A/D reference voltage (High) input.
RA4/T0CKI/C1OUT	6	7	23	23		ST	
RA4					I/O		Digital I/O – Open-drain when configured as output.
T0CKI					I		Timer0 external clock input.
C1OUT					O		Comparator 1 output.
RA5/AN4/$\overline{SS}$/C2OUT	7	8	24	24		TTL	
RA5					I/O		Digital I/O.
AN4					I		Analog input 4.
$\overline{SS}$					I		SPI slave select input.
C2OUT					O		Comparator 2 output.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F874A/877A PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
							PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	9		TTL/ST(1)	
RB0					I/O		Digital I/O.
INT					I		External interrupt.
RB1	34	37	9	10	I/O	TTL	Digital I/O.
RB2	35	38	10	11	I/O	TTL	Digital I/O.
RB3/PGM	36	39	11	12		TTL	
RB3					I/O		Digital I/O.
PGM					I		Low-voltage ICSP programming enable pin.
RB4	37	41	14	14	I/O	TTL	Digital I/O.
RB5	38	42	15	15	I/O	TTL	Digital I/O.
RB6/PGC	39	43	16	16		TTL/ST(2)	
RB6					I/O		Digital I/O.
PGC					I		In-circuit debugger and ICSP programming clock.
RB7/PGD	40	44	17	17		TTL/ST(2)	
RB7					I/O		Digital I/O.
PGD					I/O		In-circuit debugger and ICSP programming data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F874A/877A PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
							PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	15	16	32	34		ST	
RC0					I/O		Digital I/O.
T1OSO					O		Timer1 oscillator output.
T1CKI					I		Timer1 external clock input.
RC1/T1OSI/CCP2	16	18	35	35		ST	
RC1					I/O		Digital I/O.
T1OSI					I		Timer1 oscillator input.
CCP2					I/O		Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	17	19	36	36		ST	
RC2					I/O		Digital I/O.
CCP1					I/O		Capture1 input, Compare1 output, PWM1 output.
RC3/SCK/SCL	18	20	37	37		ST	
RC3					I/O		Digital I/O.
SCK					I/O		Synchronous serial clock input/output for SPI mode.
SCL					I/O		Synchronous serial clock input/output for I^2C mode.
RC4/SDI/SDA	23	25	42	42		ST	
RC4					I/O		Digital I/O.
SDI					I		SPI data in.
SDA					I/O		I^2C data I/O.
RC5/SDO	24	26	43	43		ST	
RC5					I/O		Digital I/O.
SDO					O		SPI data out.
RC6/TX/CK	25	27	44	44		ST	
RC6					I/O		Digital I/O.
TX					O		USART asynchronous transmit.
CK					I/O		USART1 synchronous clock.
RC7/RX/DT	26	29	1	1		ST	
RC7					I/O		Digital I/O.
RX					I		USART asynchronous receive.
DT					I/O		USART synchronous data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F874A/877A PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
							PORTD is a bidirectional I/O port or Parallel Slave Port when interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	38		ST/TTL(3)	
RD0					I/O		Digital I/O.
PSP0					I/O		Parallel Slave Port data.
RD1/PSP1	20	22	39	39		ST/TTL(3)	
RD1					I/O		Digital I/O.
PSP1					I/O		Parallel Slave Port data.
RD2/PSP2	21	23	40	40		ST/TTL(3)	
RD2					I/O		Digital I/O.
PSP2					I/O		Parallel Slave Port data.
RD3/PSP3	22	24	41	41		ST/TTL(3)	
RD3					I/O		Digital I/O.
PSP3					I/O		Parallel Slave Port data.
RD4/PSP4	27	30	2	2		ST/TTL(3)	
RD4					I/O		Digital I/O.
PSP4					I/O		Parallel Slave Port data.
RD5/PSP5	28	31	3	3		ST/TTL(3)	
RD5					I/O		Digital I/O.
PSP5					I/O		Parallel Slave Port data.
RD6/PSP6	29	32	4	4		ST/TTL(3)	
RD6					I/O		Digital I/O.
PSP6					I/O		Parallel Slave Port data.
RD7/PSP7	30	33	5	5		ST/TTL(3)	
RD7					I/O		Digital I/O.
PSP7					I/O		Parallel Slave Port data.
							PORTE is a bidirectional I/O port.
RE0/$\overline{RD}$/AN5	8	9	25	25		ST/TTL(3)	
RE0					I/O		Digital I/O.
$\overline{RD}$					I		Read control for Parallel Slave Port.
AN5					I		Analog input 5.
RE1/$\overline{WR}$/AN6	9	10	26	26		ST/TTL(3)	
RE1					I/O		Digital I/O.
$\overline{WR}$					I		Write control for Parallel Slave Port.
AN6					I		Analog input 6.
RE2/$\overline{CS}$/AN7	10	11	27	27		ST/TTL(3)	
RE2					I/O		Digital I/O.
$\overline{CS}$					I		Chip select control for Parallel Slave Port.
AN7					I		Analog input 7.
VSS	12, 31	13, 34	6, 29	6, 30, 31	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	12, 35	7, 28	7, 8, 28, 29	P	—	Positive supply for logic and I/O pins.
NC	—	1, 17, 28, 40	12,13, 33, 34	13	—	—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

11.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has five inputs for the 28-pin devices and eight for the 40/44-pin devices.

The conversion of an analog input signal results in a corresponding 10-bit digital number. The A/D module has high and low-voltage reference input that is software selectable to some combination of VDD, VSS, RA2 or RA3.

The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Register 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 11-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be the voltage reference) or as digital I/O.

Additional information on using the A/D module can be found in the *PICmicro® Mid-Range MCU Family Reference Manual* (DS33023).

REGISTER 11-1: ADCON0 REGISTER (ADDRESS 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	FOSC/2
0	01	FOSC/8
0	10	FOSC/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	FOSC/4
1	01	FOSC/16
1	10	FOSC/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits

000 = Channel 0 (AN0)
001 = Channel 1 (AN1)
010 = Channel 2 (AN2)
011 = Channel 3 (AN3)
100 = Channel 4 (AN4)
101 = Channel 5 (AN5)
110 = Channel 6 (AN6)
111 = Channel 7 (AN7)

Note: The PIC16F873A/876A devices only implement A/D channels 0 through 4; the unimplemented selections are reserved. Do not select any unimplemented channels with these devices.

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

When ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit

1 = A/D converter module is powered up
0 = A/D converter module is shut-off and consumes no operating current

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 11-2: ADCON1 REGISTER (ADDRESS 9Fh)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.
0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in shaded area and in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C/R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2/1
011x	D	D	D	D	D	D	D	D	—	—	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1/2

A = Analog input D = Digital I/O
C/R = # of analog input channels/# of A/D voltage references

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Note: On any device Reset, the port pins that are multiplexed with analog functions (ANx) are forced to be an analog input.

The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D Result register pair, the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 11-1.

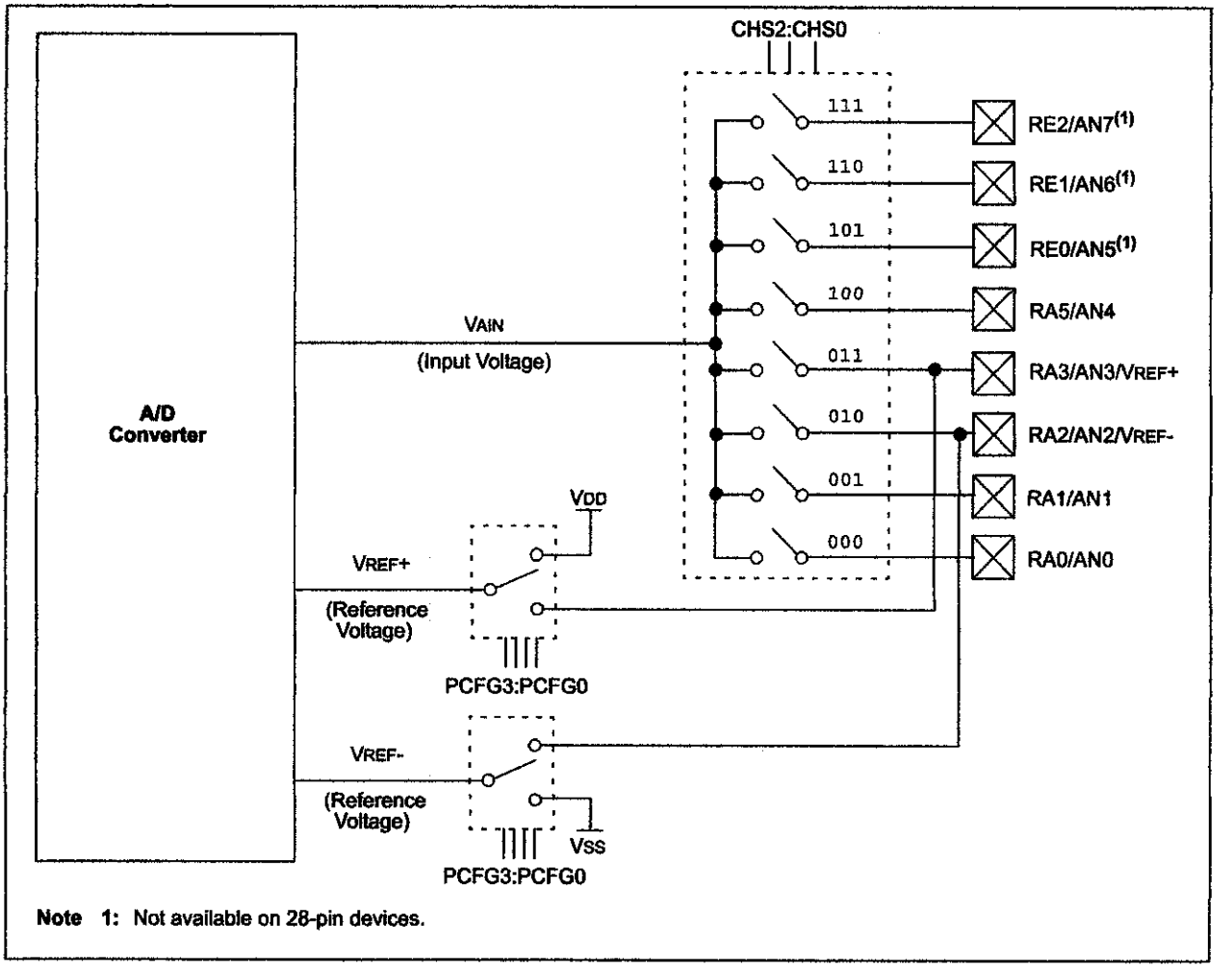
After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To determine sample time, see **Section 11.1 "A/D Acquisition Requirements"**. After this acquisition time has elapsed, the A/D conversion can be started.

To do an A/D Conversion, follow these steps:

1. Configure the A/D module:
   - Configure analog pins/voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set PEIE bit
   - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0)
5. Wait for A/D conversion to complete by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared (interrupts disabled); OR
   - Waiting for the A/D interrupt
6. Read A/D Result register pair (ADRESH:ADRESL), clear bit ADIF if required.
7. For the next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD.

FIGURE 11-1: A/D BLOCK DIAGRAM



Note 1: Not available on 28-pin devices.

11.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 11-2. The source impedance (RS) and the internal sampling switch impedance (RSS) directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD); see Figure 11-2. **The maximum recommended impedance for analog sources is 2.5 kΩ.** As the impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 11-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, TACQ, see the PICmicro® Mid-Range MCU Family Reference Manual (DS33023).

EQUATION 11-1: ACQUISITION TIME

TACQ = Amplifier Settling Time + Hold Capacitor Charging Time + Temperature Coefficient

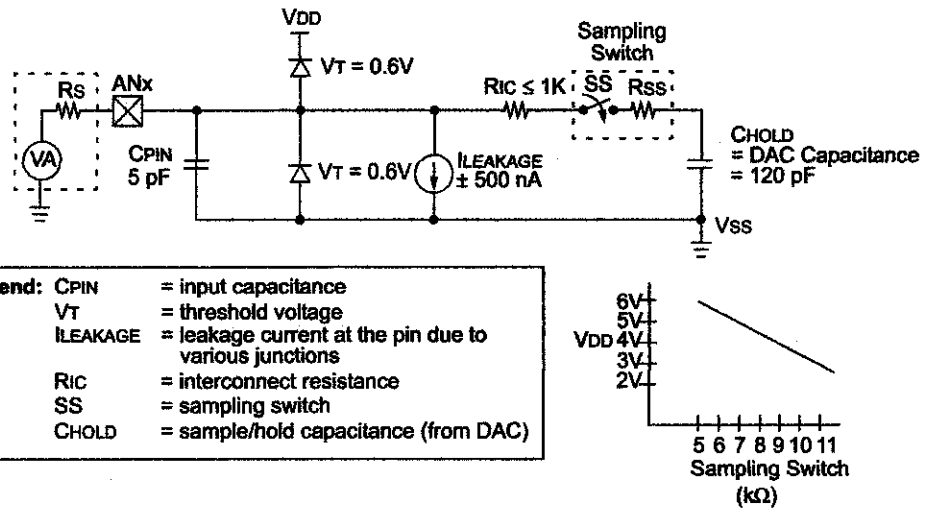
= TAMP + TC + TCOFF
= 2 µs + TC + [(Temperature – 25°C)(0.05 µs/°C)]
TC = CHOLD (RIC + RSS + RS) In(1/2047)
= - 120 pF (1 kΩ + 7 kΩ + 10 kΩ) In(0.0004885)
= 16.47 µs
TACQ = 2 µs + 16.47 µs + [(50°C – 25°C)(0.05 µs/°C)
= 19.72 µs

Note 1: The reference voltage (VREF) has no effect on the equation since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 2.5 kΩ. This is required to meet the pin leakage specification.

FIGURE 11-2: ANALOG INPUT MODEL



11.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires a minimum 12 TAD per 10-bit conversion. The source of the A/D conversion clock is software selected. The seven possible options for TAD are:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal A/D module RC oscillator (2-6 µs)

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 µs.

Table 11-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

11.3 Configuring Analog Port Pins

The ADCON1 and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

Note 1: When reading the port register, any pin configured as an analog input channel will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

2: Analog levels on any pin that is defined as a digital input (including the AN7:AN0 pins) may cause the input buffer to consume current that is out of the device specifications.

TABLE 11-1: TAD vs. MAXIMUM DEVICE OPERATING FREQUENCIES (STANDARD DEVICES (F))

AD Clock Source (TAD)		Maximum Device Frequency
Operation	ADCS2:ADCS1:ADCS0	
2 TOSC	000	1.25 MHz
4 TOSC	100	2.5 MHz
8 TOSC	001	5 MHz
16 TOSC	101	10 MHz
32 TOSC	010	20 MHz
64 TOSC	110	20 MHz
RC(1, 2, 3)	x11	(Note 1)

Note 1: The RC source has a typical TAD time of 4 µs but can vary between 2-6 µs.

2: When the device frequencies are greater than 1 MHz, the RC A/D conversion clock source is only recommended for Sleep operation.

3: For extended voltage devices (LF), please refer to **Section 17.0 "Electrical Characteristics"**.

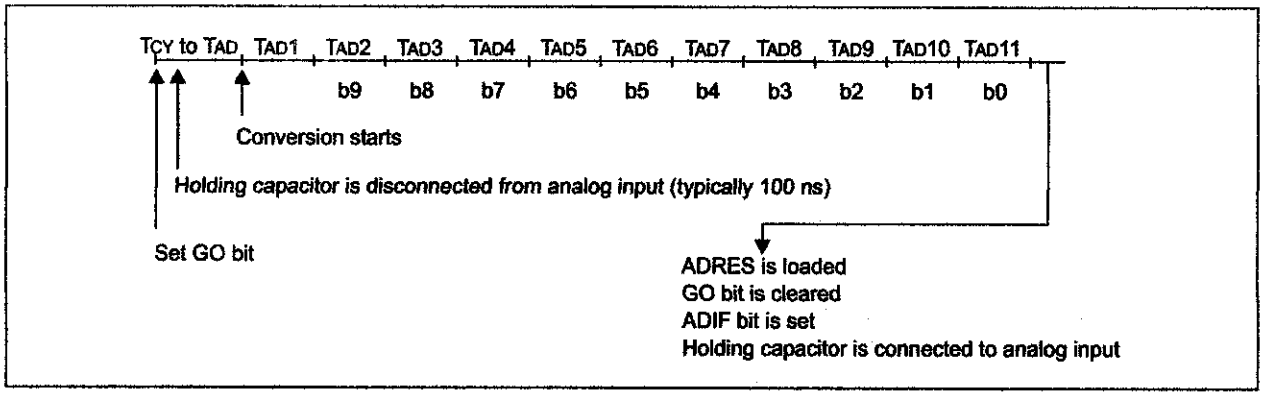
11.4 A/D Conversions

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. That is, the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers). After the A/D conversion is aborted, the next acquisition on the selected channel is automatically started. The GO/$\overline{\text{DONE}}$ bit can then be set to start the conversion.

In Figure 11-3, after the GO bit is set, the first time segment has a minimum of TCY and a maximum of TAD.

Note:	The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D.

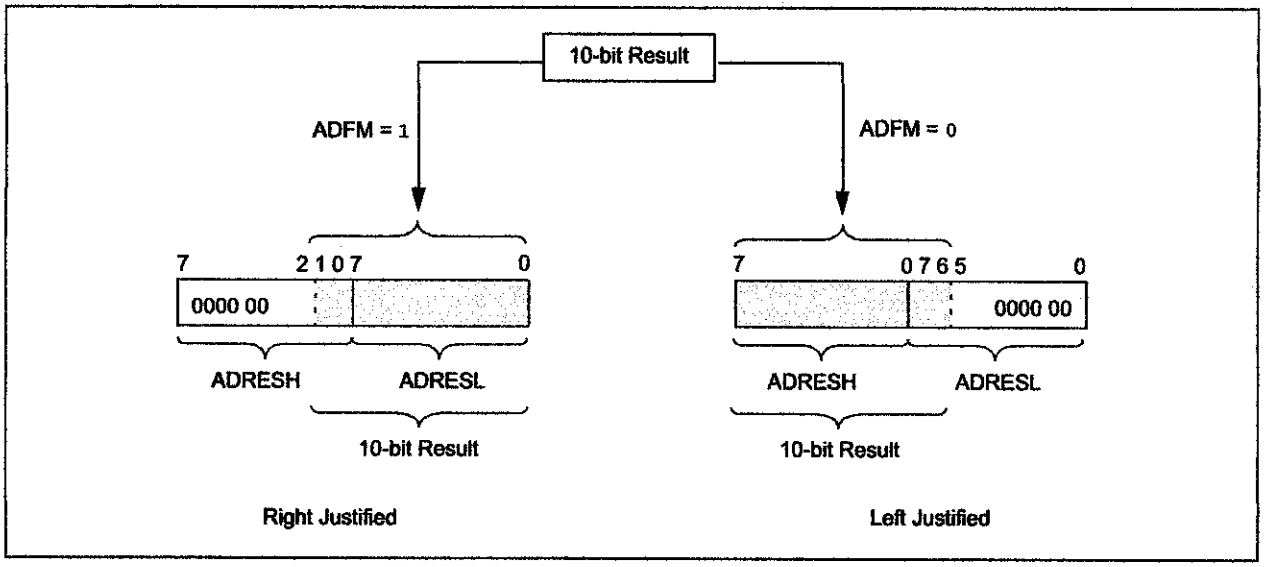
FIGURE 11-3: A/D CONVERSION TAD CYCLES



11.4.1 A/D RESULT REGISTERS

The ADRESH:ADRESL register pair is the location where the 10-bit A/D result is loaded at the completion of the A/D conversion. This register pair is 16 bits wide. The A/D module gives the flexibility to left or right justify the 10-bit result in the 16-bit result register. The A/D Format Select bit (ADFM) controls this justification. Figure 11-4 shows the operation of the A/D result justification. The extra bits are loaded with '0's. When an A/D result will not overwrite these locations (A/D disable), these registers may be used as two general purpose 8-bit registers.

FIGURE 11-4: A/D RESULT JUSTIFICATION



11.5 A/D Operation During Sleep

The A/D module can operate during Sleep mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed which eliminates all digital switching noise from the conversion. When the conversion is completed, the GO/$\overline{\text{DONE}}$ bit will be cleared and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from Sleep. If the A/D interrupt is not enabled, the A/D module will then be turned off, although the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note: For the A/D module to operate in Sleep, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To allow the conversion to occur during Sleep, ensure the SLEEP instruction immediately follows the instruction that sets the GO/$\overline{\text{DONE}}$ bit.

11.6 Effects of a Reset

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion is aborted. All A/D input pins are configured as analog inputs.

The value that is in the ADRESH:ADRESL registers is not modified for a Power-on Reset. The ADRESH:ADRESL registers will contain unknown data after a Power-on Reset.

TABLE 11-2: REGISTERS/BITS ASSOCIATED WITH A/D

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on $\overline{\text{MCLR}}$, WDT
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0	00-- 0000	00-- 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000	--0u 0000
89h(1)	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction bits			0000 -111	0000 -111
09h(1)	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: These registers are not available on 28-pin devices.

9-4323; Rev 11; 2/03

MAXIM

+5V-Powered, Multichannel RS-232 Drivers/Receivers

General Description

he MAX220–MAX249 family of line drivers/receivers is ıtended for all EIA/TIA-232E and V.28/V.24 communica-ons interfaces, particularly applications where ±12V is ot available.

hese parts are especially useful in battery-powered sys-ems, since their low-power shutdown mode reduces ower dissipation to less than 5µW. The MAX225, IAX233, MAX235, and MAX245/MAX246/MAX247 use o external components and are recommended for appli-ations where printed circuit board space is critical.

Applications

Portable Computers

Low-Power Modems

Interface Translation

Battery-Powered RS-232 Systems

Multidrop RS-232 Networks

Features

Superior to Bipolar

- **Operate from Single +5V Power Supply (+5V and +12V—MAX231/MAX239)**
- **Low-Power Receive Mode in Shutdown (MAX223/MAX242)**
- **Meet All EIA/TIA-232E and V.28 Specifications**
- **Multiple Drivers and Receivers**
- **3-State Driver and Receiver Outputs**
- **Open-Line Detection (MAX243)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic DIP
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220C/D	0°C to +70°C	Dice*
MAX220EPE	-40°C to +85°C	16 Plastic DIP
MAX220ESE	-40°C to +85°C	16 Narrow SO
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220EJE	-40°C to +85°C	16 CERDIP
MAX220MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Selection Table

Part Number	Power Supply (V)	No. of RS-232 Drivers/Rx	No. of Ext. Caps	Nominal Cap. Value (µF)	SHDN & Three-State	Rx Active in SHDN	Data Rate (kbps)	Features
MAX220	+5	2/2	4	0.1	No	—	120	Ultra-low-power, industry-standard pinout
MAX222	+5	2/2	4	0.1	Yes	—	200	Low-power shutdown
MAX223 (MAX213)	+5	4/5	4	1.0 (0.1)	Yes	✔	120	MAX241 and receivers active in shutdown
MAX225	+5	5/5	0	—	Yes	✔	120	Available in SO
MAX230 (MAX200)	+5	5/0	4	1.0 (0.1)	Yes	—	120	5 drivers with shutdown
MAX231 (MAX201)	+5 and +7.5 to +13.2	2/2	2	1.0 (0.1)	No	—	120	Standard +5/+12V or battery supplies; same functions as MAX232
MAX232 (MAX202)	+5	2/2	4	1.0 (0.1)	No	—	120 (64)	Industry standard
MAX232A	+5	2/2	4	0.1	No	—	200	Higher slew rate, small caps
MAX233 (MAX203)	+5	2/2	0	—	No	—	120	No external caps
MAX233A	+5	2/2	0	—	No	—	200	No external caps, high slew rate
MAX234 (MAX204)	+5	4/0	4	1.0 (0.1)	No	—	120	Replaces 1488
MAX235 (MAX205)	+5	5/5	0	—	Yes	—	120	No external caps
MAX236 (MAX206)	+5	4/3	4	1.0 (0.1)	Yes	—	120	Shutdown, three state
MAX237 (MAX207)	+5	5/3	4	1.0 (0.1)	No	—	120	Complements IBM PC serial port
MAX238 (MAX208)	+5	4/4	4	1.0 (0.1)	No	—	120	Replaces 1488 and 1489
MAX239 (MAX209)	+5 and +7.5 to +13.2	3/5	2	1.0 (0.1)	No	—	120	Standard +5/+12V or battery supplies; single-package solution for IBM PC serial port
MAX240	+5	5/5	4	1.0	Yes	—	120	DIP or flatpack package
MAX241 (MAX211)	+5	4/5	4	1.0 (0.1)	Yes	—	120	Complete IBM PC serial port
MAX242	+5	2/2	4	0.1	Yes	✔	200	Separate shutdown and enable
MAX243	+5	2/2	4	0.1	No	—	200	Open-line detection simplifies cabling
MAX244	+5	8/10	4	1.0	No	—	120	High slew rate
MAX245	+5	8/10	0	—	Yes	✔	120	High slew rate, int. caps, two shutdown modes
MAX246	+5	8/10	0	—	Yes	✔	120	High slew rate, int. caps, three shutdown modes
MAX247	+5	8/9	0	—	Yes	✔	120	High slew rate, int. caps, nine operating modes
MAX248	+5	8/8	4	1.0	Yes	✔	120	High slew rate, selective half-chip enables
MAX249	+5	6/10	4	1.0	Yes	✔	120	Available in quad flatpack package

+5V-Powered, Multichannel RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS—MAX220/222/232A/233A/242/243

upply Voltage (V_{CC}) ..... -0.3V to +6V
iput Voltages
T_{IN} ..... -0.3V to (V_{CC} - 0.3V)
R_{IN} (Except MAX220) ..... ±30V
R_{IN} (MAX220) ..... ±25V
T_{OUT} (Except MAX220) (Note 1) ..... ±15V
T_{OUT} (MAX220) ..... ±13.2V
utput Voltages
T_{OUT} ..... ±15V
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
river/Receiver Output Short Circuited to GND ..... Continuous
ontinuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin Plastic DIP (derate 8.00mW/°C above +70°C) 440mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) 800mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C) 842mW
Operating Temperature Ranges
MAX2_ _AC_ _, MAX2_ _C_ _ ..... 0°C to +70°C
MAX2_ _AE_ _, MAX2_ _E_ _ ..... -40°C to +85°C
MAX2_ _AM_ _, MAX2_ _M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C

lote 1: Input voltage measured with T_{OUT} in high-impedance state, $\overline{SHDN}$ or V_{CC} = 0V.
lote 2: For the MAX220, V+ and V- can have a maximum magnitude of 7V, but their absolute difference cannot exceed 13V.

'tresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional peration of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to bsolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243

(V_{CC} = +5V ±10%, C1–C4 = 0.1µF, MAX220, C1 = 0.047µF, C2–C4 = 0.33µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±8		V
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High	All devices except MAX220		2	1.4		V
	MAX220: V_{CC} = 5.0V		2.4			
Logic Pull-Up/Input Current	All except MAX220, normal operation			5	40	µA
	$\overline{SHDN}$ = 0V, MAX222/242, shutdown, MAX220			±0.01	±1	
Output Leakage Current	V_{CC} = 5.5V, $\overline{SHDN}$ = 0V, V_{OUT} = ±15V, MAX222/242			±0.01	±10	µA
	V_{CC} = $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	
Data Rate				200	116	kbps
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±22		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±30	V
RS-232 Input Threshold Low	V_{CC} = 5V	All except MAX243 $R2_{IN}$	0.8	1.3		V
		MAX243 $R2_{IN}$ (Note 2)	-3			
RS-232 Input Threshold High	V_{CC} = 5V	All except MAX243 $R2_{IN}$		1.8	2.4	V
		MAX243 $R2_{IN}$ (Note 2)		-0.5	-0.1	
RS-232 Input Hysteresis	All except MAX243, V_{CC} = 5V, no hysteresis in shdn.		0.2	0.5	1	V
	MAX243			1		
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Shrinking V_{OUT} = V_{CC}		10	30		

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243 (continued)

(V_{CC} = +5V ±10%, C1–C4 = 0.1µF, MAX220, C1 = 0.047µF, C2–C4 = 0.33µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

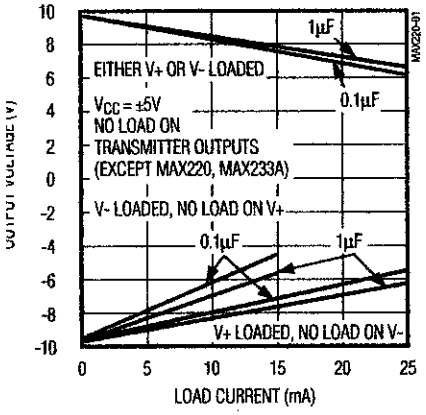
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TTL/CMOS Output Leakage Current	$\overline{SHDN}$ = V_{CC} or $\overline{EN}$ = V_{CC} ($\overline{SHDN}$ = 0V for MAX222), 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA
$\overline{EN}$ Input Threshold Low	MAX242			1.4	0.8	V
$\overline{EN}$ Input Threshold High	MAX242		2.0	1.4		V
Operating Supply Voltage			4.5		5.5	V
V_{CC} Supply Current ($\overline{SHDN}$ = V_{CC}), Figures 5, 6, 11, 19	No load	MAX220		0.5	2	mA
		MAX222/232A/233A/242/243		4	10	
	3kΩ load both inputs	MAX220		12		
		MAX222/232A/233A/242/243		15		
Shutdown Supply Current	MAX222/242	T_A = +25°C		0.1	10	µA
		T_A = 0°C to +70°C		2	50	
		T_A = -40°C to +85°C		2	50	
		T_A = -55°C to +125°C		35	100	
$\overline{SHDN}$ Input Leakage Current	MAX222/242				±1	µA
$\overline{SHDN}$ Threshold Low	MAX222/242			1.4	0.8	V
$\overline{SHDN}$ Threshold High	MAX222/242		2.0	1.4		V
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V	MAX222/232A/233A/242/243	6	12	30	V/µs
		MAX220	1.5	3	30	
Transmitter Propagation Delay TLL to RS-232 (Normal Operation), Figure 1	t_{PHLT}	MAX222/232A/233A/242/243		1.3	3.5	µs
		MAX220		4	10	
	t_{PLHT}	MAX222/232A/233A/242/243		1.5	3.5	
		MAX220		5	10	
Receiver Propagation Delay RS-232 to TLL (Normal Operation), Figure 2	t_{PHLR}	MAX222/232A/233A/242/243		0.5	1	µs
		MAX220		0.6	3	
	t_{PLHR}	MAX222/232A/233A/242/243		0.6	1	
		MAX220		0.8	3	
Receiver Propagation Delay RS-232 to TLL (Shutdown), Figure 2	t_{PHLS}	MAX242		0.5	10	µs
	t_{PLHS}	MAX242		2.5	10	
Receiver-Output Enable Time, Figure 3	t_{ER}	MAX242		125	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}	MAX242		160	500	ns
Transmitter-Output Enable Time ($\overline{SHDN}$ Goes High), Figure 4	t_{ET}	MAX222/242, 0.1µF caps (includes charge-pump start-up)		250		µs
Transmitter-Output Disable Time ($\overline{SHDN}$ Goes Low), Figure 4	t_{DT}	MAX222/242, 0.1µF caps		600		ns
Transmitter + to - Propagation Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}	MAX222/232A/233A/242/243		300		ns
		MAX220		2000		
Receiver + to - Propagation Delay Difference (Normal Operation)	t_{PHLR} - t_{PLHR}	MAX222/232A/233A/242/243		100		ns
		MAX220		225		

Note 3: MAX243 $R2_{OUT}$ is guaranteed to be low when $R2_{IN}$ is ≥ 0V or is floating.

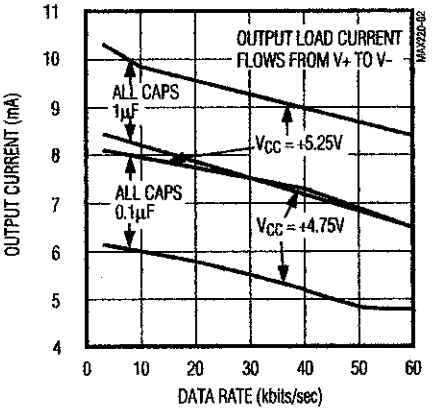
Typical Operating Characteristics

MAX220/MAX222/MAX232A/MAX233A/MAX242/MAX243

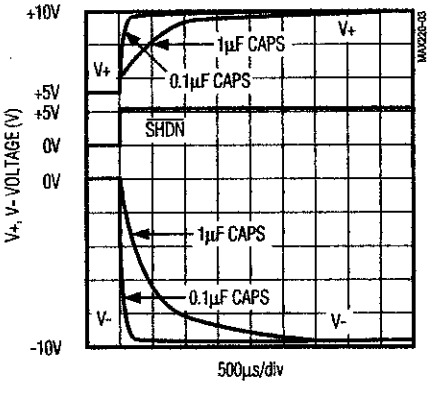
OUTPUT VOLTAGE vs. LOAD CURRENT



AVAILABLE OUTPUT CURRENT vs. DATA RATE



MAX222/MAX242 ON-TIME EXITING SHUTDOWN



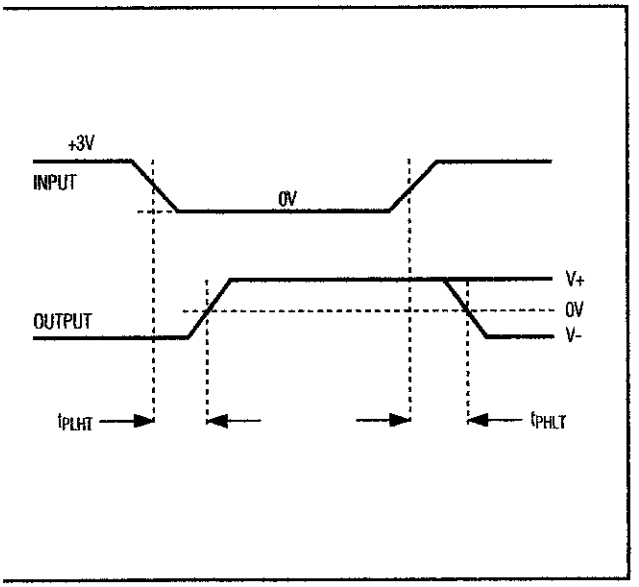


Figure 1. Transmitter Propagation-Delay Timing

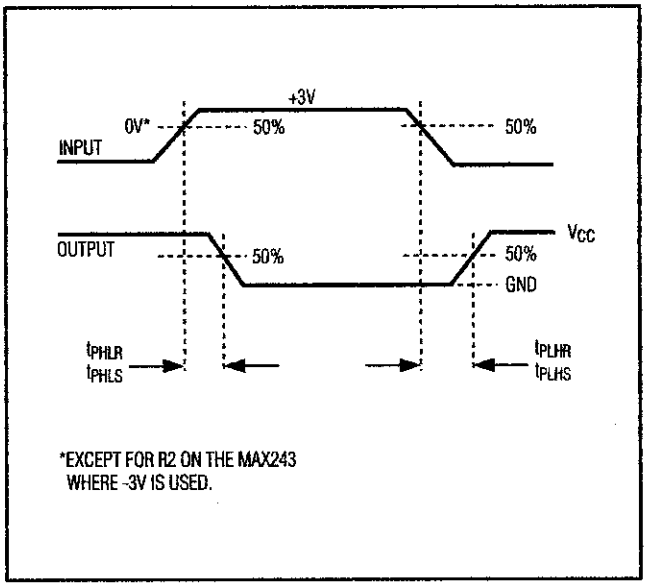


Figure 2. Receiver Propagation-Delay Timing

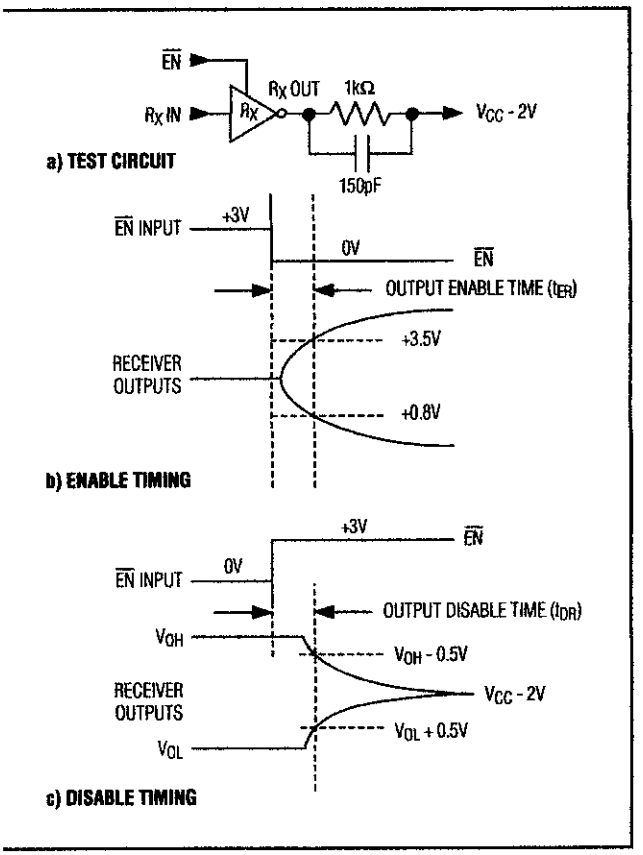


Figure 3. Receiver-Output Enable and Disable Timing

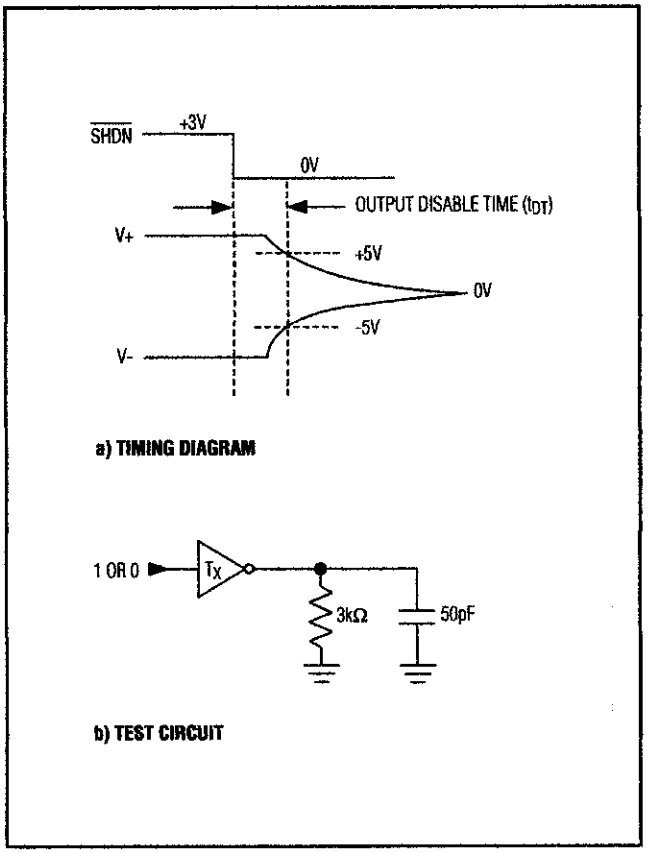


Figure 4. Transmitter-Output Disable Timing

Detailed Description

he MAX220–MAX249 contain four sections: dual harge-pump DC-DC voltage converters, RS-232 dri- ers, RS-232 receivers, and receiver and transmitter nable control inputs.

Dual Charge-Pump Voltage Converter

he MAX220–MAX249 have two internal charge-pumps iat convert +5V to ±10V (unloaded) for RS-232 driver peration. The first converter uses capacitor C1 to dou- le the +5V input to +10V on C3 at the V+ output. The econd converter uses capacitor C2 to invert +10V to 10V on C4 at the V- output.

\ small amount of power may be drawn from the +10V V+) and -10V (V-) outputs to power external circuitry see the *Typical Operating Characteristics* section), xcept on the MAX225 and MAX245–MAX247, where iese pins are not available. V+ and V- are not regulated, o the output voltage drops with increasing load current.)o not load V+ and V- to a point that violates the mini- num ±5V EIA/TIA-232E driver output voltage when ourcing current from V+ and V- to external circuitry.

Vhen using the shutdown feature in the MAX222, /IAX225, MAX230, MAX235, MAX236, MAX240, /IAX241, and MAX245–MAX249, avoid using V+ and V- o power external circuitry. When these parts are shut lown, V- falls to 0V, and V+ falls to +5V. For applica- ions where a +10V external supply is applied to the V+ in (instead of using the internal charge pump to gen- rate +10V), the C1 capacitor must not be installed and he $\overline{SHDN}$ pin must be tied to V_{CC}. This is because V+ s internally connected to V_{CC} in shutdown mode.

RS-232 Drivers

The typical driver output voltage swing is ±8V when oaded with a nominal 5kΩ RS-232 receiver and V_{CC} = -5V. Output swing is guaranteed to meet the EIA/TIA- 232E and V.28 specification, which calls for ±5V mini- num driver output levels under worst-case conditions. These include a minimum 3kΩ load, V_{CC} = +4.5V, and naximum operating temperature. Unloaded driver out- ut voltage ranges from (V+ -1.3V) to (V- +0.5V).

nput thresholds are both TTL and CMOS compatible. The inputs of unused drivers can be left unconnected ince 400kΩ input pull-up resistors to V_{CC} are built in except for the MAX220). The pull-up resistors force the utputs of unused drivers low because all drivers invert. The internal input pull-up resistors typically source 12µA, xcept in shutdown mode where the pull-ups are dis- abled. Driver outputs turn off and enter a high-imped- ance state—where leakage current is typically nicroamperes (maximum 25µA)—when in shutdown mode, in three-state mode, or when device power is removed. Outputs can be driven to ±15V. The power-supply current typically drops to 8µA in shutdown mode. The MAX220 does not have pull-up resistors to force the outputs of the unused drivers low. Connect unused inputs to GND or V_{CC}.

The MAX239 has a receiver three-state control line, and the MAX223, MAX225, MAX235, MAX236, MAX240, and MAX241 have both a receiver three-state control line and a low-power shutdown control. Table 2 shows the effects of the shutdown control and receiver three-state control on the receiver outputs.

The receiver TTL/CMOS outputs are in a high-impedance, three-state mode whenever the three-state enable line is high (for the MAX225/MAX235/MAX236/MAX239–MAX241), and are also high-impedance whenever the shutdown control line is high.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA with the driver output pulled to ground. The driver output leakage remains less than 1µA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V, the transmitter is diode clamped to ground with 1kΩ series impedance. The transmitter is also zener clamped to approximately V_{CC} + 6V, with a series impedance of 1kΩ.

The driver output slew rate is limited to less than 30V/µs as required by the EIA/TIA-232E and V.28 specifications. Typical slew rates are 24V/µs unloaded and 10V/µs loaded with 3Ω and 2500pF.

RS-232 Receivers

EIA/TIA-232E and V.28 specifications define a voltage level greater than 3V as a logic 0, so all receivers invert. Input thresholds are set at 0.8V and 2.4V, so receivers respond to TTL level inputs as well as EIA/TIA-232E and V.28 levels.

The receiver inputs withstand an input overvoltage up to ±25V and provide input terminating resistors with

Table 2. Three-State Control of Receivers

PART	SHDN	$\overline{SHDN}$	EN	$\overline{EN(R)}$	RECEIVERS
MAX223	—	Low High High	X Low High	—	High Impedance Active High Impedance
MAX225	—	—	—	Low High	High Impedance Active
MAX235 MAX236 MAX240	Low Low High	—	—	Low High X	High Impedance Active High Impedance

ıominal 5kΩ values. The receivers implement Type 1 ıterpretation of the fault conditions of V.28 and :IA/TIA-232E.

'he receiver input hysteresis is typically 0.5V with a ıuaranteed minimum of 0.2V. This produces clear out-ıut transitions with slow-moving input signals, even vith moderate amounts of noise and ringing. The eceiver propagation delay is typically 600ns and is ıdependent of input swing direction.

Low-Power Receive Mode

'he low-power receive-mode feature of the MAX223, /AX242, and MAX245–MAX249 puts the IC into shut-lown mode but still allows it to receive information. This s important for applications where systems are periodi-:ally awakened to look for activity. Using low-power eceive mode, the system can still receive a signal that vill activate it on command and prepare it for communi-:ation at faster data rates. This operation conserves ıystem power.

Negative Threshold—MAX243

'he MAX243 is pin compatible with the MAX232A, differ-ıg only in that RS-232 cable fault protection is removed ın one of the two receiver inputs. This means that control ines such as CTS and RTS can either be driven or left loating without interrupting communication. Different :ables are not needed to interface with different pieces of :quipment.

'he input threshold of the receiver without cable fault ırotection is -0.8V rather than +1.4V. Its output goes ıositive only if the input is connected to a control line hat is actively driven negative. If not driven, it defaults o the 0 or "OK to send" state. Normally, the MAX243's ıther receiver (+1.4V threshold) is used for the data line TD or RD), while the negative threshold receiver is con-ıected to the control line (DTR, DTS, CTS, RTS, etc.).

)ther members of the RS-232 family implement the ıptional cable fault protection as specified by EIA/TIA-232E specifications. This means a receiver output goes ıigh whenever its input is driven negative, left floating, ır shorted to ground. The high output tells the serial :ommunications IC to stop sending data. To avoid this, he control lines must either be driven or connected vith jumpers to an appropriate positive voltage level.

Shutdown—MAX222–MAX242

On the MAX222, MAX235, MAX236, MAX240, and MAX241, all receivers are disabled during shutdown. On the MAX223 and MAX242, two receivers continue to operate in a reduced power mode when the chip is in shutdown. Under these conditions, the propagation delay increases to about 2.5µs for a high-to-low input transition. When in shutdown, the receiver acts as a CMOS inverter with no hysteresis. The MAX223 and MAX242 also have a receiver output enable input ($\overline{EN}$ for the MAX242 and EN for the MAX223) that allows receiver output control independent of $\overline{SHDN}$ (SHDN for MAX241). With all other devices, $\overline{SHDN}$ (SHDN for MAX241) also disables the receiver outputs.

The MAX225 provides five transmitters and five receivers, while the MAX245 provides ten receivers and eight transmitters. Both devices have separate receiver and transmitter-enable controls. The charge pumps turn off and the devices shut down when a logic high is applied to the ENT input. In this state, the supply current drops to less than 25µA and the receivers continue to operate in a low-power receive mode. Driver outputs enter a high-impedance state (three-state mode). On the MAX225, all five receivers are controlled by the $\overline{ENR}$ input. On the MAX245, eight of the receiver outputs are controlled by the $\overline{ENR}$ input, while the remaining two receivers (RA5 and RB5) are always active. RA1–RA4 and RB1–RB4 are put in a three-state mode when $\overline{ENR}$ is a logic high.

Receiver and Transmitter Enable Control Inputs

The MAX225 and MAX245–MAX249 feature transmitter and receiver enable controls.

The receivers have three modes of operation: full-speed receive (normal active), three-state (disabled), and low-power receive (enabled receivers continue to function at lower data rates). The receiver enable inputs control the full-speed receive and three-state modes. The transmitters have two modes of operation: full-speed transmit (normal active) and three-state (disabled). The transmitter enable inputs also control the shutdown mode. The device enters shutdown mode when all transmitters are disabled. Enabled receivers function in the low-power receive mode when in shutdown.

ables 1a–1d define the control states. The MAX244 as no control pins and is not included in these tables.

he MAX246 has ten receivers and eight drivers with vo control pins, each controlling one side of the evice. A logic high at the A-side control input ($\overline{ENA}$) auses the four A-side receivers and drivers to go into three-state mode. Similarly, the B-side control input $\overline{ENB}$) causes the four B-side drivers and receivers to o into a three-state mode. As in the MAX245, one A-ide and one B-side receiver (RA5 and RB5) remain ctive at all times. The entire device is put into shut-own mode when both the A and B sides are disabled $\overline{ENA}$ = $\overline{ENB}$ = +5V).

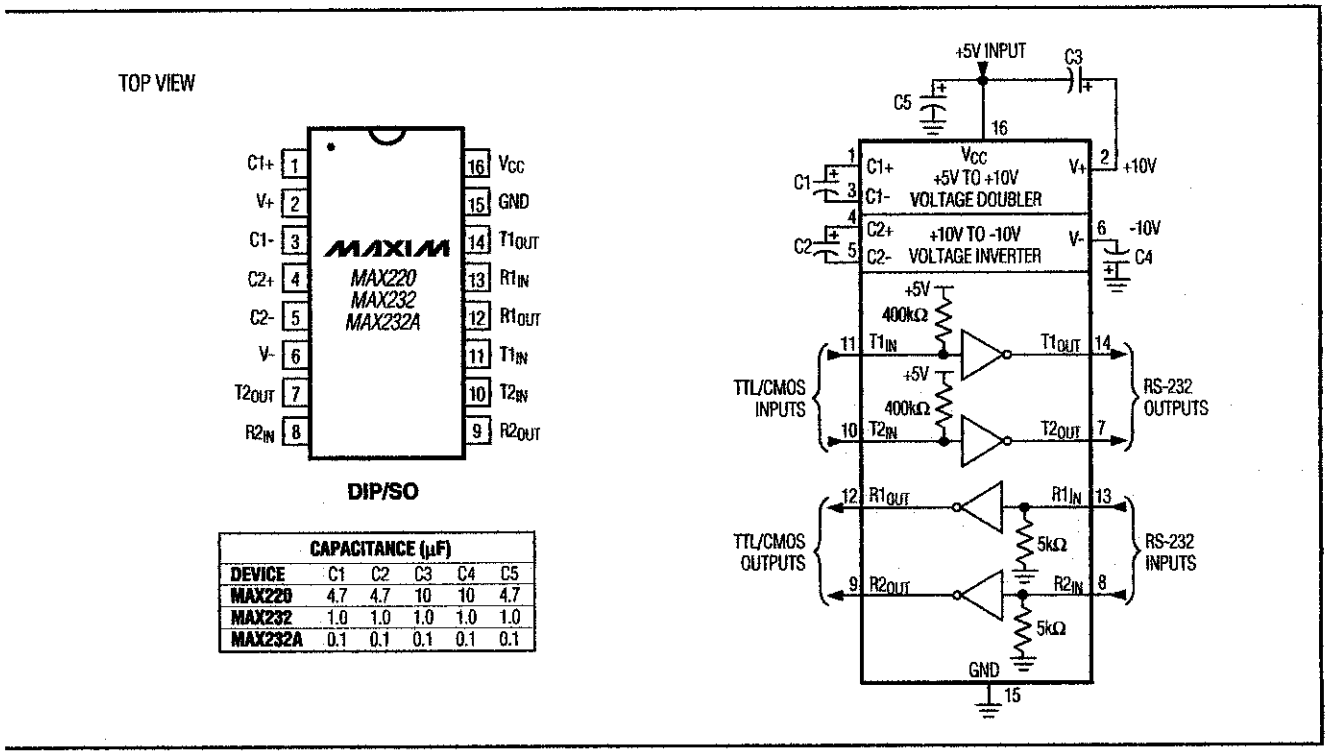
he MAX247 provides nine receivers and eight drivers /ith four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver nable inputs each control four receiver outputs. The $\overline{NTA}$ and $\overline{ENTB}$ transmitter enable inputs each control our drivers. The ninth receiver (RB5) is always active. he device enters shutdown mode with a logic high on oth $\overline{ENTA}$ and $\overline{ENTB}$.

he MAX248 provides eight receivers and eight drivers /ith four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver nable inputs each control four receiver outputs. The $\overline{NTA}$ and $\overline{ENTB}$ transmitter enable inputs control four lrivers each. This part does not have an always-active eceiver. The device enters shutdown mode and trans-nitters go into a three-state mode with a logic high on oth $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX249 provides ten receivers and six drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control five receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control three drivers each. There is no always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$. In shutdown mode, active receivers operate in a low-power receive mode at data rates up to 20kbits/sec.

Applications Information

Figures 5 through 25 show pin configurations and typical operating circuits. In applications that are sensitive to power-supply noise, V_{CC} should be decoupled to ground with a capacitor of the same value as C1 and C2 connected as close as possible to the device.



CAPACITANCE (µF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	10	4.7
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1

Figure 5. MAX220/MAX232/MAX232A Pin Configuration and Typical Operating Circuit

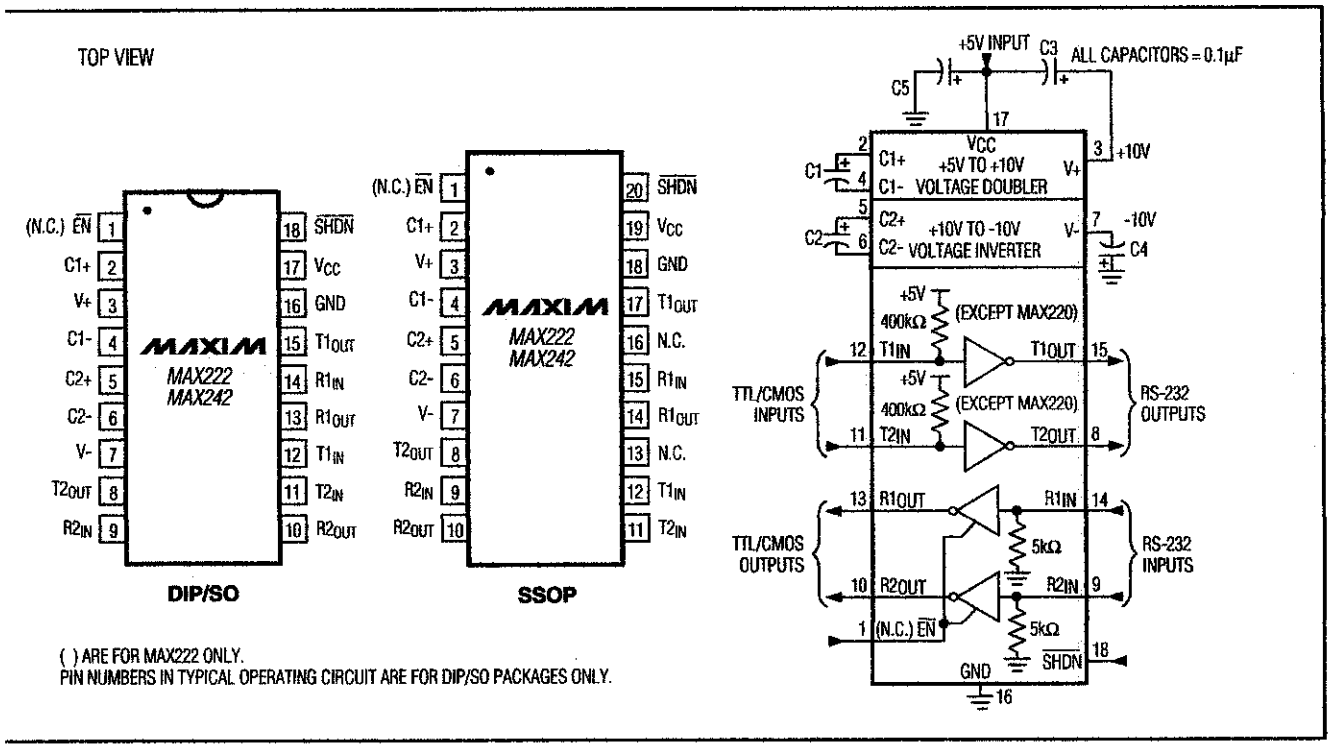


Figure 6. MAX222/MAX242 Pin Configurations and Typical Operating Circuit