STUDY THE EFFECT OF GATE OXIDE THICKNESS AND LDD DOPING PROFILE ON THE PERFORMANCE OF LDMOS BY USING SIMULATOR

By

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FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
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CERTIFICATION OF APPROVAL

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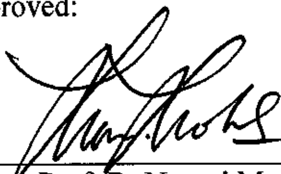
Approved:



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TRONOH, PERAK

June 2007

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

RAJA SAHARUDDIN B RAJA DAUD

ABSTRACT

LDMOS is a silicon device and has been proven to be a popular device in high power RF application. It has excellent efficiency, linearity and peak power capability. The LDMOS roadmap is always to improve intrinsic die performance in key areas such as efficiency, gain and continuing focus on cost – effective device packaging. The objective of this work is to study the effect of gate oxide thickness and LDD doping profile on performance of LDMOS for high power RF applications by using Silvaco TCAD simulator as a part of work to improve its performance. The work is done by varying the gate oxide thickness, T_{ox} from 200 Å up to 700 Å and varying LDD doping profile, N_D from $2x10^{10}cm^{-3}$ to $2x10^{13}cm^{-3}$. The performance of LDMOS is analyzed by investigating the effect on the following parameters: V_T, g_m, f_t, $Ciss$, BV. The results obtained shows that as gate oxide thickness, T_{ox} is increased; V_T and f_t are increased while magnitude of g_m, C_{iss} and BV are reduced. Besides, as LDD concentration, N_D is increased, V_T, magnitude of g_m, and f_t are increased while magnitude of C_{iss}, and BV are reduced. The fundamental of semiconductor device fabrication is studied and understood while the knowledge of using both process and device simulator (Athena & Atlas) has been acquired.

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LIST OF ABBREVIATIONS

LDMOS	Laterally Diffused Metal Oxide semiconductor
RF	Radio Frequency
GaAs	Gallium Arsenic
LDD	Lightly Doped Drain
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
DMOS	Double Diffused Metal Oxide Semiconductor
HEXFET	Hexagonal Field Effect Transistor
VMOS	V-Groove Metal Oxide Semiconductor
UMOS	U-Groove metal Oxide Semiconductor
SiO_2	Silicon Dioxide
UV	Ultra Violet
T_{ox}	Oxide Thickness (Å)
L_c	Channel Length (μ)
V_{br}	Breakdown Voltage (v)
V_t	Threshold Voltage (v)
g_m	Transconductance (Ω^{-1})
I_{Dsat}	Saturation Current (A)
C_{iss},	Input Capacitance (gate-gate) (F)
C_{oss},	Output Capacitance (drain-drain) (F)
C_{rss},	Miller Feedback Capacitance (gate drain) (F)
C_{GS}	Gate – Source capacitance (F)
f_t	Cut Off Frequency (Ghz)
W	Width of the channel (μm)
N_D	Donor Concentration (cm^{-3})

CHAPTER 1

INTRODUCTION

1. 1. Background of Study

The recent wireless communication service has created a huge demand for cost-effective, high gain, ultra-linear high power RF transistor for use in base station power amplifiers. Traditionally, RF power transistors have been built using Si bipolar technology, although Gallium Arsenic (GaAs) transistors are also available. Nowadays laterally diffused metal-oxide semiconductor (LDMOS) transistors have been proven to be very popular for these applications. This is because, LDMOS has superior RF performance compared to bipolar transistors and highly cost-effective compared to the GaAs [1].

1.2. Problem Statement

Since the demand of the RF-LDMOS increased and it is a dominant device technology used in high power wireless infrastructure applications, its performance in term of gain, breakdown voltage, cut off frequency and so on need to be improved. A study of LDMOS device will be conducted in order to investigate and finding the method to improve its performance. Basically an LDMOS is designed base on the silicon technology in order to meet the good power gain, output power, efficiency and linearity of the power amplifier which are the critical parameters that affect the overall performance and cost effectiveness of the system [2]. Base on the available LDMOS structure with 3.5 µm technology refers to the channel length is used as a standard structure for this study. The effect of the gate oxide thickness, T_{ox} and LDD doping profile, N_D on the LDMOS performance are investigated. Gate oxide thickness T_{ox} is varied from 200 Å to 700 Å as well as the LDD doping profile is varied from $2x10^{10}cm^{-3}$ to $2x10^{13}cm^{-3}$.

1.3. Objective and Scope of Study

The objective of this project is to study the effect of gate oxide thickness and LDD doping profile on the performance of LDMOS as a part of work to improve its performance. The knowledge of device fabrication process needs to be acquired and understood by investigating the effect of process parameter such as gate oxide thickness, T_{ox} and LDD doping profile, N_D as well as to find the ways of how to improve its performance. Through this project, the knowledge of device technology, principle of semiconductor device, structure and fabrication process would be acquired. The knowledge of using both process and device simulator such as Silvaco TCAD (Athena & Atlas) would be acquired and understood at the end of the work.

1.3.1. Project Requirement

i. To conduct a study on LDMOS structure for high power RF applications.

ii. Identifying the process involve in creating the LDMOS structure and verifying the effect of the device characteristics when its parameters are changed by using ATHENA and ATLAS simulations.

iii. To investigate how the parameter changes affects the device electrical characteristics and understand the physical theory and concept.

iv. Find out the ways of how to improve the device performance so that a better device can be created.

CHAPTER 2

LITERATURE REVIEW AND THEORY

2.1. Fundamental Review

Power semiconductor device is divided into two categories, which is 2-Terminal device and 3-Terminal devices. The power MOSFET is a 3-Terminal device that consist the gate, source and drain terminal. In the power MOSFET device, there are consist of several types of device which are grown by different method and technique for the particular application and different characteristics. Examples of power MOSFET device are DMOS, LDMOS, HEXFET, VMOS and UMOS. The Figure 1 shows the family of the power semiconductor devices.

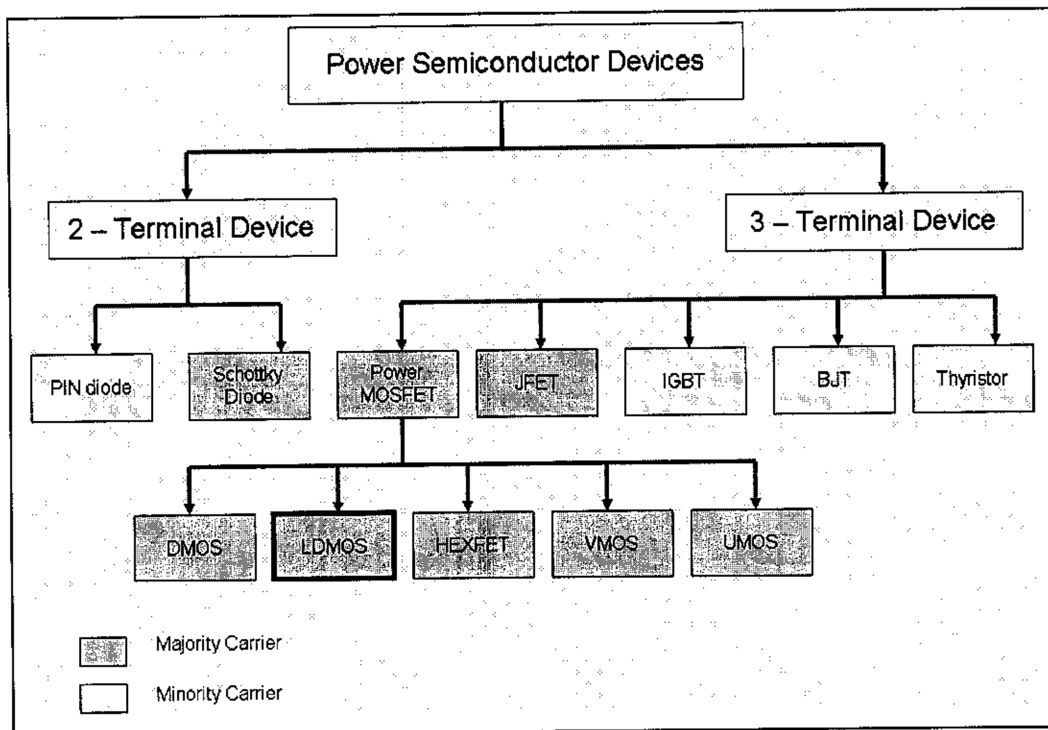
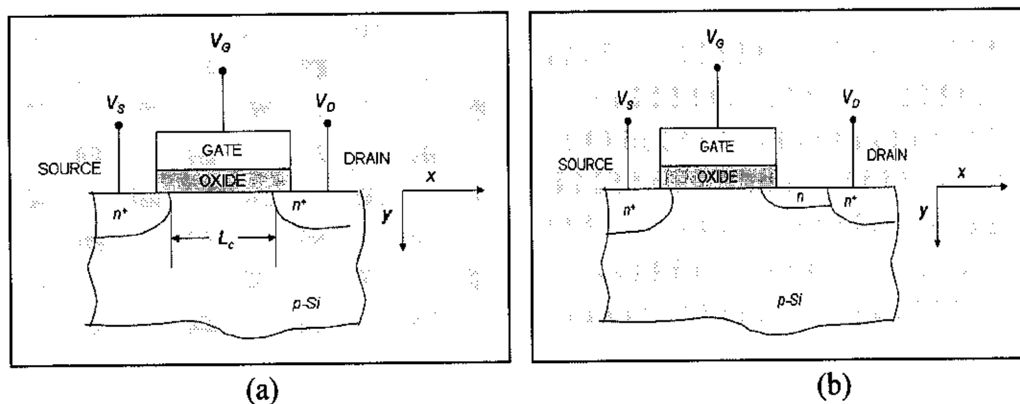


Figure 1: Power device family

LDMOS is an application of power MOSFET device. LDMOS has an asymmetric source and drain. The drain side has a region of lightly doped junction known as

LDD. LDD is fully depleted under large drain bias in order to support a large drain voltage that is necessary for a high-voltage power device. The Figure 2 below shows the cross section of the basic structure of the MOSFET device and LDMOS structure respectively.



(a) (b)

Figure 2: Cross section of the MOSFET and LDMOS
(a) MOSFET n-channel enhancement mode and (b) LDMOSFET

For *n*-channel device, electrons conduct the current from source to drain. The source and drain are formed by n^+ -region on order of $10x10^{20}$ cm^{-3} for good contacts to the channel [10]. The source and drain are formed by ion implantation after the gate structure is defined, source and drain will be self aligned to the gate. The critical part is the formation of a continuous channel and that is determined by gate-to-source and gate-to-drain overlap. If the device in symmetrical, that means the source and drain can be interchanged. In figure 2 (a), L_c is refers to the length of the channel. The length of the channel needs to be optimized so that the current leakage between the source and drain can be minimized. The channel length also will determine the threshold gate voltage, which is to turn on the channel. The threshold voltage can be adjusted according to the channel length.

Commonly the gate material is polysilicon however a metals and silicides also can be used [10]. The metals and silicides are compatible with high-temperature processing.

2.1. Basic LDMOS Structure on Existing Device

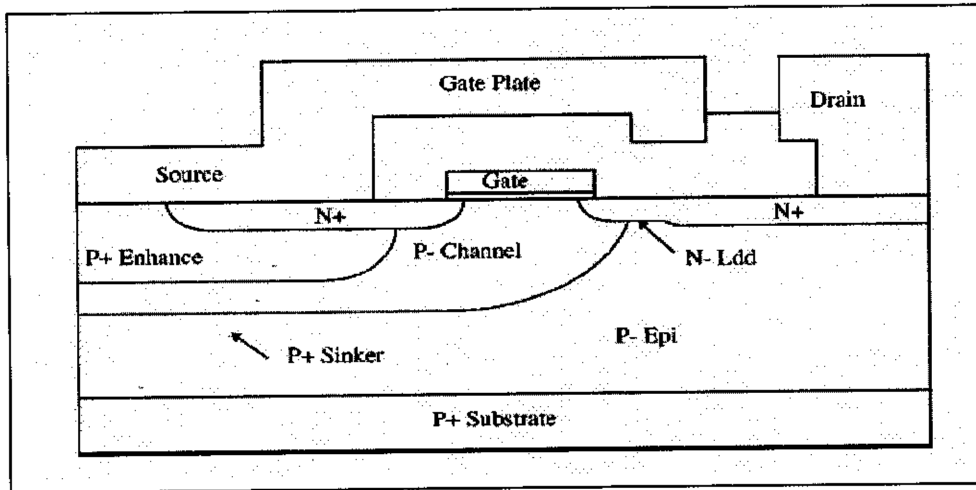


Figure 3: Cross section of LDMOS device

Figure 3 above shows the cross sectional of LDMOS structure that is taken from [3]. The device basically has a high doped p-type sinker diffusion which is used to ground the source to the substrate. This structure can eliminate the need for an external connection from source to the ground and hence the minimum common lead inductance and maximum RF gain. The channel of the device is formed by p-type body region under the gate. Normally the LDMOS device is fabricated to operate for 3 V up to 48 V on the drain. The breakdown voltage of LDMOS devices is accomplished by Lightly Doped Drain (LDD) or drift region to provide higher breakdown voltage. By having LDD region in LDMOS structure, most of the applied voltage appears across the gate oxide and leads to breakdown by impact generation in the substrate region. This corresponds in a specific breakdown voltage for a given oxide thickness. The drain is receded away from the gate result from formation of LDD region between gate and drain edges. In another manner, the LDD also is designed to support a uniform electric field during breakdown [1] and greatly influences the breakdown voltage, on-resistance, saturation current and feedback capacitance of LDMOS.

2.2. LDMOS Characteristics

Common DC characteristics of the LDMOS are [5]:

- Breakdown Voltage, V_{br}
- Threshold Voltage, V_t
- Transconductance, g_m
- Drain saturation current, I_{Dsat}
- Input Capacitance, C_{iss}, (gate-gate)
- Output Capacitance, C_{oss}, (drain-drain)
- Miller feedback capacitance, C_{rss}, (gate-drain)
- Cut off frequency, f_t

2.2.1. Threshold Voltage

A critical part of the MOSFET device is the threshold voltage, V_T where smaller V_T will reduce switching time and switching losses. The threshold voltage is given by the relationship below taken from [10].

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_s qN(2\psi_B)}}{C_{ox}} \quad \text{Where} \tag{1}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{x_{ox}} \tag{2}$$

C_{ox} = Channel Capacitance
V_{FB} = Flat - band voltage
$2\psi_B$ = Surface bending required to ON the channel
$\frac{\sqrt{2\varepsilon_s qN(2\psi_B)}}{C_{ox}}$ = Voltage across oxide layer

Beyond the flat-band condition, the threshold voltage is given by the sum of voltages across the oxide and the semiconductor. To turn on the channel, the surface bending Ψ_s required is $2\Psi_B$. The last term of the equation is voltage across the oxide layer, V_{ox} that is given by the charge in the depletion layer, Q divided by the oxide capacitance, C_{ox}. In the negative substrate bias presence, V_T is increased. It will change the surface potential from $2\Psi_B$ to $(2\Psi_B + |V_{sub}|)$. This condition is dependence on the V_T on the substrate bias or called as body effect. When the drain is biased, the channel potential, $V_c(x)$ will change from drain to source. $V_c(x)$ is the semiconductor potential, Ψ at the surface. The gate voltage above the threshold, the inversion-layer charge density is given by:

$$Q_i(x) = C_{ox}[V_G - V_T - V_c(x)] \tag{3}$$

Where

$Q_i(x)$ = inversion-layer charge density

2.2.2. Drift Current

The electric current induced by an electric potential difference or equivalently electric field is called drift current. The drift equation of the MOSFET is given by [10]:

$$I = W\mu Q_i \xi_x \quad (4)$$

$$I = WC_{ox}\left[V_G - V_T - V_C(x)\right]\frac{dV_C(x)}{dx} \quad (5)$$

where W = Cahnnel width μ = surface mobility Q_i = Charge Density
$V_C(x)$ = Capacitance voltage

$\xi_x = 1 - 2\times10^4\ V/cm$ and $v_{sat} = 1\times10^7\ cm/s$

Integrating from $x = 0$ to L_c

$$I = \frac{\mu C_{ox} W}{L_C}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \quad (6)$$

where

μ = surface mobility	V_G = Gate Voltage
C_{ox} = Channel Capacitance	V_T = Threshold Voltage
W = Channel width	V_D = Drain Voltage
L_C = Channel length	

Drain voltage saturation is:

$$V_{D,sat} = V_G - V_T \quad (7)$$

$$I_{sat} = \frac{W\mu C_{ox}}{2L_c(V_G - V_T)} \quad (8)$$

where W = width of the channel L_c = Channel length C_{ox} = Oxide capacitance

2.2.3. Transconductance

Transconductance is the rate of output current from a device with respect to its input voltage. Transconductance in the saturation region is given as:

$$g_{m,sat} = \frac{dI_{sat}}{dV_G} = \frac{W\mu C_{ox}(V_G - V_T)}{L_C} \quad \text{And} \quad g_m = \frac{W\mu_n C_{ox}}{L}V_D \quad (9)$$

Noted that transconductance will increases with V_D

2.2.4. Cut off Frequency

The cutoff frequency f_T of a MOSFET device will give an indication of the upper limit on the circuit speed. The frequency at the current gain becomes unity is given by [7]:

$$f_T = \frac{g_{m,sat}}{2\pi\left(WL_C C_{ox} + C_{par}\right)} \tag{10}$$

where

$g_{m,sat}$ = Transconductance in saturation $\quad$ $WL_C C_{ox} + C_{par}$ = input capacitance C_{iss}

W = Channel width

L_C = Channel length

C_{ox} = Channel capacitance

C_{par} = Input paracitic capacitance

$$g_{m,sat} = WC_{ox}v_{sat} \tag{11}$$

where

$v_{sat} = 1 \times 10^7 \ cm/s$ for silicon = velocity saturation of carriers

2.2.5. Power gain

The gain of the LDMOS is factor between input and output power and it is given by [3]:

$$G = 10\log\left(\frac{P_{load}}{P_{avs}}\right) \tag{12}$$

where,

P_{load} = Output power delivered to the load

P_{avs} = Power available from the source

2.2.6. Static Capacitance Characteristics

There are three terminal capacitances associated commonly C_{iss}, C_{oss}, and C_{rss}. The capacitances are measured when the transistor channel is not active (no supplied bias current) [1].

Feedback Capacitance C_{rss}

It is formed between gate electrode and drain, primarily due to the overlap of gate oxide over drift region in the device. Extensive improvement in device technology there is significantly minimizing this capacitance in an LDMOS transistor. Typical values of modern day LDMOS are in the range of 12 fF/mm of gate periphery [1].

Output Capacitance, C_{oss}

This capacitance is due to the junction capacitance between the p-body and n-epitaxial regions in the device. It has maximum value under zero-bias conditions, and reducing in value with increasing drain-to-source voltage.

$$C_{oss} = C_{GD} + C_{DS} \quad (13)$$

Input Capacitance, C_{iss}

This capacitance is formed between source metal interconnects and gate material. This capacitance is influenced by gate oxide thickness. It is desirable to reduce C_{iss} for high frequency application. Gate oxide thickness cannot be increased too much as it might compromise the gain and current capability of transistor.

$$C_{iss} \sim C_{rss} + C_{ox} \quad (14)$$

Other contributors to C_{iss} are gate-to-source overlap capacitance, C_{GS} and gate-to-channel capacitance.

2.3. LDMOS Transistor Features for RF Power Application

Base from [1], there are summarizes features of an LDMOS transistor that make it technology of choice for present-day as a high power linear amplifiers.

Table 1: LDMOS Features

Attribute	Effective Parameter	Benefit
Higher gain	High g_m and low C_{rss}	Lower system cost due to fewer stages, Increased gain can be traded for enhance stability
Higher efficiency	Low $R_{DS(on)}$ and Low C_{oss}	Lower junction temperature for same output power, hence greater system performance and higher MTBF
Greater stability	Low C_{rss} and very low source inductor	Easier Design
Simplicity of use	High input resistance, single supply, and backside source contact	Very little Gate current, hence simple Gate bias circuits. Dual supply sources not needed
Improved linearity	$I_{D(sat)}$ and G_m flatness	Less output distortion, reduce overall system power for the same degree of linearity

CHAPTER 3

METHODOLOGY AND PROJECT WORK

3.1. Procedure

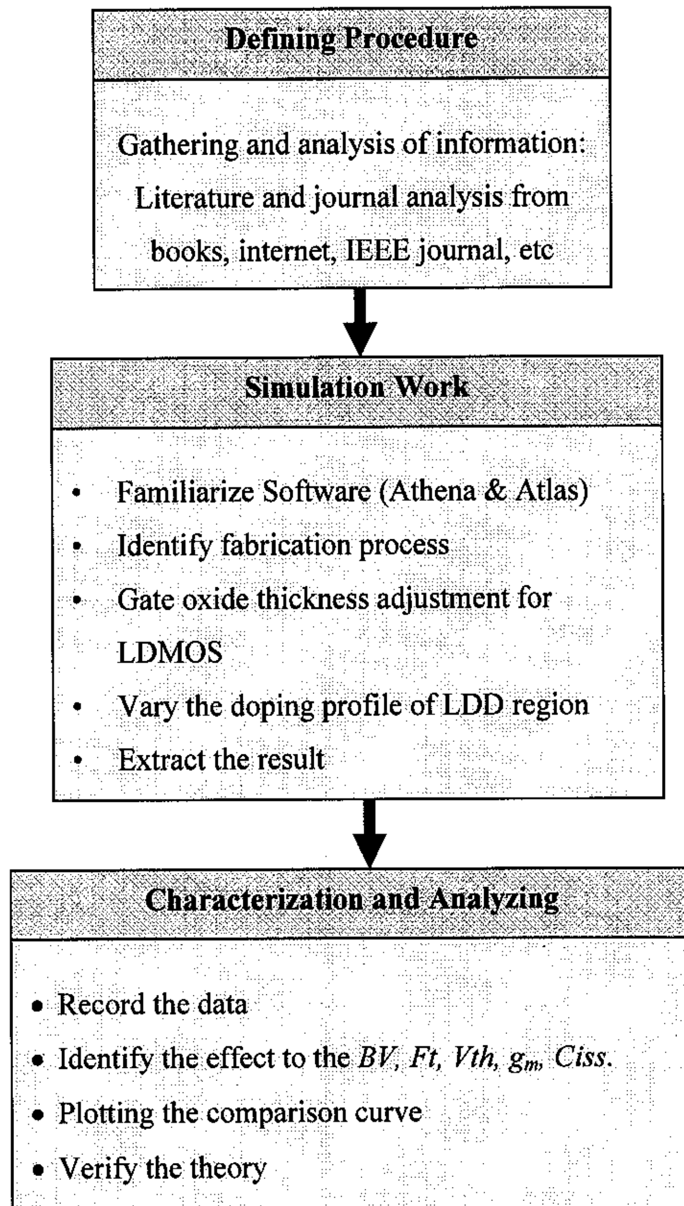


Figure 4: Project Flow Diagram

The **Figure 4** shows the project flow diagram which represents the complete process flow of the work.

3.1.1. Defining Procedure

Conduct a literature review and gathering the information of semiconductor device technology. Find out more information on the internet, books and journals available. The basic principles of fabricating a semiconductor device are understood by reading the book and review the existing research that were conducted by other researcher such as from IEEE transactions. All the information obtained are gathered and utilized for this work.

3.1.2. Simulation Work

SILVACO TCAD workstation is used which consist of ATHENA and ATLAS simulator. ATHENA and ATLAS simulator are used for different purpose where the ATHENA is used in creating the device structure which the materials, width and concentration are defined. On the other hand, ATLAS simulator is used in testing the device structure created in ATHENA. Device electrical characteristics can be analyzed in ATLAS simulation both in term of data measurement and graphical approach.

The exercise and practice have been done in the SILVACO TCAD workstation by getting started with the software through the creating a basic NMOS device structure using ATHENA. The available structure in the workstation also reviewed in order to get an idea on how the semiconductor device structure looks like. After the structure is created in ATHENA, its electrical performance is tested in ATLAS simulation and the characteristics curve is displayed.

Basic operations required for creating a typical MOSFET input file obtained from [9]:

i. Developing a good simulation grid
ii. Performing conformal deposition
iii. Performing geometric etches
iv. Performing oxidation, diffusion, annealing and ion implantation
v. Structure manipulation
vi. Saving and loading structure information.

3.1.3. Review on the Existing Device Structure

The information of the LDMOS structure are discovered in order to identify the current issues on the existing devices and to get the current data of existing device so that it can be used as a reference to this project. Journals and articles are found by surfing the internet, especially IEEE journal. The articles are read and all the findings are recorded and the data found will be used for comparison with the data from the modified structure that will be done on the next step.

In the SILVACO TCAD workstation, the available example of the LDMOS structure is reviewed and studied. Its electrical characteristics are identified through the ATLAS simulation.

3.1.4. Characterization and Analyzing

All the results obtained are recorded. The gate oxide thickness, T_{ox} and LDD doping profile is varied and the effect on the device parameter such as BV, f_t, g_m, C_{iss}, and V_T are analyzed by plotting the comparison curve. The LDMOS structure is analyzed in term of its field, concentration and dimensions.

3.2. Fabrication process

According to [3, 4], the every component of the LDMOS structure are created with the certain process and it has a respective functions that contribute to the device performance. Basically the materials used in creating the LDMOS structure are:

i. Silicon
ii. Silicon dioxide, SiO_2
iii. Polysilicon
iv. Aluminum
v. Phosphorous & Arsenic

The silicon is defined as an initial structure of the device. From the silicon structure, the silicon dioxide, SiO_2 layer is grown through the oxidation process. This process is used to form the gate oxide layer. The polysilicon is defined as a multilayer deposit structure and the aluminum is used in the metallization process. From [9], the basic semiconductor device fabrications are oxidation process, photolithography and etching, Diffusion and ion implantation, and metallization.

3.2.1. Oxidation

The oxidation process of semiconductor device is referred to the development of high-quality silicon dioxide (SiO_2). SiO_2 functions as an insulator on the device structure or barrier to diffusion and implantation process during device fabrication.

3.2.2. Photolithography and Etching

This step defines the geometry of the *p-n* junction. After the oxidations, the wafer is coated with ultraviolet (UV) light-sensitive called a *photoresist*. The area exposed to the light become polymerized and it will remains during the etching process.

3.2.3. Diffusion and Ion Implantation

The surface of semiconductor which not protected by oxide and exposed to a source with a high concentration of opposite-type impurity, the impurity will moves into the semiconductor crystal by solid-state diffusion. In ion implantations, the intended impurity is introduced into the semiconductor by accelerating the impurity ions to a high energy level and then implanting the ions into the semiconductor materials.

3.2.4. Metallization

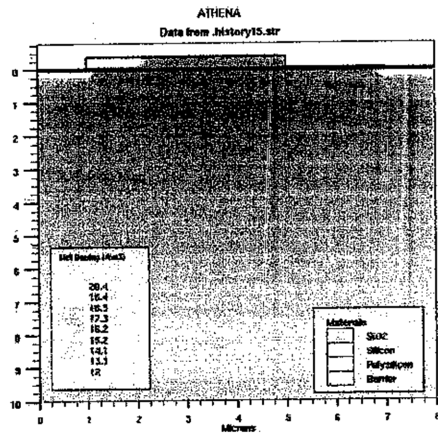
It is used to form an ohmic contacts and interconnections by deposition of metals on the substrate.

3.3. LDMOS Fabrication

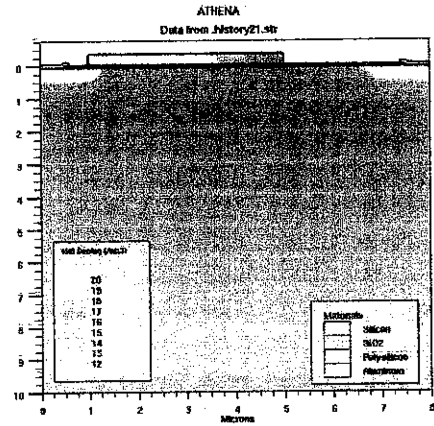
The device is fabricated by using an advance process simulator (ATHENA) where the actual process recipe used for wafer fabrication. The device structure is presented in a 2-D finite grid element and a device simulator (ATLAS) is used to simulate the electrical characteristics. The device is fabricated on p-type substrate grown by boron implantation with concentration of 1.0 x 10^{15}cm^{-3} and <100> orientation. The Gussian doping profile is used in the simulation with appropriate x- and y- direction. After a sacrificial oxide deposition and etching, 500Å of gate oxide is thermally grown at about 985 °C. 0.4μm Polysilicon is deposited over the oxide and the phosphorous is implanted and then annealed as shown in the figure (a). The boron is implanted with dose of 9 x 10^{11}cm^{-3} and energy of 20 Kev for V_T adjustment and results the threshold voltage about 1.3 V. After the V_T adjustment is done, the lightly doped drain (LDD) feature is fabricated result in the figure (b). This part is also known as drift region and it is a critical for achieving the desired breakdown voltage. LDD is formed by blanket implant of phosphorous (2 x 10^{12} cm^{-3}, 100 Kev). P-type body region under the gate forms the channel. Then source and drain regions are formed using implantation of phosphorous (3 x 10^{15} cm^{-3}, 100 Kev) as shown in the figure (c). After several thermal steps for dopant activation and oxide densification and final annealing, the metallization of aluminum are formed for source and drain contact, figure (d).

(a): Polysilicon gate deposition

(b): LDD Formation



(c): Source and Drain Formation



(d): Source and Drain Contact Metal

Figure 5: LDMOS Fabrications Process

3.4. Tools Required

i. **Silvaco TCAD workstations.**

ii. **Silvaco ATHENA simulation software** – To predict the physical structure of the device that result from processing.

iii. **ATLAS simulation software** – To predict the electrical characteristics associated with specified bias conditions.

CHAPTER 4

RESULT AND DISCUSSION

4.1. Standard LDMOS Structure

4.2.1. Process Simulation

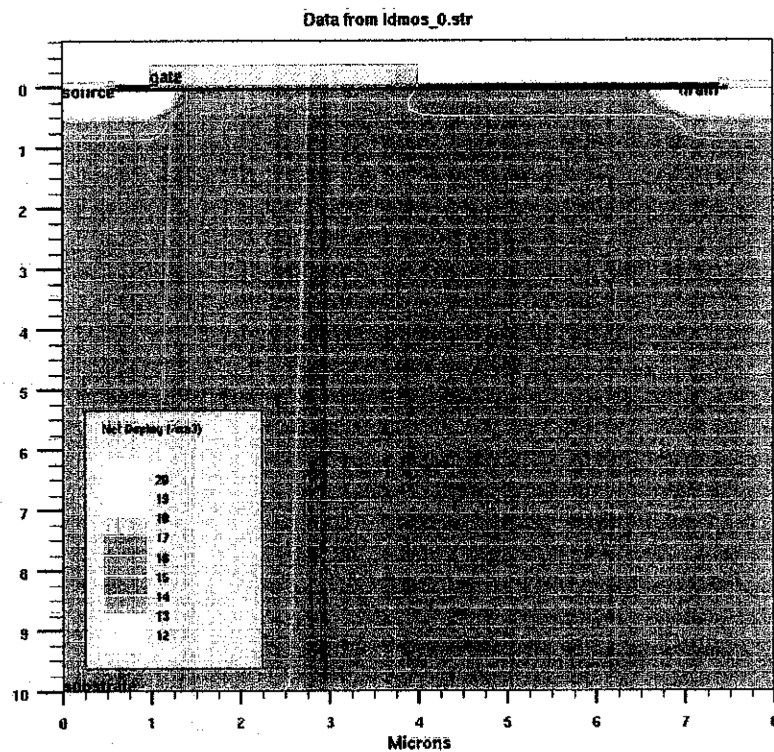


Figure 6: LDMOS Structure Simulated

Base on the figure 6 above, it shows an LDMOS structure simulated in ATHENA. The gate and channel length is 3 μm and its electrical characteristics were extracted so that the performance of the structure can be evaluated. The dimensions of the device structure are shown in the table 2.

Table 2: Dimension of LDMOS structure

Parameters	Dimension (μm)
Source length, l_s	0.6
Source-gate spacing, l_{so}	0.4
Gate length, l_g	3.0
LDD length, l_{ldd}	3.4
Drain length, l_d	0.6

The LDD region is grown at 3.4 μm. This leads to a large electric field in the oxide region and correspondingly large field in silicon substrate underneath the gate [5]. The graded doping in LDD is needed to ensure that the breakdown occurs not at the surface but deeper into the substrate. The electric field distribution of LDMOS studied is shown in the figure 7. Electric field only exists in the PN-junction where a depletion region is created as shown in Figure 7. Holes diffuse from P to N side and electron diffuse from N to P side results positively charged donor ions are left behind on the N side while negatively charged acceptor ions on the P side. The existence of positively charges on one side and negatively charges on the other side causes an electric field directed from N to P [20]. LDD region is formed to decrease the electric field at the drain end of the channel and to optimize breakdown voltage [3].

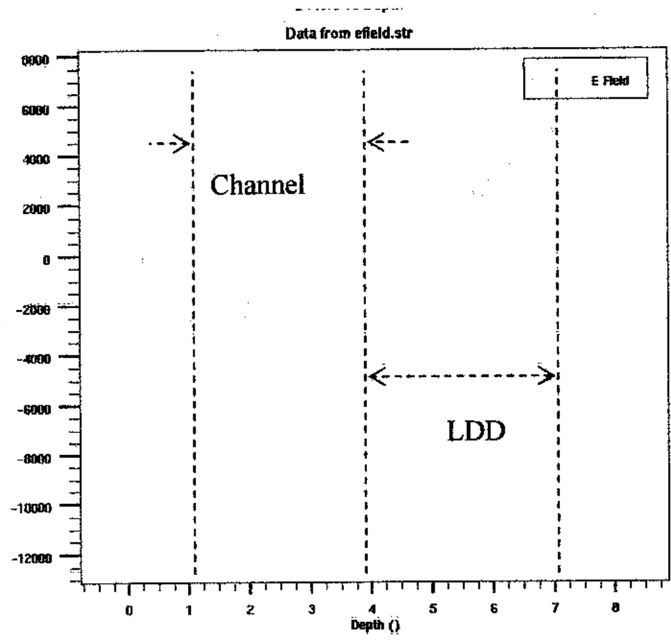


Figure 7: Electric field distribution across the region

4.2.2. Concentrations Profile

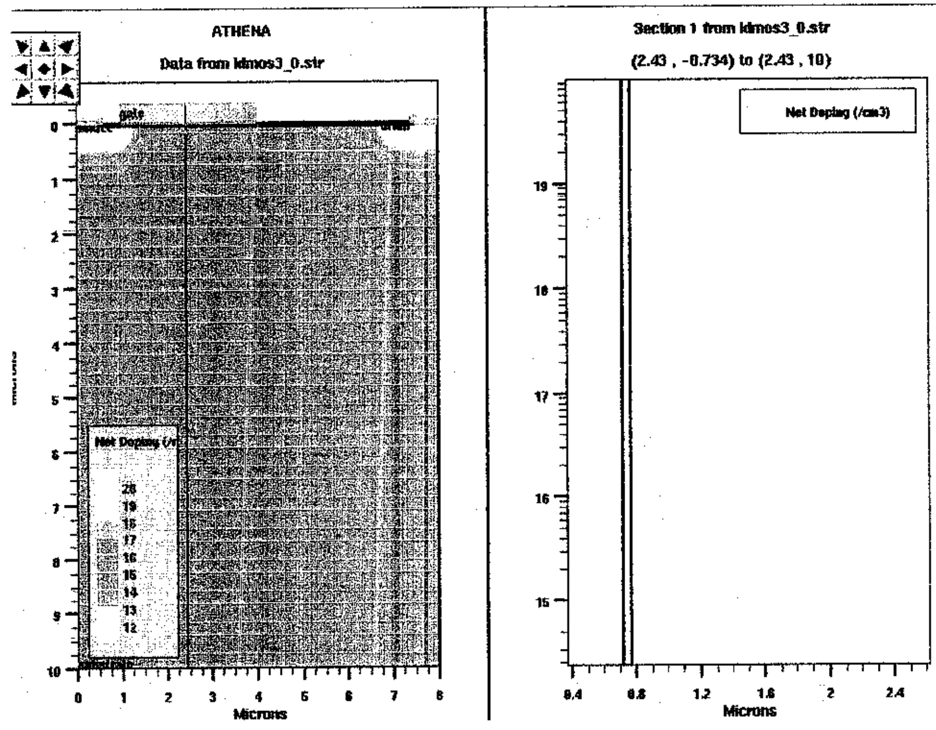


Figure 8: Doping Profile across the channel

The figure 8 shows the doping profile of the extrinsic semiconductor of LDMOS across the channel. The maximum concentration of the P-type channel is $10^{17}cm^{-3}$ and reducing as the cut line go far inside the device. As the depth of device increases, the net doping concentration in P-type substrate is constant at $10^{15}cm^{-3}$ starting from depth of 1.2μm. The doping concentration inside the polysilicon gate is higher up to $10^{19}cm^{-3}$ with the thickness of 0.4 μm. The P-type channel is formed by implantation of boron (acceptor) which is material from group III of periodic table.

On the other hand, the figure 9 shows the doping profile of the LDMOS across the LDD region. The LDD region is formed by implantation of phosphorous (donor) which is from group V of periodic table. The maximum concentration of donor inside the LDD region is about $10^{17}cm^{-3}$ and reduced to $10^{15}cm^{-3}$ starting the depth of 1.2μm and become constant as the depth is increased.

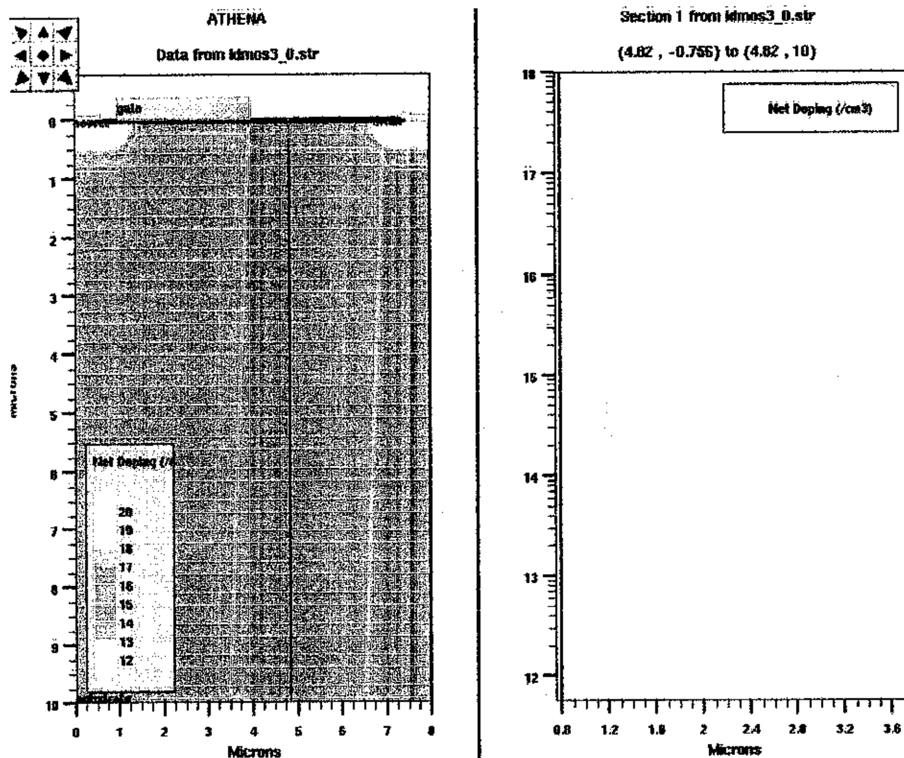


Figure 9: Doping Profile across the LDD region

4.2.3. Atlas Simulation for standard structure

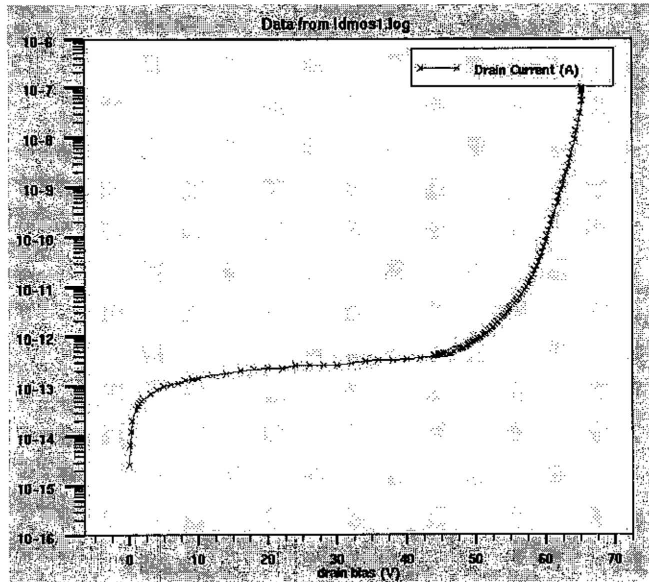


Figure 10: I_D versus Drain bias for breakdown performance

Figure 10 above shows the breakdown characteristics at the gate voltage of 0 V. Drain voltage, V_D is ramped up to 80 V and the maximum breakdown voltage achieved is 65.5 V as shown in the Table 3.

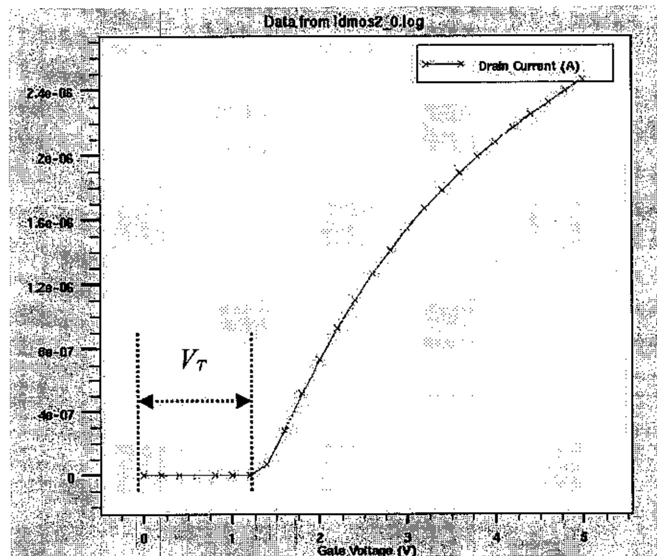


Figure 11: Drain current, I_D versus Gate voltage, V_G

Figure 11 shows the characteristics of I_D versus V_G at drain voltage 0.1 V. From the figure, the threshold voltages, V_T is 1.31023 V.

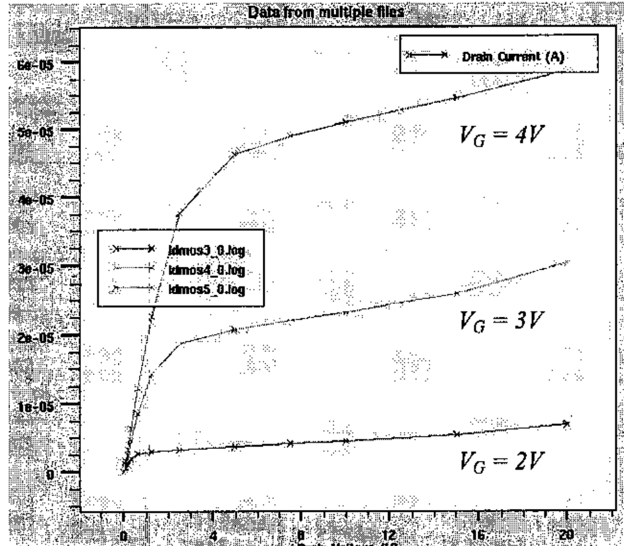


Figure 12: Drain current, I_D, versus Drain voltage, V_D

Base on the figure 12 above, the drain current, I_D characteristics versus drain voltage, V_D is plotted for different gate voltage, V_G. V_G is varied for 2V, 3V and 4V. This shows that the current is affected by the gate voltage. As V_G is increased, I_D will increase when the drain is biased. The DC characteristics are summarized as in the table 3.

Table 3: DC parameter extracted for standard LDMOS structure

Parameters	Extracted Value
Gate oxide thickness, *Å*	501.197
Breakdown voltage, *V*	65.3579
Threshold Voltage, *V*	1.31023
Leakage current / Ids max, *A/um*	2.4657×10^{-06}
Input capacitance (Cgg), *Ciss, F*	-1.24953×10^{-15}
Output capacitance (Cdd), *Coss, F*	$-1.196927 \times 10^{-16}$
Feedback capacitance (Cgd), *Crss, F*	1.04498×10^{-16}
Cut of Frequency, *Ft, Ghz*	2.73211
Transconductance, g_m $(\mu\Omega^{-1}/\mu m)$	-21.43900

4.2. Gate oxide Thickness, T_{ox} Adjustment

Gate oxide thickness is varied from 200 Å to the 700 Å with the constant net doping profile. The standard T_{ox} is 500Å. The results are captured and recorded.

4.2.1. Effect on Device Threshold Voltage

Table 4: Threshold voltage for varied gate oxide thickness

gate oxide thickness (Å)	Threshold Voltage (V)
200	0.454967
300	0.792578
400	1.02949
500	1.31023
600	1.40777
700	1.36659

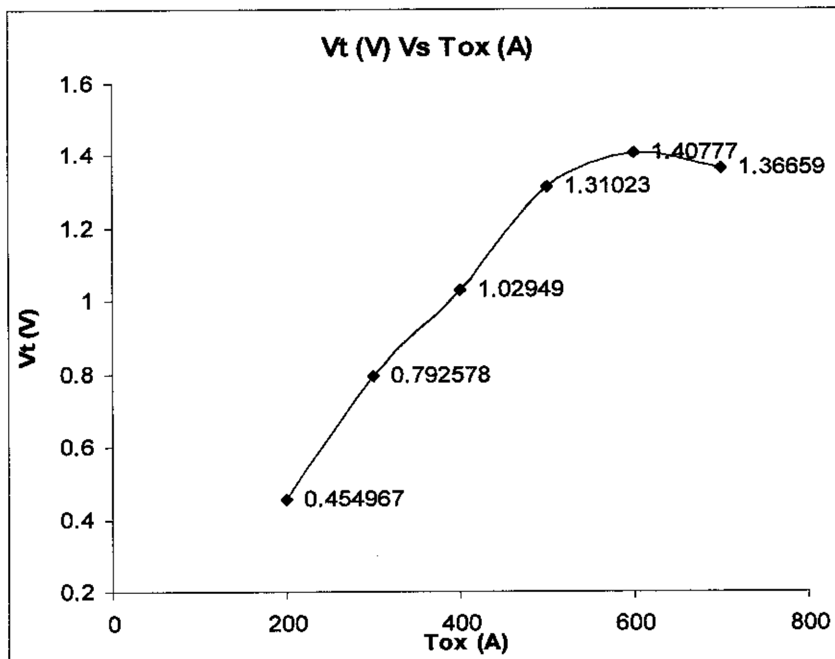


Figure 13: Threshold voltage versus gate oxide thickness

The V_T obtained from the simulation of I_D versus V_G for maximum V_G is 3.3 V. From [11], stated the threshold voltage V_T of the MOS device is a function of the gate oxide layer thickness T_{ox}. On the other vital parameters, such as the effective channel length L_{eff} and total drain and source series resistance are less clear. From the curve of threshold voltage versus gate oxide thickness, it shows that the V_T is linear to the gate oxide thickness, T_{ox} where the threshold voltage is increasing as the gate oxide thickness is being increased.

For a fixed V_G, the vertical electric field at the surface of the semiconductor along the channel becomes constant. When the gate oxide thickness, T_{ox}, is increased, the vertical electric field along the channel reduces which necessitates an increment in V_G to cause strong inversion and thus increase the V_T. The amount of field reduced is related to the increased voltage drop in the oxide and governing by Gauss law, the slope of V_T versus T_{ox}, should be approximately equal to the electric field in the oxide [11]. However, for the MOS device, it is better to have low threshold voltage. The threshold voltage can be represented by the equation below obtained from [10]:

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_s qN(2\psi_B)}}{C_{ox}} \tag{1}$$

Where

V_{FB} = Flat band voltage

$2\psi_B$ = Surface bending

$\frac{\sqrt{2\varepsilon_s qN(2\psi_B)}}{C_{ox}}$ = Voltage across oxide layer

and

$$V_{ox} = \frac{Q}{C_{ox}} \tag{2}$$

$$Q = \sqrt{2\varepsilon_s qN(2\psi_B)}$$

$$C_{ox} = \varepsilon \frac{A}{T_{ox}}$$

From the equation above, the oxide capacitance is inversely proportional to the gate oxide thickness where as the gate oxide thickness, T_{ox} increase, the oxide capacitance, C_{ox} will be reduced results an increasing in voltage across the oxide layer. Finally, the threshold voltage will increase as the T_{ox} increase. The flat band voltage of real MOS structures is further affected by the presence of charge in the oxide or at the oxide-semiconductor interface. The flat band voltage still corresponds to the voltage which when applied to the gate electrode yields a flat energy band in the semiconductor. The charge in the oxide or at the interface changes this flatband voltage. For a charge, Q_i, located at the interface between the oxide and the semiconductor, and a charge density, ρ_{ox}, distributed within the oxide, the flat band voltage is given by [13]:

$$V_{FB} = \Phi_{MS} - \frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x) x dx \tag{15}$$

4.2.2. Effect on Device Transconductance, g_m

Table 5: Transconductance, for varied gate oxide thickness

gate oxide thickness (Å)	Transconductance, gm ($\mu\Omega^{-1}/\mu m$)
200	-28.51730
300	-25.37960
400	-24.11830
500	-21.43900
600	-19.08000
700	-15.90369

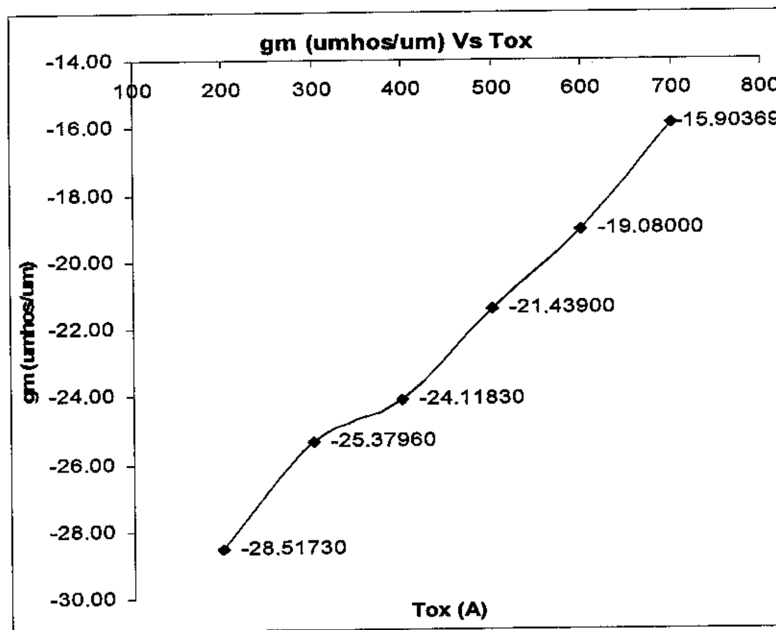


Figure 14: Transconductance versus gate oxide thickness

From [10],

$$g_{m,sat} = WC_{ox}v_{sat} \tag{11}$$

where

W = Width of the device

C_{ox} = Oxide Capacitance

v_{sat} = velocity saturation of carriers

$v_{sat} = 1\times10^{7}\ cm/s$ for silicon

From the plot shows, the transconductance of the LDMOS is reduced in magnitude as the gate oxide is increased. The transconductance is given by the equation above where it is directly proportional to the capacitance of the oxide layer, C_{ox}, width of the device and the velocity saturation of the carriers. For this device, silicon is used

which is v_{sat} = 1 x 10^7 cms^{-1}. Since the W and v_{sat} are constant, the $g_{m,sat}$ is directly proportional to the oxide capacitance where: $C_{ox} = \varepsilon \frac{A}{T_{ox}}$ (16)

As the gate oxide thickness, T_{ox} increases, the magnitude of oxide capacitance, C_{ox} is reduced results the transconductance, $g_{m,sat}$ will be reduced in magnitude.

4.2.3. Effect on Device input Capacitance, C_{iss}

Table 6: Input capacitance, for varied gate oxide thickness

gate oxide thickness (Å)	Input Capacitance, Ciss (fF)
200	-1.86921
300	-1.60639
400	-1.39653
500	-1.24953
600	-1.07135
700	-0.87481

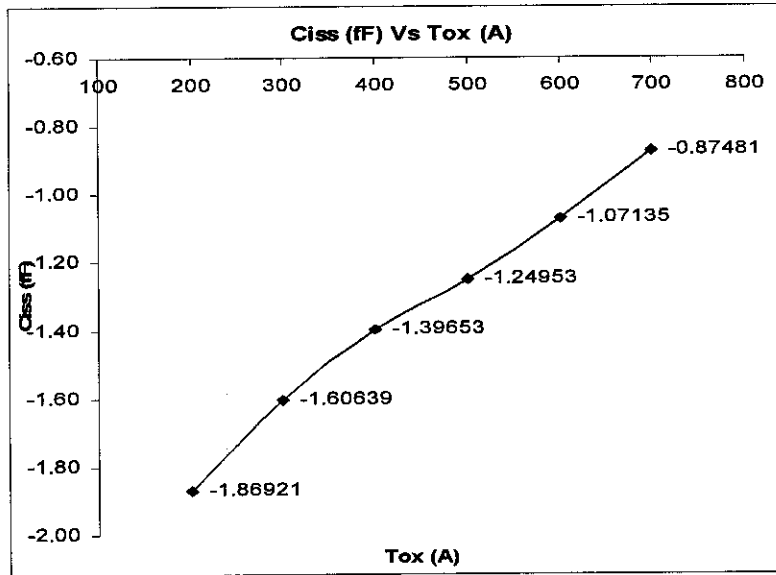


Figure 15: Input Capacitance, Ciss versus gate Oxide Thickness

$$C_{iss} = C_{GS} + C_{GD} \quad (17)$$

where

C_{GS} = gate to source capacitance

C_{GD} = gate to drain capacitance

and $$C_{iss} \approx \frac{\varepsilon_{ox} WL}{T_{ox}} = C_{ox} WL \quad (18)$$

W = width of the device

L = Length of the gate

T_{ox} = Gate oxide thickness

The input capacitance C_{iss}, is given by the equation above from [13] and [17]. The input capacitance C_{iss}, is proportional to the gate oxide capacitance, C_{ox},. As the oxide thickness T_{ox} is increased, the oxide capacitance C_{ox} will be reduced hence the input capacitance C_{iss} is reduced in its magnitude.

4.2.4. Effect on device Cut off Frequency, f_T

Table 7: Cut of Frequency for varied Gate Oxide thickness

gate oxide thickness (Å)	Cut Off Frequency (GHz)
200	2.42935
300	2.51579
400	2.75003
500	2.73211
600	2.83589
700	2.89484

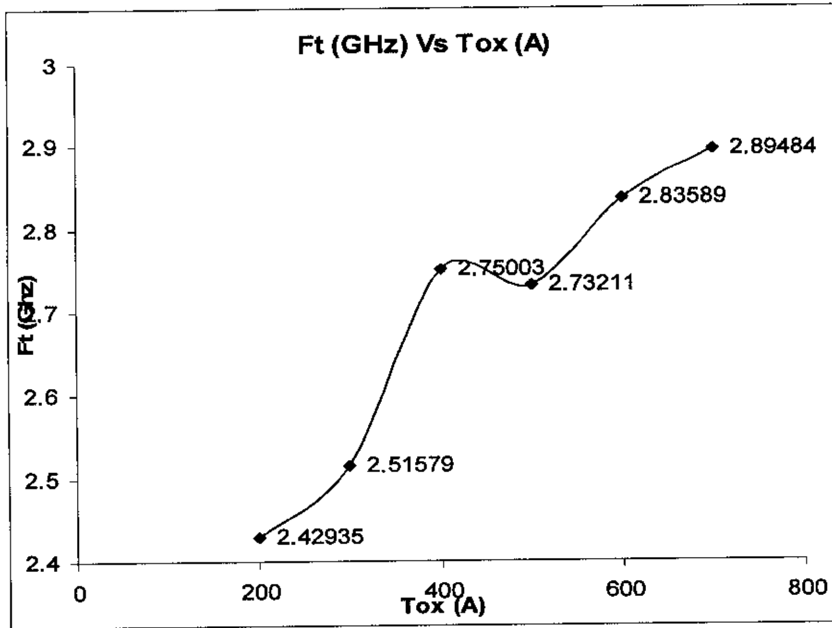


Figure 16: Cut off Frequency versus Gate Oxide Thickness

From [17]

$$f_T = \frac{g_m}{2\pi C_{in}} \quad (19)$$

where

g_m = Transconductance

C_{in} = Input paracitic capacitance C_{iss}

The cut off frequency is given by the equation above. Its can be analyzed that, the cut off frequency, f_t is directly proportional to the tranconductance, g_m and inversely proportional to the input parasitic capacitance, C_{iss}. From the curve of g_m versus T_{ox} and C_{iss} versus T_{ox}, both g_m and C_{iss} are reduced in magnitude as the gate oxide thickness; T_{ox} is increased while the oxide capacitance, C_{ox} also directly reduced. However the reduction of input capacitance is higher compare to the reduction of

transconductance, g_m results the cut off frequency, f_t is increased. The percentage reduction for both g_m and C_{iss} as follows:

1. g_m reduction:

$$\% \text{ of reduction} = \frac{g_{m,\max} - g_{m,\min}}{g_{m,\max}} \times 100\%$$

$$g_{m,\max} = 28.5173\mu mhos/\mu m \quad \text{and} \quad g_{m,\min} = 15.90369\mu mhos/\mu m$$

$$\therefore \% \text{ of reduction} = \frac{28.5173\mu mhos/\mu m - 15.90369\mu mhos/\mu m}{-28.5173\mu mhos/\mu m} \times 100\%$$

$$= 44.23\%$$

2. C_{iss} reduction:

$$\% \text{ of reduction} = \frac{C_{iss,\max} - C_{iss,\min}}{C_{iss,\min}} \times 100\%$$

$$C_{iss,\max} = 1.86921 fF \quad \text{and} \quad C_{iss,\min} = 0.874809 fF$$

$$\therefore \% \text{ of reduction} = \frac{1.86921 fF - 0.874809 fF}{-1.86921 fF} \times 100\%$$

$$= 53.2\%$$

The percentage of reduction for input capacitance, C_{iss} is higher than g_m. It shows that the cut off frequency, f_t is more affected by the changes of input capacitance, C_{iss} rather than g_m. As T_{ox} is increased, magnitude of C_{iss} is reduced and f_t will be increased.

4.2.5. Effect on Device Breakdown Voltage

Table 8: Breakdown voltage for varies gate oxide thickness

gate oxide Thickness (Å)	Breakdown Voltage (v)
200	65.0364
300	66.6256
400	65.2002
500	65.3579
600	64.0703
700	61.4375

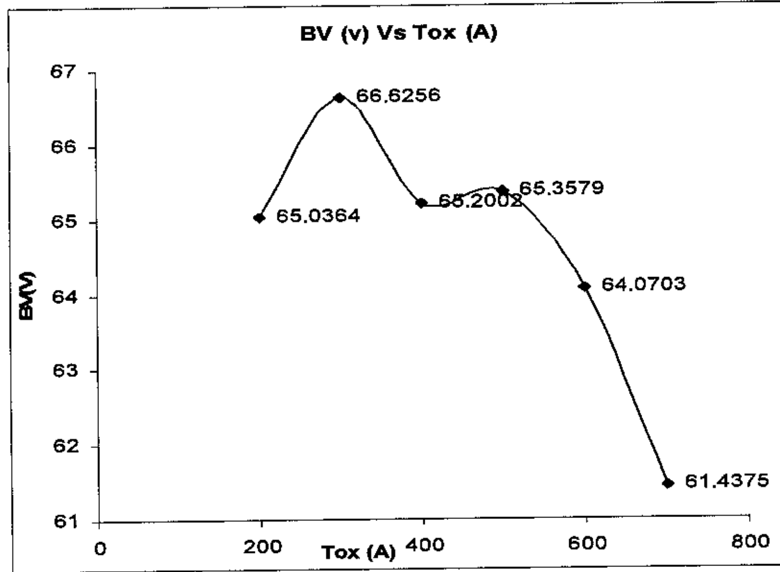


Figure 17: Breakdown Voltage versus Gate Oxide Thickness

A problem that limits a breakdown voltage of LDMOS is the concentration of the electric field at the tip of both source and drain [5]. The breakdown occurs at a certain critical value of electric field. From [12], the relationship between electric field, E and gate oxide thickness, T_{ox} for MOS device is given by:

$$E_m = \frac{(V_{DS} - V_{Dsat})}{0.22 T_{ox}^{1/3} X_j^{1/2}} \quad (20)$$

where

E_m = Maximum Electric field

$V_{DS} - V_{Dsat}$ = Voltage drop in velocity saturation (pinch - off)

T_{ox} = Oxide Thickness

X_j = Depth

From [20], breakdown occurs at $E_{cr} = E_m$ so that the breakdown voltage is given by the following relationships:

$$V_{br} = \frac{\varepsilon E_{cr}^2}{2qN_D} \; and \; V_{br} \alpha \frac{1}{N_D}$$

$$\begin{aligned} &where \\ &\varepsilon = \text{Permitivity} \\ &E_{crit} = \text{Critical surface Field} \\ &q = \text{Electron charge} \\ &N_D = \text{Doping concentration} \end{aligned} \qquad (21)$$

From the relationship above, it shows that the breakdown voltage for MOS device is directly proportional to the square of critical electric field, E_{crit}. However, the breakdown is occurs at $E_{cr} = E_m$, so that the critical electric field is inversely proportional to the gate oxide thickness, T_{ox}. Can be analyzed that, as the gate oxide thickness, T_{ox} is increased, the critical electric field, E_{crit} will be reduced results in reducing of breakdown voltage. From the results obtained for breakdown voltage, BV versus gate oxide thickness, T_{ox} curve, it is shows that the theory is satisfied. Besides, as the gate-oxide is scaled down, breakdown of the oxide and oxide reliability becomes more of a concern. Higher fields in the oxide increase the tunneling of carriers from the channel into the oxide. These carriers slowly degrade the quality of the oxide and lead over time to failure of the oxide. This effect is referred to as time dependent destructive breakdown [11].

4.3. LDD Doping, N_D Adjustment

The LDD doping profile is varied for different concentration. The standard concentration used is $2x10^{12}$ cm^{-3}. The LDD concentration is varied for $2x10^{10}$, $2x10^{11}$ and $2x10^{13}$ cm^{-3} while the gate oxide thickness is maintain constant at 500Å.

4.3.1. Effect on Device Threshold Voltage

Table 9: Threshold voltage for different LDD concentration

Doping (/cm3)	Threshold Voltage (v)
$2.00x10^{10}$	-5.66969
$2.00x10^{11}$	-11.6568
$2.00x10^{12}$	1.31023
$2.00x10^{13}$	1.32769

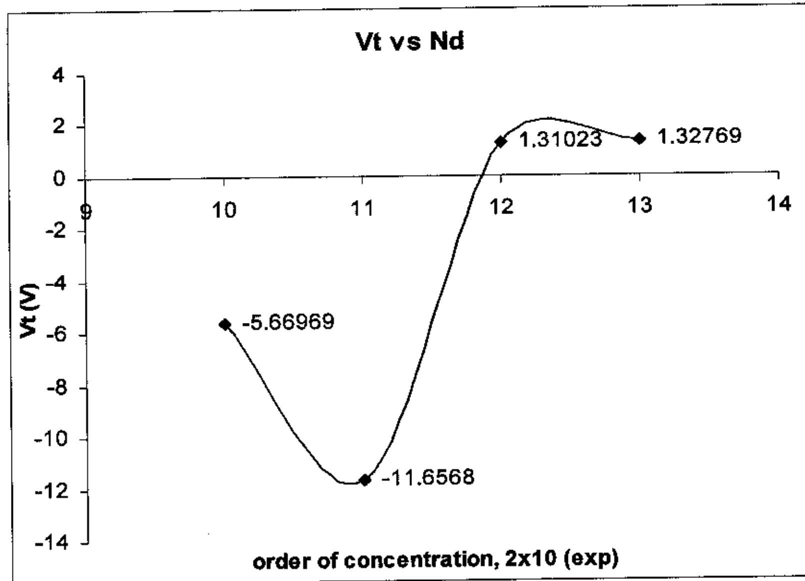


Figure 18: Threshold Voltage vs LDD concentration

The threshold voltage is given by the same equations [10]:

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_s qN(2\psi_B)}}{C_{ox}} \quad \text{Where} \qquad (1)$$

V_{FB} = Flat band voltage; $2\psi_B$ = Surface bending;

$$\frac{\sqrt{2\varepsilon_s qN(2\psi_B)}}{C_{ox}} = \text{Voltage across oxide layer}$$

and

$$V_{ox} = \frac{Q}{C_{ox}} = \text{voltage across the oxide layer} \quad (2)$$

$$Q = \sqrt{2\varepsilon_s qN(2\psi_B)} = \text{Charge in the oxide layer}$$

$$C_{ox} = \varepsilon \frac{A}{T_{ox}} = \text{Oxide capacitance}$$

As the gate oxide thickness is remains constant for 500 Å, the gate oxide capacitance, C_{ox} will be constant. While varying the LDD doping or donor concentration N_D, from $2x10^{10}$ to $2x10^{13}$ cm^{-3}, the concentration of the charge in the oxide layer, Q will be varied. As the N_D is reduced, the charge Q will be reduced hence reducing the voltage across the oxide, V_{ox}, hence reducing the threshold voltage, V_T. Otherwise, when the N_D is increased, Q will be increased hence the V_{ox} is increased and finally increase the V_T. From the results obtained, the threshold voltage become negative when concentration of LDD is reduced below than $2x10^{12}cm^{-3}$ and it means that there is a leakage current occurs in the device. At this condition, the device is not working properly due to the higher current leakage. For this level, can be concluded that the optimum LDD doping profile is $2x10^{12}cm^{-3}$ since the device require lowest threshold voltage for minimum switching time.

4.3.2. Effect on Device Transconductance, g_m

Table 10: Transconductance for different LDD Concentration

Doping (/cm3)	Transconductance, gm ($\mu\Omega^{-1}/\mu m$)
2.00×10^{10}	-1.39×10^{-12}
2.00×10^{11}	-1.30×10^{-12}
2.00×10^{12}	-2.14×10^{-05}
2.00×10^{13}	-4.19×10^{-05}

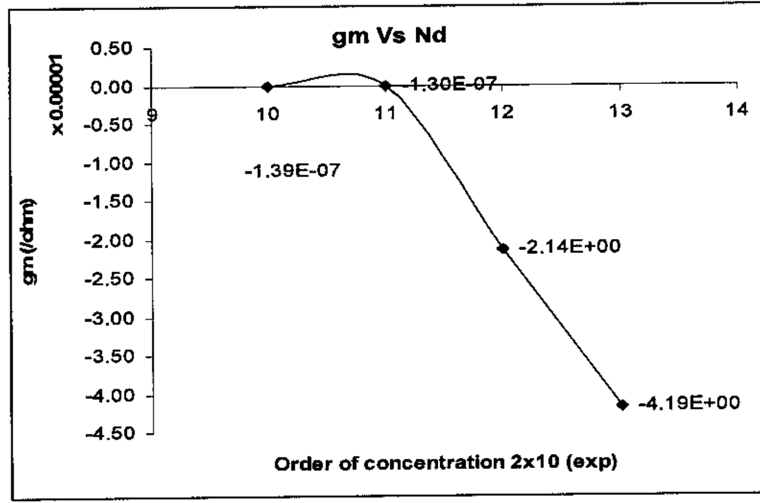


Figure 19: Transconductance vs LDD Concentration

From [17]:

$$g_m = \frac{W\mu_n C_{ox}}{L} V_D \quad (22)$$

W = Channel Width
L = Channel Length
μ_n = mobility of the electron

From [19]:

$$W = \frac{qN(\xi x_{dT}^2)}{C_{ox}(\Delta V_T)} \quad (23)$$

ξ = fitting parameters
q = electron charge
x_{dT} = vertical width
C_{ox} = oxide capacitance
ΔV_T = changes in threshold voltage

Transconductance is defined as the changes in drain current with respect to the corresponding change in gate voltage [19]. From the equation above can be analyzed that the tranconductance, g_m is proportional to the width of the channel, W, carrier mobility, μ_n, oxide capacitance, C_{ox} and inversely to the length of the channel. From

[18], in highly doped samples will cause more scattering and have lower carrier mobility. According to equation (23), it shows that W is directly proportional to N where $N = N_D$. As LDD region is highly doped, channel width, W will be increased result in increasing of the magnitude of transconductance, g_m. From the plot, at the LDD doping is below than $2x10^{12}cm^{-3}$, the transconductance become nearly zero since at that level the device is not working properly due to leakage as discussed in previous sections.

4.3.2. Effect on Device input Capacitance, C_{iss}

Table 11: Input Capacitance for different LDD Concentration

Doping (/cm3)	Input Capacitance Ciss (fF)
$2.00x10^{10}$	-1.55583
$2.00x10^{11}$	-1.55365
$2.00x10^{12}$	-1.24953
$2.00x10^{13}$	-1.21202

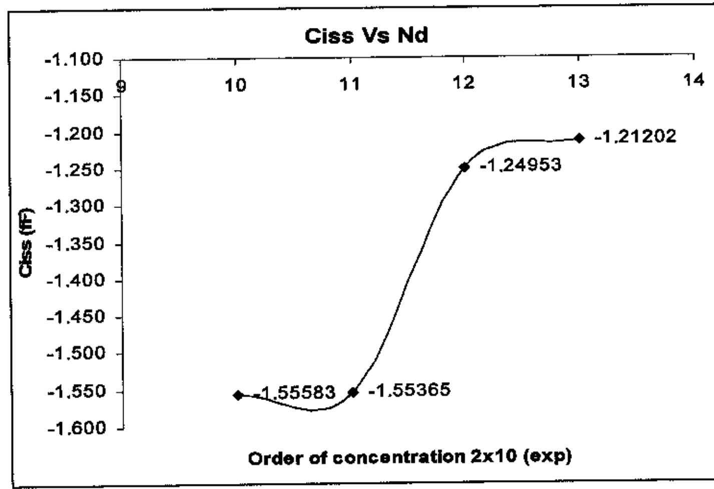


Figure 20: Input Capacitance vs LDD concentration

From [17]:

$$C_{iss} \approx \frac{\varepsilon_{ox} WL}{T_{ox}} = C_{ox} WL \qquad (24)$$

From [19]

$$L = \frac{W\mu_n C_{ox}}{g_m} V_D \qquad (25)$$

$$W = \frac{qN(\xi x_{dT}^2)}{C_{ox}(\Delta V_T)} \qquad (26)$$

W = channel width
μ_n = carrier mobility
C_{ox} = oxide capacitance
V_D = drain voltage
g_m = transconductance

ξ = fitting parameters
q = electron charge
x_{dT} = vertical width
C_{ox} = oxide capacitance
ΔV_T = changesin threshdd voltage

The input capacitance C_{iss} is given by equation above (24). Input capacitance, C_{iss} is directly proportional to the width and channel length obtained from [17]. Channel length, L is given by equation (25) obtained from [19] shows that L is inversely proportional to transconductance, g_m. As doping concentration increased, N_D, g_m is increased, results L is being reduced and correspond to decrease the magnitude of input capacitance, C_{iss}. At the same time, channel width is increased as concentration increased but in the small values of changes. From the plot obtained, the C_{iss} is follows the relationship above. The C_{iss} for N_D below than $2x10^{12}cm^{-3}$, C_{iss} is too small due to device failure.

4.3.4. Effect on device Cut off Frequency

Table 12: Cut Off frequency for Different LDD Concentration

Doping (/cm3)	Cut Off Frequency (Hz)
$2.00\text{x}10^{10}$	142.323
$2.00\text{x}10^{11}$	132.733
$2.00\text{x}10^{12}$	$2.73\text{x}10^{+09}$
$2.00\text{x}10^{13}$	$5.50\text{x}10^{+09}$

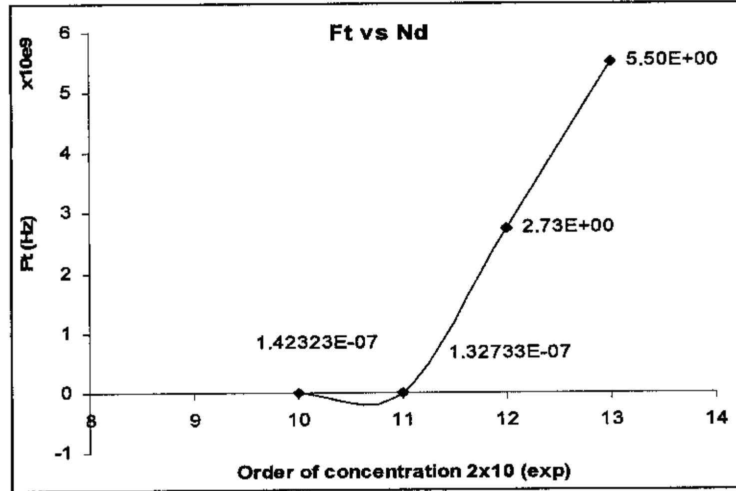


Figure 21: Cut off Frequency vs LDD Concentration

From the results obtained for cut off frequency versus LDD doping concentration, very low frequency is obtained for LDD concentration of $2\text{x}10^{11}$ and $2\text{x}10^{10}\text{cm}^{-3}$. This is because the effect of channel leakage and device in failure condition. Again the cut off frequency, f_t is given by [17]:

$$f_T = \frac{g_m}{2\pi C_{in}} \quad \begin{array}{l} \text{where} \\ g_m = \text{Transcondu ctance} \\ C_{in} = \text{Input paracitic capacitanc e } C_{iss} \end{array} \qquad (19)$$

Cut off frequency, f_t is directly proportional to the transconductance, g_m, and inversely proportional to the input capacitance C_{iss}. The curve for f_t versus LDD concentration obtained is linear to the curve of g_m versus LDD concentration however the g_m is in negative direction. From the g_m curve, more negative of g_m is higher its magnitude results in higher of cut off frequency will be obtained. The input capacitance, C_{iss} is not much give the affect to the cut off frequency even it is reducing in its magnitude since smaller magnitude of C_{iss}.

4.3.5. Effect on Device Breakdown Voltage

Table 13: Breakdown Voltage for different LDD Concentration

Doping (/cm3)	Breakdown voltage (V)
2.00×10^{10}	42.2682
2.00×10^{11}	48.125
2.00×10^{12}	65.3579
2.00×10^{13}	21.7892

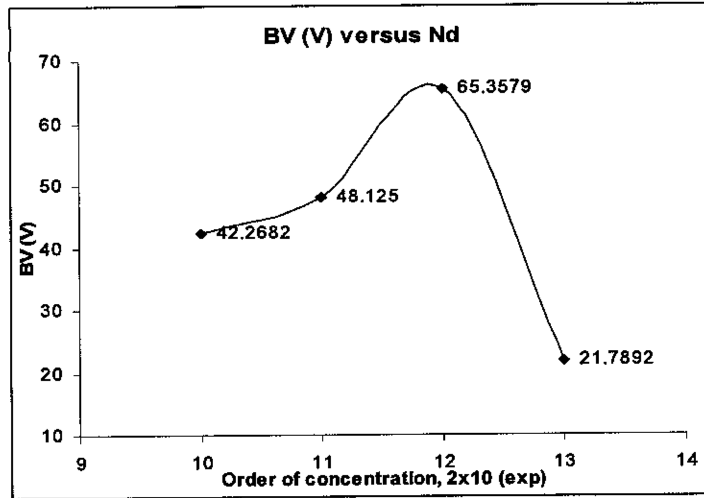


Figure 22: Breakdown Voltage vs LDD Concentration

$$V_{br} = \frac{\varepsilon E_{cr}^2}{2qN_D} \; and \; V_{br} \alpha \frac{1}{N_D} \tag{28}$$

$$\begin{aligned} &where \\ &\varepsilon = \text{Permitivity} \\ &E_{cr} = \text{Critical surface Field} \\ &q = \text{Electron charge} \\ &N_D = \text{Doping concentration} \end{aligned}$$

From the results obtained for breakdown voltage, the maximum breakdown voltage is obtained at the LDD concentration of $2 \times 10^{12} cm^{-3}$. The breakdown voltage is limited by the critical electric field on the P-N junction. Means that the higher critical electric field, E_{cr}, higher breakdown voltage, V_{br} will be achieved. From the relationship above obtained from [20], the breakdown voltage is inversely

proportional to the concentration of the donor, N_D. As the N_D is increased, the lower breakdown will be achieved however it will be limited by the critical electric field, E_{cr}. The E_{cr} is given by:

$$E_{max} = -\left(\frac{2qN_D V_{bi}}{\varepsilon}\right)^{\frac{1}{2}} \quad (29)$$

Breakdown occurs at $-V_{br}$

$$E_{cr} = E_{max}; \quad V_{bi} << V_a$$

V_{bi} = Build in voltage

E_{cr} = Critical field

E_{max} = Maximum field

N_D =Donor concentration

q = electron charge

$\varepsilon = \varepsilon_o \varepsilon_r$ = permitivity

4.4. Summary of the Results

From the result of varying the gate oxide thickness, T_{ox} and LDD doping concentration N_D, the effect on the breakdown voltage, BV, cut off frequency, f_t, threshold voltage, V_T, transconductance, g_m and input capacitance, C_{iss} are analyzed. The function and essentiality of those parameters are summarized below:

Table 14: Effect of parameters

Parameter	Requirement	Function
Breakdown voltage, BV	Higher	- Provide higher range of voltage operation - Higher limit for high voltage applications
Cut Off Frequency, f_t	Higher	- Provide higher range frequency operation - Provide higher frequency limit for high frequency applications
Threshold Voltage, V_T	Lower	- Low threshold voltage for reducing switching time - Reducing switching loss
Transconductance, g_m	Higher	- Provide higher cut off frequency - Provide higher gain
Input Capacitance, C_{iss}	Lower	- Gives higher cut off frequency

The table below shows the summary of the result obtained from varying the gate oxide thickness, T_{ox} and LDD doping concentrations, N_D.

Table 15: Summary of the results

		BV	F_t	g_m	C_{iss}	V_T
Varying T_{ox}	**Highest**	300Å	700Å	200Å		
	Lowest				700Å	200Å
Varying N_D	**Highest**	$2x10^{12}$	$2x10^{13}$	$2x10^{13}$		
	Lowest				$2x10^{13}$	$2x10^{12}$

Gate oxide thickness adjustment

Higher breakdown voltage, BV and higher magnitude of transconductance are achieved at gate oxide thickness, T_{ox} equal to 300Å and 200Å respectively. Higher cut off frequency, f_t, achieved at 700Å of T_{ox}. Meanwhile, lower input capacitance, C_{iss} and threshold voltage, V_T, achieved at T_{ox} 700Å and 200 Å respectively.

LDD doping concentration adjustment

Higher breakdown voltage is obtained when the LDD region is doped with $2x10^{12}cm^{-3}$ of phosphorous. However, higher cut off frequency, f_t and transconductance, g_m achieved at concentration of $2x10^{13}cm^{-3}$. Meanwhile, lower input capacitance, C_{iss} and threshold voltage, V_T achieved at concentration of $2x10^{13}cm^{-3}$ and $2x10^{12}cm^{-3}$ respectively.

For the time being, the optimum values for gate oxide thickness, T_{ox} and LDD doping concentrations, N_D are at 500 Å and $2x10^{12}cm^{-3}$ respectively since the optimum values for device parameters are achieved.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1. Conclusions

The effect of gate oxide thickness and doping profile of LDD on the performance of LDMOS were analyzed. Higher breakdown voltage, *BV,* and higher cut off frequency, *Ft,* will provide higher range of LDMOS operation capability. Higher transconductance, g_m and lower input capacitance, C_{iss} will result in higher gain and higher cut off frequency. Lower threshold voltage, V_T is required to minimize the device switching time. The optimum parameter of gate oxide thickness and LDD doping profile are required to improve the LDMOS performance. For the time being, the optimum values for gate oxide thickness, T_{ox} and LDD doping concentrations, N_D are 500 Å and $2x10^{12}cm^{-3}$ respectively since the optimum values for the device performance are achieved. The fundamental of semiconductor device fabrication and principle were studied and understood as well as the knowledge of using process and device simulator (Athena & Atlas) are acquired.

5.2. Recommendations

Through this project, the effect of gate oxide thickness, T_{ox} and LDD doping profile, N_D were studied as a part of work to improve LDMOS performance. Other process parameters of LDMOS fabrication also need to be investigated so that its performance can be further improved. For example the effect of channel length, L_c gate thickness, size of drain and source contact, type of materials as well as doping concentration, device dimensions also need to be investigated. In this work, phosphorous is being used as a donor to form LDD, source and drain region of LDMOS. However other materials from group V of periodic table such as arsenic also can be used. The effect of different material used also should be investigated and more time of research required. If more process parameters are studied the optimum values for process parameters can be easily determined so that better LDMOS performance can be achieved.

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APPENDICES

APPENDIX A

LDMOS ATHENA FABRICATION COMMAND

```
go  athena
#
line x loc=0 spac=0.4
line x loc=0.5 spac=0.1
line x loc=0.6 spac=0.1
line x loc=1 spac=0.08
line x loc=2 spac=0.3

line x loc=3 spac=0.5
line x loc=5 spac=0.05
line x loc=6 spac=0.3
line x loc=7 spac=0.1
line x loc=7.4 spac=0.1
line x loc=7.5 spac=0.1
line x loc=8 spac=0.4

#
line y loc=0.00 spac=0.01
line y loc=0.2 spac=0.015
line y loc=0.5 spac=0.06
line y loc=1    spac=0.12
line y loc=10.0 spac=2.0
#
init orientation=100 c.boron=1e15
# sacrificial oxide
diffus time=30 temp=1000 dryo2
#
etch oxide all
#
# gate oxide growth
# make sure more than one grid point is included within the gate oxide thickness
method grid.ox=0.01
diffus time=50 temp=985.911 dryo2 press=0.992457 hcl=3
#
extract name="gateox" thickness material="SiO~2" mat.occno=1 x.val=-10

# vt adjust implant
implant boron dose=9e11 energy=20 pearson

# Poly deposition
depo poly thick=0.35 divi=10

# Poly definition
etch poly left p1.x=1
etch poly right p1.x=4
# slightly relax grid
relax y.min=0.4 dir.y=f
relax y.min=0.4 dir.y=f

# Light n+ implant
implant phosphor dose=2e12 energy=100 pearson
# S/D mask and implant
depo barrier thick=0.01
etch barrier left p1.x=1.5
etch barrier right p1.x=7
implant phos dose=3.0e15 energy=100 pearson
strip

# final anneal
method fermi compress
impurity i.phosph poly /oxide trn.0=0.0
```

```
diffuse time=30 temp=1000 nitro press=1.0

# contact holes
etch oxide left p1.x=0.5
etch oxide right p1.x=7.5

# Contact metal deposition and etching
deposit alumin thick=0.1 divi=2
etch alumin start x=0.6 y=-10
etch cont x=0.6 y=10
etch cont x=7.4 y=10
etch done x=7.4 y=-10

# electrode naming
electrode name=source x=0.3
electrode name=gate x=2 y=0.0
electrode name=drain x=7.7
electrode name=substrate backside


# estimate threshold voltage
extract name="1dvt" 1dvt ntype x.val=3.0

structure outf=ldmos_0.str
tonyplot ldmos_0.str -set ldmos_0.set

#
extract name="efield" curve(depth,efield material="Silicon" mat.occno=1 \
        y.val=0.5) outfile="efield.str"

tonyplot efield.str

struct outfile=ldmos_0.str
```

APPENDIX B

ATLAS CURRENT VOLTAGE CHARACTERISTICS COMMAND

```
go atlas
#
mesh  infile=ldmos5_0.str
#
models cvt  srh print
impact selb


contact name=gate n.poly
interface qf=3e10
#
solve init
method newton trap maxtraps=10 climit=1e-4  ir.tol=1e-30 ix.tol=1e-30

solve init
#
log outf=ldmos.log
solve vdrain=0.03
solve vdrain=0.1
solve vdrain=0.25 vstep=0.25 vfinal=2 name=drain

solve  vstep=1 vfinal=10 name=drain

solve  vstep=2.0 vfinal=44 name=drain
solve  vstep=0.25 vfinal=80 name=drain compl=1.e-7 cname=drain \
    outf=ldmos_1.str master onefile
extract name="bv" max(v."drain")

tonyplot ldmos.log -set ldmos_log.set
tonyplot ldmos_1.str -set ldmos_1.set


solve init
solve vdrain=0.1
log outf=ldmos2_0.log

solve name=gate vgate=0 vfinal=5.0 vstep=0.5
extract name="vt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
        - abs(ave(v."drain"))/2.0)
extract name="beta" slope(maxslope(curve(abs(v."gate"),abs(i."drain")))) * \
        (1.0/abs(ave(v."drain")))
extract name="theta" ((max(abs(v."drain")) * $"beta")/max(abs(i."drain"))) - \
        (1.0 / (max(abs(v."gate")) - ($"vt")))

extract name="leak" max(abs(i."drain"))
extract name="idsmax" max(abs(i."drain"))
extract name="isubmax" max(abs(i."substrate"))


tonyplot ldmos2_0.log


log off
solve vgate=2.0 outfile=solve1
solve vgate=3.0 outfile=solve2
solve vgate=4.0 outfile=solve3
#
load infile=solve1
log outf=ldmos3_0.log
solve name=drain vdrain=0 vfinal=20 vstep=5.0
```

```
load infile=solve2
log outf=ldmos4_0.log
solve name=drain vdrain=0 vfinal=20 vstep=5.0

load infile=solve3
log outf=ldmos5_0.log
solve name=drain vdrain=0 vfinal=20 vstep=5.0

tonyplot -overlay ldmos3_0.log ldmos4_0.log ldmos5_0.log
```

APPENDIX C

ATLAS PARASITIC EXTRACTION COMMAND

```
go atlas
#
mesh infile=ldmos1_0.str
#
models cvt srh print
impact selb


contact name=gate n.poly
interface qf=3e10
#
solve init
method newton trap maxtraps=10 climit=1e-4 ir.tol=1e-30 ix.tol=1e-30

solve init

log outf=cap.log
solve vgate=0 vdrain=28 ac freq=1e6

extract name="Ciss/Cgg" max(c."gate""gate")
extract name="Coss/Cdd" max(c."drain""drain")
extract name="Crss/Cgd" max(c."gate""drain")
extract name="gmax" max(g."drain""gate")
extract name="gm" ave(g."drain""gate")
extract name="Ft" max(g."drain""gate" / (6.28*c."gate""gate"))

solve init
solve vdrain=0.0 vgate=0.0 vsource=0.0

solve vdrain=0.1
solve vdrain=0.2
solve vdrain=0.3
solve vdrain=0.5
solve vdrain=0.7
solve vdrain=1.0 vstep=1.0 name=drain vfinal=10

solve vgate=-5.0
solve vgate=-5.3
solve vgate=-4.5
solve vgate=-4.0

log outf=dt.log
solve vstep=0.5 vfinal=4.0 name=gate ac freq=1e6
extract init infile="dt.log"
extract name="cgg" curve(v."gate" , c."gate""gate") outfile="cgg.str"
tonyplot cgg.str

extract name="cgs" curve(v."gate" , c."gate""source") outfile="cgs.str"
tonyplot cgs.str

extract name="g" max(g."drain""gate")
extract name="Ft" max(g."drain""gate" / (6.28*c."gate""gate")) outfile="Ft.str"
quit
```