TRAFFIC LIGHT CONTROL USING INDUCTIVE LOOP SENSOR

by

Nazmi Syamimi Azmi

Dissertation submitted in partial fulfilment of
the requirements for the
Bachelor of Engineering (Hons)
(Electrical and Electronics Engineering)

JUNE 2007

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CERTIFICATION OF APPROVAL

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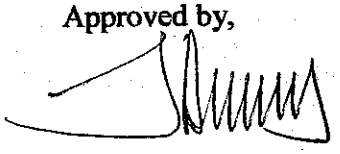
Approved by,



(Dr John Ojur Dennis)

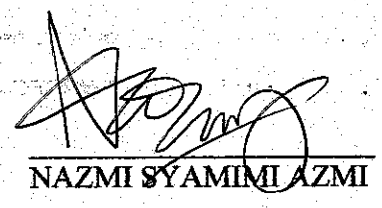
UNIVERSITI TEKNOLOGI PETRONAS

TRONOH, PERAK

June 2007

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



NAZMI SYAMIMI AZMI

ABSTRACT

The purpose of this study is to design a smart traffic light which consists of a sensor to detect the density of cars waiting along a particular lane. The main objective is to design a working traffic light system interfaces with the inductive loops sensor. The experiments and simulations are done to investigate the behavior of the inductive sensor with metal presence. From the experimental and simulations results, the best performance of inductive sensor is chose .The sequences of the light of each lane are reset according to the state of the car density. The lane with longer queue has a longer time passing than a normal queue. The implementation of the inductive sensor is to count the number of vehicles in a particular lane per unit time. The sensor will act as an input counter to the traffic light circuit. The traffic light controller will evaluate the information whether to give a long time and green light priority or a normal light sequence with a normal timing delay. The final product of this project which is a prototype is constructed to demonstrate the traffic light controller with inductive loop sensor.

ACKNOWLEDGEMENT

There are so many persons the author would like to thank upon the completion of this project. These are the people who became the light of dark highway of learning who inspire to strive harder in order to achieve success besides giving advice and support all the way. With all heart, the author would like to say a big thank you to these people.

Firstly, the author would like to thank supervisor, Dr John Ojur Dennis who has been guiding with full dedication and relentless in helping on the certain points that the author is unsure of.

The author would also to express gratitude to other lecturers who have been giving guidance and putting ideas in completing the project.

Next are of course parents and family members who have given a never-ending support in the quest to gain knowledge in this university through the completion of this project.

Certainly on the list of people to thank are friends from all around. To list down their names would be an honourable task. However, that action wills double the length of this lengthy assignment. To all friends out there especially who are the comrades on this road to a brighter future, who have lent a hand when the author needs it without hesitation, from the bottom of heart, thank you.

Last but not least, to those people that were not mentioned here, despair not; for you are not forgotten. You names may slip our minds at this moment but you actions, however small they may be, stay engraved on the author's soul forever and the author too, would like to thank you.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND STUDY

In Malaysia or any developing country, the traffic lights are crucial for busy street as a result, most of the junctions must have traffic lights to smoothen the traffic flow. With the increasing numbers of automobiles, serious action should be taken especially in the development state or industrial areas in ones country. The traffic congestion in the state capital and industrial areas are the worst. As a result, the effectiveness in reducing the traffic congestion is yet to be agued. In other to keep the traffic moving smoothly, Malaysia needs to have efficient traffic lights. Apparently, the conventional design has failed to reduce the traffic congestion. By just using counters during changing of lights is nevertheless not an efficient way to solve heavy density traffic. As a result, there is still in need of police traffic to control the traffic regardless to the traffic light.

As a solution to the above mentioned problem, a traffic light with sensor can be implemented so that the traffic is in the best management. In keeping with the scope of the Final Year Project, this traffic light should have a sensor that can detect the numbers of cars. The type of sensor which will be used is weighted by its efficiency and cost in implementing and maintaining it. An addition feature of the traffic light is the light sequences can be determined by the controller with the help of the sensor.

1.2 PROBLEM STATEMENT

Currently, Malaysia is using the basic counter traffic light to change the light sequences. However these type of traffic light are limited to the programmed sequences as they have been predetermined for the time elapsed between each light sequences. In most areas, the lane with fewer cars has the same length of time for the cars to pass through between each lane.

There are a lot of techniques to enhance the capability of the traffic light. By adding a suitable sensor that can count number of cars queuing, it can change the light sequences. As a result, the sensor can shorten the length of time for the traffic light with less cars and give way to the lane in which has more cars queuing.

Another problem is that the basic counter will just allocated certain amount of time as predetermined by the programmer. A heavy lane tends to have a long queue. The traffic light will pass a few number of cars although the lane can accommodate a few more cars. As a result there is a jam in the traffic and cars have to wait for maybe third green light before moving forward. Consequently, the lane may have a very long queue and even worse during peak hours which can affect other lanes.

1.3 OBJECTIVES

The objectives of this project are:

- To attain knowledge in depth about the traffic light controller and inductive loop sensor.
- To design and construct an intelligent traffic light.
- To design and construct an inductive loop sensor.
- To build a prototype of traffic light.

1.4 SCOPE OF STUDY

The scopes of study consist of identifying the problem, problem definition, research, specifications, decision making, simulation and modeling, evaluation, documentation and oral presentation.

Table 1 summarizes the activities that will be carried out to achieve the objectives of Final Year Project:

Table 1: The Activities

ACTIVITIES
Identifying needs • Brainstorm
Problem definition • Conduct literature research • Analyze and criticize research outcome • List shortcoming problems
Research • Collect data of existing cleaning devices • Personal observation • Consult lecturers, technicians & individuals
Specification • Traffic light circuit devices • Sensor selections • Materials used in the design
Decision making • Efficiency & practicality • Material • Features • Cost

Simulation and modeling • Design the circuitry and electrical components of the device • Construct the mechanism of the design • Design an ideal place for sensors
Evaluation of the system • Practicality & ease of use • Efficiency of electrical components • Efficiency of mechanical equipment • Cost effectiveness & reliability • Integrity and performance of the design • Overall aspects
Documentation • Project proposal • Preliminary report • Logbooks • Progress report • Draft report • Final report
Oral presentation

The plan and the flow of the process can be summarized in Figure 1.

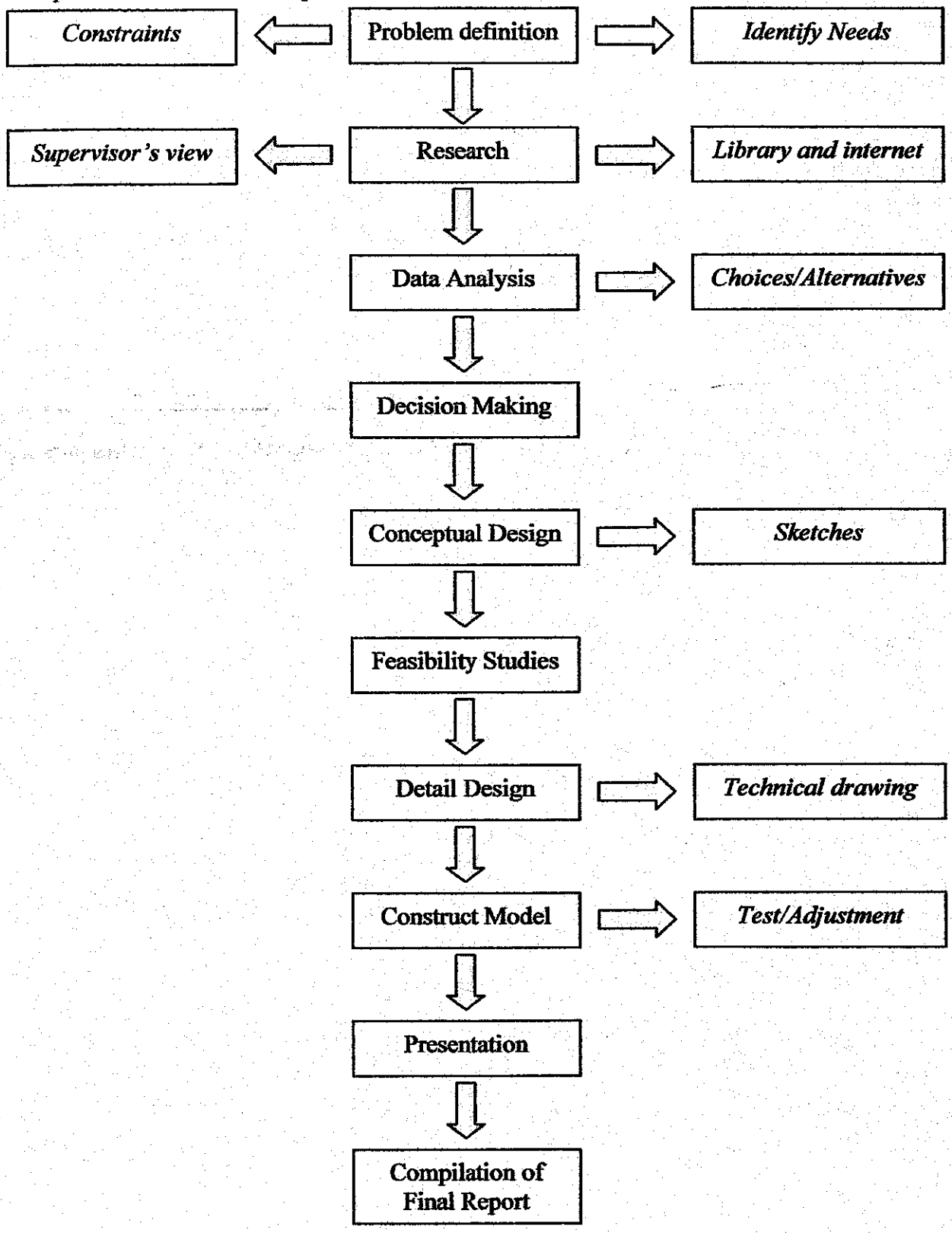


Figure 1: Flowchart of Plan and Schematic Flow Process

CHAPTER 2

BACKGROUND STUDY/LITERATURE REVIEW

2.1 TRAFFIC LIGHT

In order to model a car's movement throughout the traffic environment, time and space have been discretized. For each discrete time step, a car is located in one discrete space until the next time step in which the car may be able to move forward to next space or just stay in its current position, depending on the condition of the situations. For every traffic light, there is a queue consisting of a numbers of cars in the discrete space. Hence, every lane has its own queue. As each car attempts to move forward, the next discrete space must be empty or else the car cannot move and must stay at its current space. This process relates the cars and the traffic light. The car at the front space will remain there until the traffic light turns green and all the discrete space at the back can only be moved if the first car of the lane moves forward and empty its current space [2].

The best way to explain parts in the traffic light circuit is by using a block diagram. The traffic light as shown in Figure 2 consists of 4 block diagrams which are the sequential logic circuit, timing circuit, state decoder and the traffic circuit.

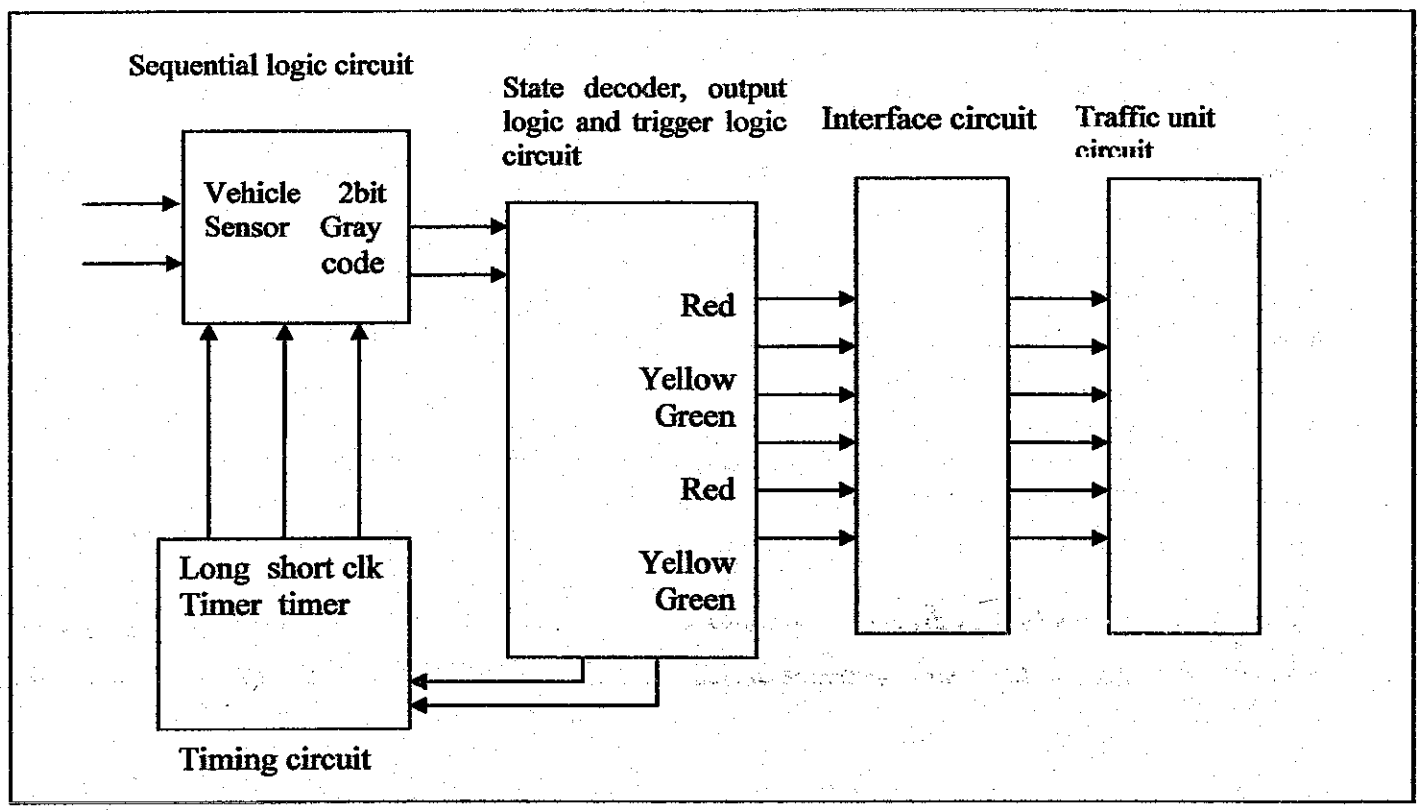


Figure 2: The Traffic Light Block Diagram

There are many reasons why the new implementations are innovated. There are varieties of designs done mostly in the urban developing country. Efficient designs are very important to accommodate and control the traffic flow. The following list stated about the current traffic lights designs:

- Traffic light with counters which use a basic counter to change the light sequences.
- Traffic light with motion sensor such as ultrasonic or infrared in which the sensor will sense the incoming cars.
- Traffic light with inductive loops as a sensor to sense the electromagnetic field created when conductive objects enters the areas.

2.1.1 Traffic Light with Counter

This type of design is a very classic and common design for traffic lights. The light sequences are based on predetermined data such as time of the day or traffic flow and other related data such as holidays or peak hours. The implementation of this type of design is simple as the systems have to be programmed according to the predetermined data and can be extended to any desired criteria depending on the survey done with a little ideas of programming, the traffic light is programmed so as to accommodate the holiday traffic pattern, peak hours traffic pattern or time in with heavy traffic pattern. The light sequences transitions are all controlled by the programmed data.

2.1.2 Traffic Light with Motion Sensors

Mostly the motion sensors are ultrasonic sensors and infrared sensors. The sensors will sense the incoming cars and send the data to microcontroller to analyze the data. The microcontroller will consider whether the cars queue is long or short. If the queue is long the microcontroller will give a longer time for that particular lane so that more cars can pass through the junction.

2.1.3 Traffic Light with Inductive Loops

An induction loop or inductive loop detector which is simply a coil of wire embedded in the road surface. The coil is used to detect conductive objects such as metal. It is applicable for cars, motorcycle and even the bicycle. The principle of operation is a changing inductance which changes the frequency of an oscillator of which the inductive loop forms a part. In order to install the inductive loop under the road surface, they lay the asphalt and cut a groove in the asphalt with a sharp object which is usually by using the wire coils are placed in the groove and sealed with a rubbery compound. As for that, the loops can be seen through naked eyes compound is obvious. Inductive loops work by detecting a change of inductance.

After conducting this research, it is best to choose a design with high efficiency and reliability to be implemented in order to replace the classic traffic lights.

2.2 SENSORS

When the sensor detects a longer queue, the timing will slightly change. A car is located in one discrete space, until the next step at a point in which the cars can move forward to the next space or stay at the point depending to the traffic light sequences. In front of each traffic light, there is a queue to represent the number of users of discrete spaces. Simply to say, each lane or street has their own queue. At each step, the user will attempt to move forward to the next empty discrete space. If there is a car already filled the space, then the car at the back cannot move and must stay at its position at the current space. It is also to the front car, the car cannot move until the other front car is moved or in this case, waiting for the traffic lights turn to green. When the traffic light is green, the car can move forward and removed from its current queue assuming there is no car ahead. It is important to make sure the movement will not lead to any blockage to the other traffic or incoming traffic. The other traffic should be moving smoothly.

The careful selection of sensors is important and essentials. Sensors are external detecting devices that represent the environmental circumstances surrounding the traffic. They are used to give feedback to the microcontroller of the length of cars.

2.2.1 Ultrasonic Sensor

In addition to that, the ultrasonic sensors are being considered to be implemented on the traffic light, to monitor the traffic. Ultrasonic sensors are cheap and easy to implement compared to above explained sensor. Ultrasonic waves travel slowly at the speed of sound, so it is possible to measure the flight time of the wave. In addition, the size is small, low weight, have a wide range detection capability and reasonable accurate.

The sensor will sense the object (automobile). The echo from the transmitter reflected from the ultrasonic wave will then be collected by the receivers. After that, the wave will be sent to the microcontroller and if the long queue is detect, the microcontroller will reset the current traffic light and give way to the longer queue.

In order to increase the accuracy of the sensor, there will be two receivers for one traffic light. As a result the scanning resolution can be increased and the operating range can be adjusted.

2.2.2 Electromagnetic Sensor

Electromagnetic sensors are the sensors that capable of detecting the changes in the electromagnetic field caused by moving metal. This type of sensor does not consider the vehicle's weight. It reacts to only the presence of metal for every vehicle has a body of metal. When a ferromagnetic metal is introduced to the balance of the circuit, the circuit reacts. As a result, an inductance change will also affect in current and voltage that will trigger a relay to switch the lights. These sensors detect large masses of metal, and a touring bike surely qualifies.
In each traffic light, a sensor is implemented that can detect the queue of each lane. This type of the sensor is capable of counting the number of discrete time steps the car has been located in this position. For each car coming and fill the empty discrete space, the sensor's counter is incremented by one [7].

Electromagnetic sensors are often known as inductive loops sensors. These kinds of sensors are one of the examples of demand actuated traffic signals. These sensors sense the flow of the traffic before changing the state transitions in order to control as a result, optimize the traffic flow.

An inductive sensor works when a conductive object which is any type of objects made of metal such as cars, bicycle and motorcycle enters the area over the inductive loops, the magnetic field generated by the alternating electric current in the signal detector circuit

induces weak electrical currents in the conductive object. This change in resonant frequency in which an increase in frequency as the inductance decreases is detected by the circuit instrumentation in the signal controller which the signal will control circuit that a vehicle is present [2].

The advantages of using the inductive loop detectors are that they are an established technology nowadays and they have a well defined zone of detection, and they are generally reliable.

- Inductive loops detector applicable in all weather.
- It is the most consistently accurate detector in terms of vehicle detection.
- The inductive loops best performs both high and low traffic density.
- Inductive loop detectors have the lowest flow error specifications according to most experiments done.

The construction of inductor is done by using a coil of conducting material in which the copper wire is wrapped around a core or any ferromagnetic material or simply in the air space. Core materials with a higher permeability than air confine the magnetic field closely to the inductor, thereby increasing the inductance. As a result, the strength of inductance is increased by using a high permeability material.

Inductors come in many shapes. Most are constructed as enamel coated wire wrapped around a ferrite bobbin with wire exposed on the outside, while some enclose the wire completely in ferrite and are called shield. Adjustable core can be used to enable the changing of the inductance. Inductors used to block very high frequencies are sometimes made with a wire passing through a ferrite cylinder or bead [3].

Therefore another type of inductive loop known as quadrupole loop is introduced to enhance the sensing capability of small object detection with limited metal for an example bike and bicycle. The sensitivity of an inductive sensor depends on certain variables. The sensitivity is affected by [2]:

- The size, shape, and conductivity of the object

- The 3-D orientation of the object with respect to the wires in the loop
- The 3-D position of the object over the loop
- The size and shape of the sensor loop
- The nominal operating frequency of the circuit

Figure 3 shows the basic construction of inductive loop:

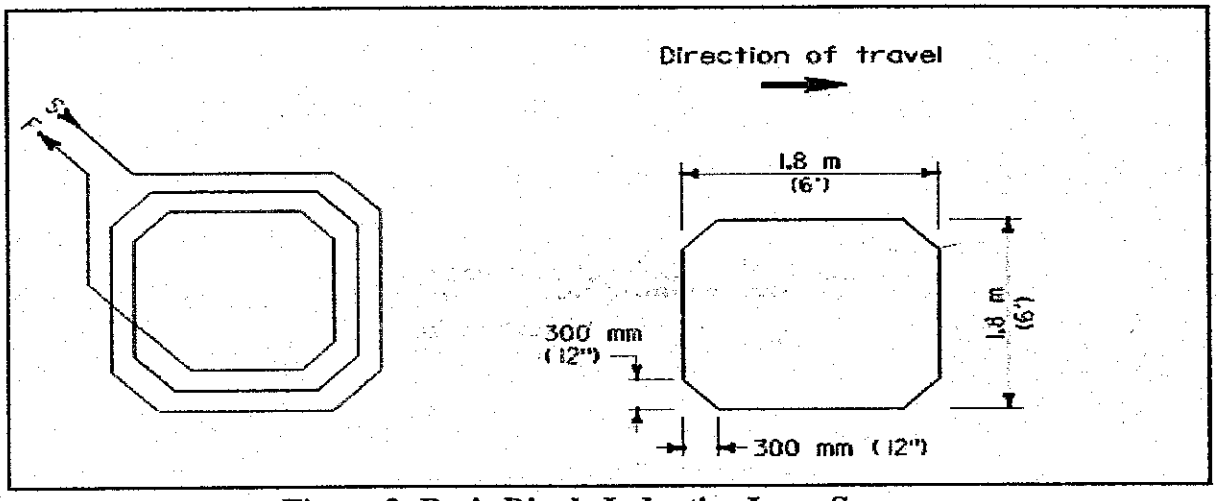


Figure 3: Basic Dipole Inductive Loop Sensor.

Figure 4 shows the types of inductive loop designs in the market.

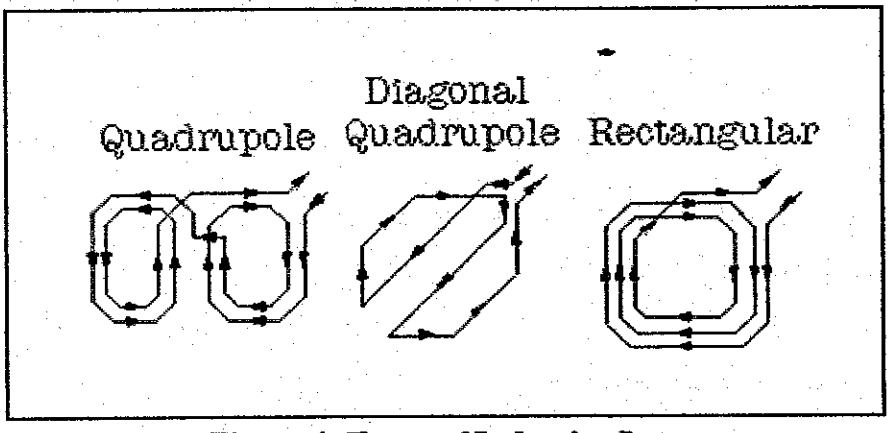


Figure 4: Types of Inductive Loops

The reason why this type of sensor is selected to be integrated with the traffic light controller is because it has the capability of detecting from the largest vehicles to the smallest vehicles such as bicycle. The sensor is applicable to all sorts of vehicles as long as they have metals on their bodies. As a result, it covers a very efficient detection. Apart

from that, as it senses the presence of metals, the flow error specifications are also can be reduced. Conventional sensor such as motion or ultrasonic sensors, the flow error rates are high. Ambient environment and rain can affect the consistency of the sensor. This is due to the sensor behavior which sense any object that is stood between the sensing regions is considered as obstacles thus provide fake information. As a result, sometimes rain can be mistakenly being presented as an obstacle.

CHAPTER 3

METHODOLOGY/ PROJECT WORK

In completing this project, some methodology had been conducted. The project scope of work includes laboratory experiments, computer programming, simulations, and prototype design.

3.1 PROCEDURE IDENTIFICATION

3.1.1 Defining the Project

This part involves the planning of a specific outline of the proposed work, requirements and deliverables of the project. It is important to plan all the procedure in order to ensure this project is complete within the allocated time frame. All basic requirements, background study, problem statements, clear objectives and scope of project have to be identified and clearly defined.

3.1.2 Literature Research

Literature research is done to have a basic idea of the project. The research has been done for both parts which are the traffic light design and the inductive sensor design. The purpose of the literature research is to gather information related to the topic and use some basic ideal of circuit construction as references.

3.1.3 Design Selections

After conducting research, the best design is chose. The design must meet all the requirement of the realistic traffic light. In order to do so, the intensive researches are done only to the specific areas.

3.1.4 Simulations and Experimentation

After all the selections being done, the constructions of the circuit will be carried and the simulations are done to verify a working circuit. The experiment for each part is crucial to determine the most effective design of both traffic light and inductive loop sensor is constructed. The circuits have been simulated by using Multisim and Pspice.

3.1.5 Modeling

At the end of the process, the modeling will be done. A prototype is constructed to demonstrate a working model of the project.

3.2 TOOLS REQUIRED

The simulation tools are used to simulate the project is:

- Electronics Workbench Multisim
- Pspice Student Edition

CHAPTER 4

RESULTS AND FINDINGS

4.1 TRAFFIC LIGHT CIRCUIT

The traffic light is designed to change the light when any perturbation occurs at the inductive loop sensor. The sensor will act as a counter to the traffic light and the controller circuit of the traffic light will determine which of the lane to be give priority to cross the junction. The traffic light will consider ten cars queuing as a long queue. As a result, the light sequence will change in which the particular lane with most cars will be given a green light and a longer time to pass by. The model consists of 4-junction road with one traffic light to control the forward journey while another one is to control the right turn junction for both opposite lane. As for that, there are six traffic light output for each lane.

4.1.1 Timer Design

Each traffic light uses six LEDs as outputs. They represent two opposite lanes. The time for each sequence is controlled by varying the R2 value. The time taken for the complete cycle of red-green-yellow-red can be varied from about 7s to about 2½ minutes by adjusting the R2. Therefore, the R2 is changed from standard resistor to 1M potentiometer.

In this project, the timer is connected as an astable multivibrator . The basic astable timer circuit is shown in Figure 5. An astable multivibrator uses two resistors, one capacitor and a 555 timer. An astable timer produces a square wave. The external components (R1, R2 and C1) from the timing network determine the frequency of the oscillation. The capacitor, C2 which is 0.01μF is connected to the control input is for decoupling purpose

and has no effect on the operation. The capacitor C2 can be neglect as it has no significant use.

The square wave is representing the digital waveform transitions between low (0V) and high (+Vs). The duration of low and high states may differ according to the values of R1 and R2. The circuit is called an astable because it is not stable in any state which means the output is continually changing between low and high.

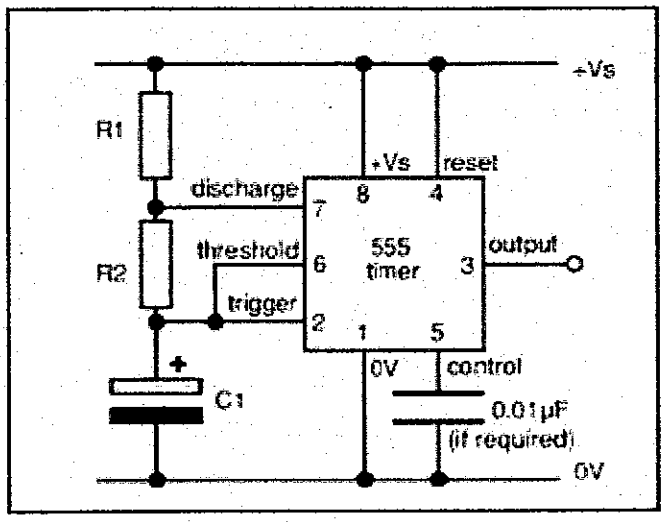


Figure 5: Basic Astable Timer

From the circuit, we can determine the time period, frequency, mark time and space time. This variable can be predetermined by the external components. Therefore, all values have been predetermined to satisfy the timer design. The external components are listed in Table 2.

Table 2: The component used in the astable timer.

Components	Value	Quantity
Resistor 1 (R1)	100 K Ω	1
Resistor 2 (R2)	1 MΩ	1

Capacitor 1 (C1)	10 μF	1

Two timers are being designed for this controller. They are for short and long timer. The short timer will be used as a normal timer or the short queue and the long timer is used for long queue. The short timer will count for seven seconds for each cycle of light sequence while the long timer will count for 14 seconds for each cycle of light sequence.

The time period, T can be determined by using the formula of:

$$T = 0.7 \times (R1 + R2)C1 \quad (1)$$

Where as the R1= 100 KΩ, R2 = 1 MΩ and C1=10 μF. Using the Equation 1 and substituting all the values, the time period, T of the timer equals to 14.700 seconds.

The frequency of oscillation is given by the following formula:

$$f = \frac{1.44}{(R1 + 2R2)C1} \quad (2)$$

After subsituting all the values, the frequancy of the timer is 0.0680 Hz

The time period can be split into two parts which are Mark Time (Tm) and Space Time (Ts). Time period is the summation of both Mark Time and Space Time. Mark Time is the period when the output is on the high state while the Space Time is the period of time when the low state occurs.

The calculations for Mark Time, Tm and Space Time, Ts are as below:

$$T = Tm + Ts \quad (3)$$

Mark time is a computation of R1, R2 and C1. As shown in the Equation 3, the mark time depends on R1, R2 and C1. Any changes to these variables will result in mark time.

$$MarkTime, Tm = 0.7 \times (R1 + R2)C1 \quad (4)$$

In Equation 4, the addition of R1 and R2 is equal to 1.1 M Ω. By timing it to the value of C1 which is 10 μF, and constant 0.7, the mark time, Tm is 7.0273 seconds.

Where as the space time, Ts is a computation of R2 and C1. It depends on the value of R2 and C1.

$$SpaceTime, Ts = 0.7 \times R2 \times C1 \quad (5)$$

Inserting the values of R2 and C1 as listed in the Table2, the space time, Ts is equal to 7.000 seconds.

From the calculation, Tm and Ts are almost equal. This is because in a standard astable circuit, Tm cannot be less than Ts. It can be verified as Tm is 0.2373 seconds higher than Ts. As a result, R2 value is higher than R1 so that the condition can be met. However, the condition is not too restricting as the output can both sink and source the current.

Duty cycle is the ratio of the pulse width to the period and it is usually being expressed as a percentage. By selecting R1 and R1, the duty cycle of the system can be adjusted. In an astable multivibrator, the C1 charges through both R1 and R2 but discharges only through R2. The duty cycle approaches at a minimum of 50% can be achieved if the selected R2 is more than R1 so that the charging and discharging time are approximately equal. For a standard 555 astable circuit the mark time (Tm) must be greater than the space time (Ts), so the duty cycle must be at least 50%. Duty cycle, D can be determine by using Equation 6.

$$DutyCycle = \frac{Tm}{Tm + Ts} \times 100\% \quad (6)$$

Or it also can be computed by using Equation 7. Equation (7) makes use the values of R1 and R2.

$$DutyCycle = \frac{R1 + R2}{R1 + 2R2} \times 100\% \quad (7)$$

As the duty cycle often expressed in the percentage, the multiplication of 100% is done to get the final answer. Both Equation 6 and Equation 7 will produce approximately the same value which is 50.0873%.

The calculations of time period, frequency, mark time, space time and duty cycle can also be verified by using computer calculator as shown in Figure 11 [9]. The values of R1, R2 and C1 need to be inserted and the calculator will do the calculation for all variables.

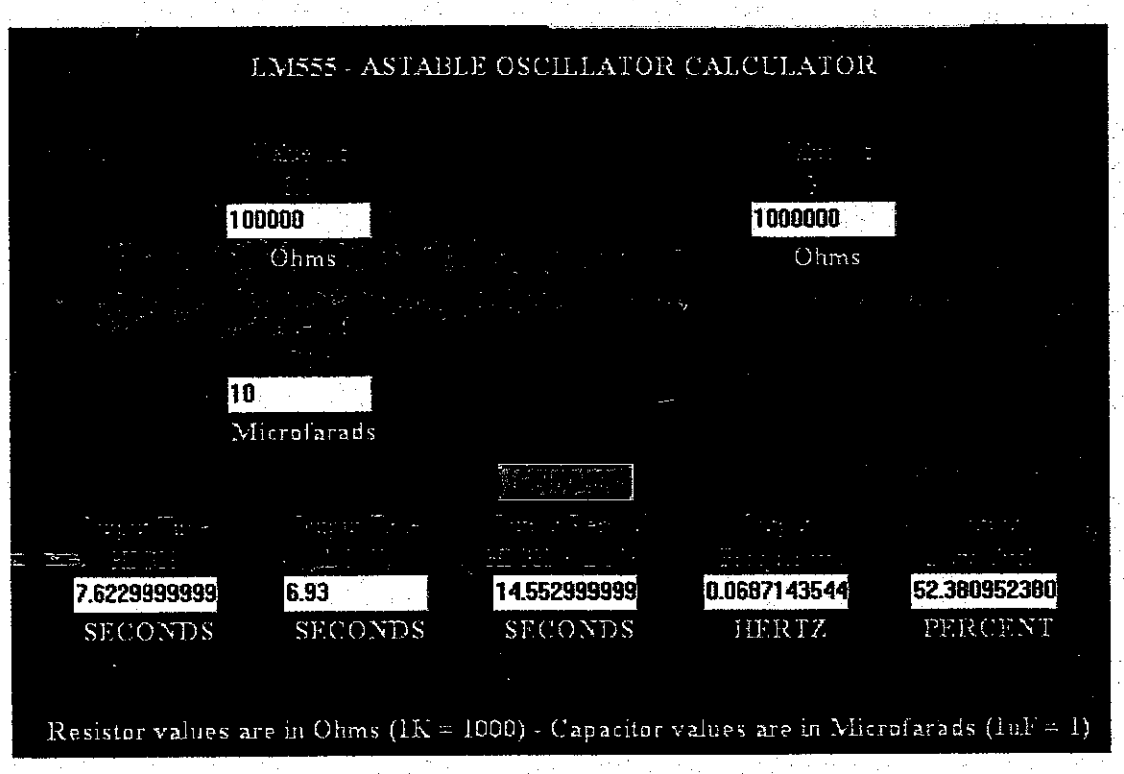


Figure 6: Astable Oscillator Calculator

Table 3 shows the comparison of both methods of calculations between manual calculation and computer calculation.

Table 3: Comparison of calculations

VARIABLES	MANUAL	COMPUTER
Mark Time (Tm)	7.0273 seconds	7.6230 seconds
Space Time (Ts)	7.0000 seconds	6.9300 seconds
Time Period (T)	14.7000 seconds	14.5530 seconds
Frequency (f)	0.0680 seconds	0.0687 seconds
Duty cycle (D)	50.0973%	52.3810%

4.1.2 Light Sequence Circuit Design

The traffic light will produce six outputs of LEDs represent a two way lane. The circuit is designed to meet the requirement of the overall system in order to be connected to the sensor. Figure 7 shows the schematics diagram of the light sequence.

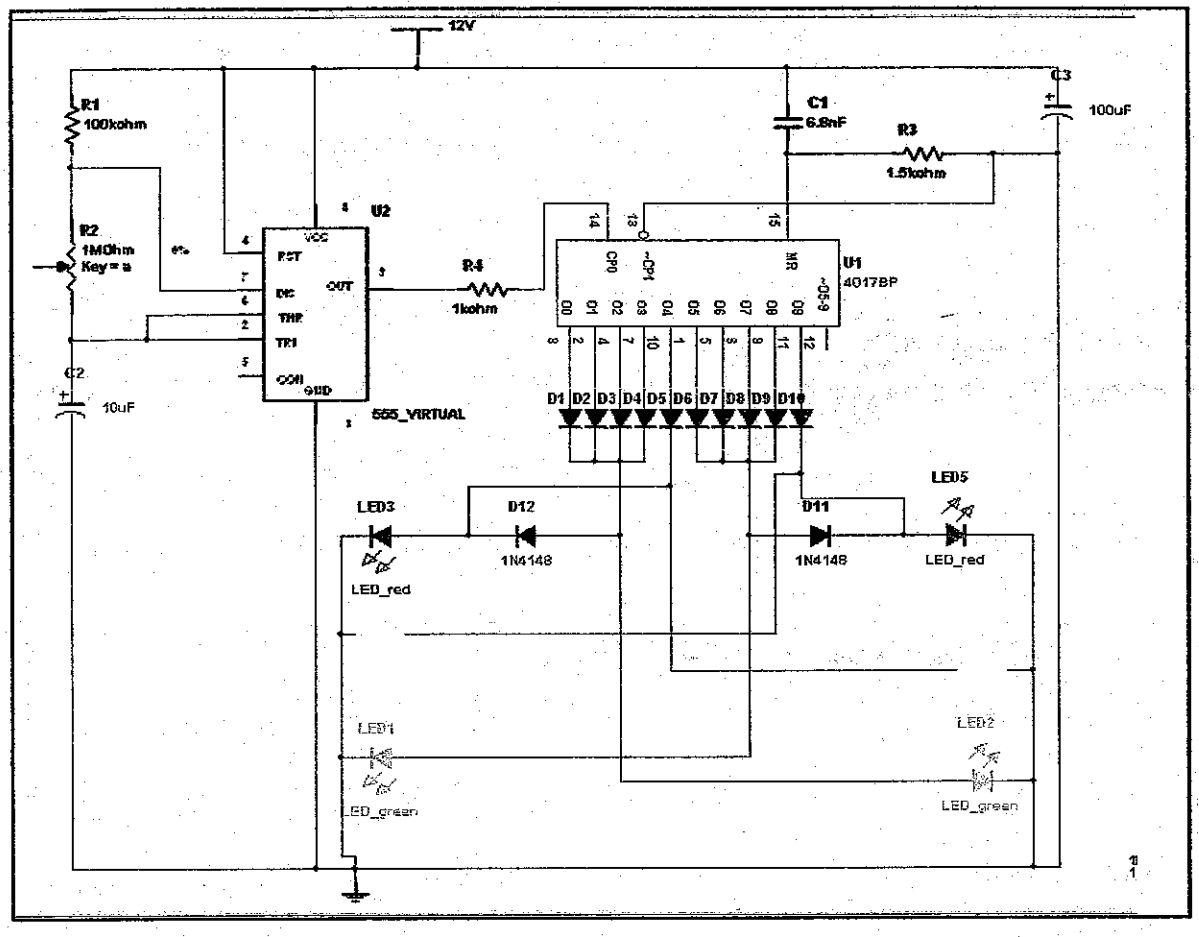


Figure 7: Schematics Diagram of Light Sequence for Traffic Light Design

The timer circuit has been connected to the light sequence circuit in order to provide a timing input to IC 4017. Table 4 lists the components used in the circuit diagram.

Table 4: The components used for traffic light circuit:

COMPONENTS	VALUE	QUANTITY
IC 4017	-	1
Timer set	From Part 1	1
Resistor	1 KΩ	1
Resistor	1.5 KΩ	1
Capacitor (electrolytic)	100 μF	1
Capacitor (ceramic)	6.8 nF	1
Diode IN4148	-	12
Red LED	-	2
Yellow LED	-	2
Green LED	-	2

4017 is a CMOS counter with ten output terminals or also known as 5-stage Johnson Counter. The 4017 decade counter has ten outputs which go HIGH in sequence. One of these ten terminals will be in a high state at any given time, with all others being low, giving a one-of-ten output sequence. If low-to-high voltage pulses are applied to the clock (Clk) terminal of the 4017 decade counter, it will increment its count, forcing the next output into a high state.

The decade counter will cycle its 10 count sequences lighting up six LEDs at one time and return to the first LED. Two terminals on the 4017 chip, Reset and Clock Enable, are maintained in a low state so that the decade counter to count freely and continuously. If the Reset terminal is made high, the output will be reset back to 0. Therefore, if the output timer (pin 3) is high, all the output pins is low. If the Clock Enable is high, the chip will stop responding to the clock signal and pause in its counting sequence. As a result the LEDs will stop lighting up and paused. As a result it is important for Reset and Clock to be maintained at low state.

The circuit operates by 555 as an astable multivibrator in a low frequency which is 0.068 Hz provides clock pulse for the 4017 decade counter. The decade counter produces ten outputs from Q0 to Q9. Every high clock pulse, the outputs will be also high. As a result, the connected LEDs are also turned up. Appropriate outputs are combined with diodes to supply the red, yellow and green LEDs. The red LED is connected to the ÷10 output which is high for the first 4 counts (Q0-Q4 high). By this, it will simplify the circuit by less diode is saved to connect to the red LEDs.

Each light sequence is designed to light for seven seconds for short queue. As for that, each pin of the 4017 will be HIGH for seven seconds. For the red and the green LEDs are connected to four pins of the 4017 will result in adding time to the sequences. As a result the red and green LEDs will light for 28 second and the yellow will only light for 7 seconds as only one pin is connected to it. The turning right junction will be delayed one cycle from the forward journey for both lane. As for that, the green light for turning right junction will only light for 21 seconds. However for long queue, each sequence will light for 14 seconds. Thus, The green and red light will light for 56 seconds and the yellow light will on for 14 seconds. The operations of the traffic light are summarized in Table 5.

Table 5: The LEDs Operations of the Traffic Light

O/P	FORWARD A			TURN RIGHT B			FORWARD B			TURN RIGHT B		
Q0	●			●				○				
Q1	●			●				○			○	
Q2	●			●				○			○	
Q3	●			●				○			○	
Q4	●			●					○			○
Q5		○					●					●
Q6		○			○		●					●
Q7		○			○		●					●
Q8		○			○		●					●
Q9			○			○	●					●

The time sequences of each light are adjusted by using the potentiometer and the diode. Diodes are used to light the LEDs from according to the clock input. It is also being used to draw enough current to light the LEDs.

4.2 INDUCTIVE LOOP SENSOR DESIGN

The designs of the inductive sensor can be divided into three parts which are the timer design, resonant circuit designs and sensor design. The timer acts as an input to the sensor circuits and the sensor design will experiment on the most efficient sensing capabilities of the inductive loop.

4.2.1 Resonant Circuit Design

In order to have a high efficiency of detection, a special circuit need to be design so that it can collect the smallest change of inductance. A resonant circuit is sensitive to a small driving perturbation thus rise a large effect to the overall system. The resonant circuit shows the best performance of detecting the inductance change. The resonance phenomena only happen when the inductive and the capacitive reactance are equal. The resonant circuit must be driven by an AC power supply in order the resonance to occur. A series resonant circuit is selected to be connected to the sensor circuit. A series resonant circuit has a resistor, an inductor and a capacitor that are connected in series.

When a ferromagnetic metal is introduced into the circuit, the frequency of the overall system is increased that will result in the increment of inductive reactance and the decrement of capacitive reactance. We can say that the inductive reactance is directly proportional to the frequency change while the capacitive reactance is reversely proportional to the frequency change.

The frequency at which the resonance occurs or the resonant frequency, Fr is determine by using Equation 8

$$Fr = \frac{1}{2\pi\sqrt{LC}} \quad (8)$$

For inductance is chosen to be 90 μH and the capacitance is 100 μF. Calculating by the given formula will give the resonant frequency of 16, 776.40 Hz. The range of best resonant frequency is from 10-20 KHz. As a result, this design is acceptable.

4.2.2 Timer Design

In inductive sensor circuit, an astable multivibrator is also being used. It functions to provide an AC supply to the resonant circuit. A resonant circuit must have an AC supply as an input so that the resonant phenomena to take place. As a result, an astable timer converts the DC supply from the power supply into the AC supply. The result from the resonant circuit design is used in designing the timer. The frequency of the power supply must equal to the resonant frequency in order for the resonance phenomena to occur. Therefore, a time with 16, 776 Hz need to be implemented.

From Equation (2), the value for resistors R1, R2 and capacitor C1 of the timer can be computed as the frequency is already being determined. The capacitor C1 is chosen to be 0.1 μF. Solving the equation, the value for resistor R1 is 400Ω and the resistor of R2 is 230 Ω.

The calculations of time period, frequency, mark time, space time and duty cycle can also be verified by using computer calculator as shown in Figure 8 [9]. The values of R1, R2 and C1 need to be inserted and the calculator will do the calculation for all variables.

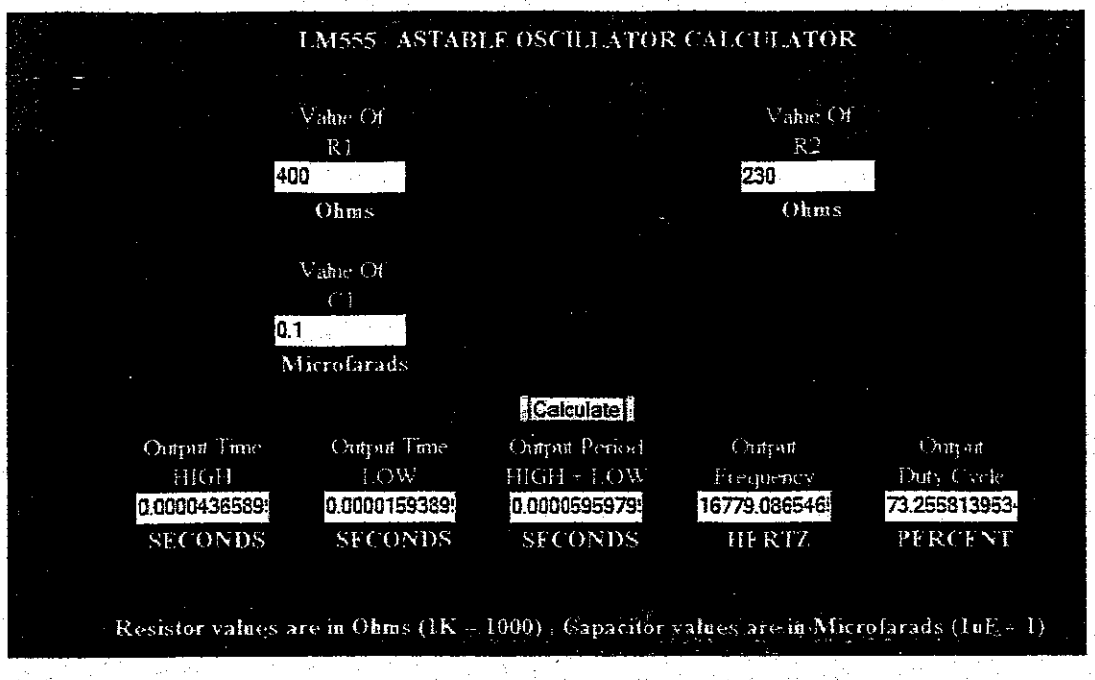


Figure 8: Astable Oscillator Calculator

Table 6 summarizes the calculation of the Astable Calculator

Table 6: Astable Calculator Results

Variables	Results
Mark Time (Tm)	0.0000436589 seconds
Space Time (Ts)	0.0000159389 seconds
Time Period (T)	0.0000595979 seconds
Frequency (f)	16779.086546 Hz
Duty cycle (D)	73.255813953%

4.2.3 Inductive Loop Sensor Design

The construction of inductor is simple. By using a coil of conducting material, an inductor is constructed. Basically, the copper wire is wrapped around a core or any ferromagnetic material or simply in the air space. Core materials with a higher permeability than air confine the magnetic field closely to the inductor, thereby increasing the inductance. As a result, we can say the strength of inductance is increased by using a high permeability material.

The electromotive force (EMF) which is produced around a closed path is directly proportional to the rate of change of the magnetic flux through any surface bounded by that path. As for this, it means that an electrical current will be induced in any closed circuit when the magnetic flux through a surface bounded by the conductor changes. This applies to the field itself changes in strength or the conductor is moved through it.

Magnetic fields are created only when the electric current flows. If the current is stronger, the magnetic field produced is also stronger. The field is directly proportional to the current strength.

The inductive sensor has been designed to be quite sensitive to pick up the small changes of the inductance drop or increase. In implementing a sensitive inductive sensor, different type and shape of inductive loop is experimented. Due to this, two types of inductive loops are experimented which are solenoid coil and quadrupole loop solenoid to determine the sensing capability.

The base frequency of the system is 10.15 KHz. After connecting it to the resonant circuit, the frequency is increased to 10.49 KHz. In this experiment, we are interested in the behavior current across the resistor (R3) in respect to the iron core introduced. Due to the nature of noise, the current across R3 is not stable. It spikes up and down makes it hard to collect a correct measurement. An improvement is made by connecting a resistor (R4) in parallel with the inductor. A multimeter is connected in parallel to the resistor R4 to measure the passing current. The behavior of each inductive loop is studied and

computed in Table 7, Table 8 and Table 9. A three sets of reading is taken for each experiment to check the consistency and accuracy of the current.

4.2.3.1 Solenoid Core 1

Base Frequency: 10.15 KHz.

System Frequency: 10.49 KHz

Number of windings: 150 windings

Diameter of the windings: 25 mm

Inductor value: 90μH

Table 7: Experimental Result Using a Solenoid Coil

Current without iron bar (mA)	Current with iron bar (mA)
0.830	0.962
0.837	0.947
0.856	0.977

4.2.3.2 Solenoid Core 2

Base Frequency: 10.15 KHz.

System Frequency: 10.49 KHz

Number of windings: 300 windings

Diameter of the windings: 25 mm

Inductor value: 330μH

Table 8: Experimental Result Using a Solenoid Coil

Current without iron bar (mA)	Current with iron bar (mA)
0.924	1.058
0.924	1.058
0.924	1.066

4.2.3.3 Quadrupole Loop

Base Frequency: 10.15 KHz.

System Frequency: 10.49 KHz

Number of windings: 100 windings

Diameter of the windings: 56 mm

Inductor value: 35μH

Table 9: Experimental Result Using a Quadrupole Loop

Current without iron bar (mA)	Current with iron bar (mA)
1.647	3.973
1.648	3.059
1.648	3.293

From the experimental results, the quadrupole loop the most sensitivity towards any perturbation of inductance change in the systems. Therefore, this type of inductive loop is selected and implemented into the sensor circuit. The complete circuit of the sensor

circuit is shown is Figure 9. The quadrupole loop replaces the normal inductor in the resonant circuit.

The timer circuit, the resonant circuit and the quadrupole is combined and a inductive sensor is designed.

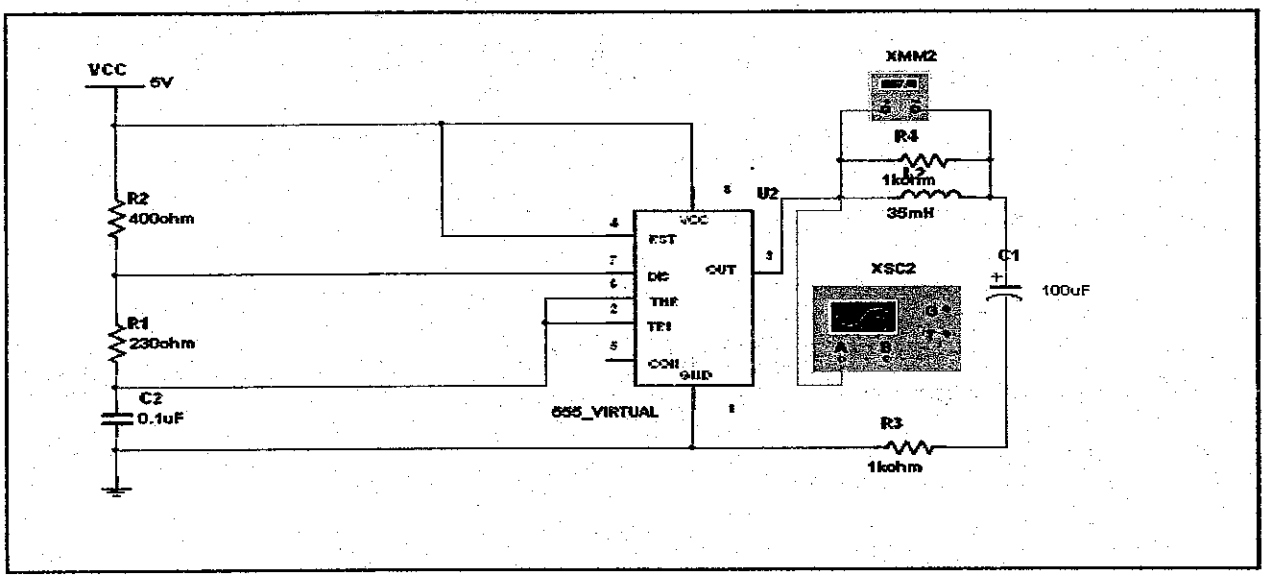


Figure 9 : The Schematics Diagram of the Inductive Loop Sensor

Table 10 shows the components used in the sensor circuit as shown in Figure 17.

Table 10: Components Used for Sensor Circuit

COMPONENT	VALUE	QUANTITY
Resistor	400 Ω	1
Resistor	230Ω	1
Resistor	1 KΩ	2
Capacitor	0.1μF	1
Capacitor	100μF	1
555 Timer	-	1

The sensor circuit acts as a counter to the traffic light circuit. The sensor counts the number of car passing by. A long queue is determined if more than ten cars pass by the

sensor. This means the sensor sense a inductance change for ten or more times and input the information to the traffic light. The traffic light acts by giving priority of green light for a longer queue and gives a longer green light so that the cars can passed by. A short queue is less than ten cars. The traffic light controller will give the normal light sequence of the traffic light. For a better detection and counting efficiency, two quadrupole loops are planted in asphalt. One quadrupole will be place 1 meter from the traffic light and another one will be 12 meters from the traffic light. The range of 12 meters is chosen for second displacement so that the sensor can sense up to ten cars or it will never be able to sense the correct numbers of car queue

CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

5.1 CONCLUSIONS

The objective of the project is to design a traffic light system that is equipped with inductive loop sensor. The project has been completed within the time frame. The proposed modifications are provided in the recommendations section.

This traffic light system has special features where it can to sense the length of cars queuing, provide the data to the traffic light controller and reset the timing of light sequences. It is also environmentally friendly because it will not interfere with any type of environment system.

The experiments are done to investigate the behavior of the inductive loop when an iron core is introduced to the circuit. Based on the experimental result, the quadrupole loop type of inductor is chosen to be implemented in sensor circuit as it shows the best sensitivity among others. The resonant circuit is used to enhance the capability of the iron detection. As a result, the inductive sensor is well designed.

The traffic light has six LEDs to represent a two way lane. By using an astable timer, a timing for each light sequence is determined. The inductive sensor will detect and count number of cars passing by and input to the traffic light controller. The controller will evaluate the information whether to give a long time and green light priority or a normal light sequence with a normal timing delay.

A prototype of the traffic light and the inductive sensor are built to demonstrate the overall performance of this project.

5.2 RECOMMENDATIONS

In order to have a better traffic light design in the future, some features can be improved by adjusting and adding new application to the existing module. These are the recommendations that we can apply in order to improve the performance of the smart traffic lights.

The future traffic light design may have a more powerful microcontroller to control bigger areas. It can be expanded to larger and complex areas such as in the big city and control heavier traffic.

Printed Circuit Board (PCB) fabrication can ease the troubleshooting and secure the connections. The circuit also ma look neat and arranged rather than use the breadboard implementations.

Apart from that, these traffic lights can be equipped with cameras to capture the road criminals and directly provide those kinds of information straight away to the police station. More over in the future, the traffic light can be equipped with emergency camera. The emergency camera will act as the eyes for ambulance. Apart from capture road criminals, the cameras can capture any accident happens and straight away inform the nearest hospitals.

The sensor sensitivity that will be used by the traffic light design must take into consideration. The maximum detection must be determined in order to avoid it sensing object in the short distance range or stretch beyond determined limits. The efficiency of the sensor also affects the performance of the traffic light. Suitable sensitivity of sensor with optimum performance must be chose and applied to the traffic light design.

CHAPTER 6

REFERENCES

[1] Steven G. Goodridge, Detection of Bicycle by Quadrupole Loops at Demand – Actuated Traffic Light Signal, 2003.

[2]Proulx, V.K., Traffic Light: A Pedagogical Exploration Through A Design Space, 1998.

[3] Wikipedia The Free Encyclopedia, Electromagnetic Induction, http://en.wikipedia.org/wiki/Electromagnetic_induction.

[4] Bill Bowden, LED Traffic Lights, http://ourworld.compuserve.com/homepages/Bill_Bowden/page10.htm#traffic.gif

[5] Detector, Indicator & Sensor Circuits, Electromagnetic Field Sensor, http://www.mitedu.freeserve.co.uk/Circuits/Misc/emf.htm

[6] Wentworth, Fundamentals of Electromagnetics with Engineering Applications, John Wiley & Sons, Inc., First Edition, 2005, pp 145-155.

[7] C. Gieseler, B. Graves, P. Maher, A Multi-Agent Intelligent Traffic Light System, 2002

[8] DIGITAL FUNDAMENTAL, Prentice Hall, 8th Edition, Thomas L. Floyd, 2003.

[9] LM 555 –ASTABLE OSCILLATOR CALCULATOR, http://home.cogeco.ca/~rpaisley4/LM555.html#3

[10] Traffic Light Project,
http://www.kpsec.freeuk.com/projects/trafficlight.htm

[11] HOW ELECTROMAGNETS WORK
http://science.howstuffworks.com/electromagnet1.htm

APPENDICES

July 2006

National Semiconductor

LM555 Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

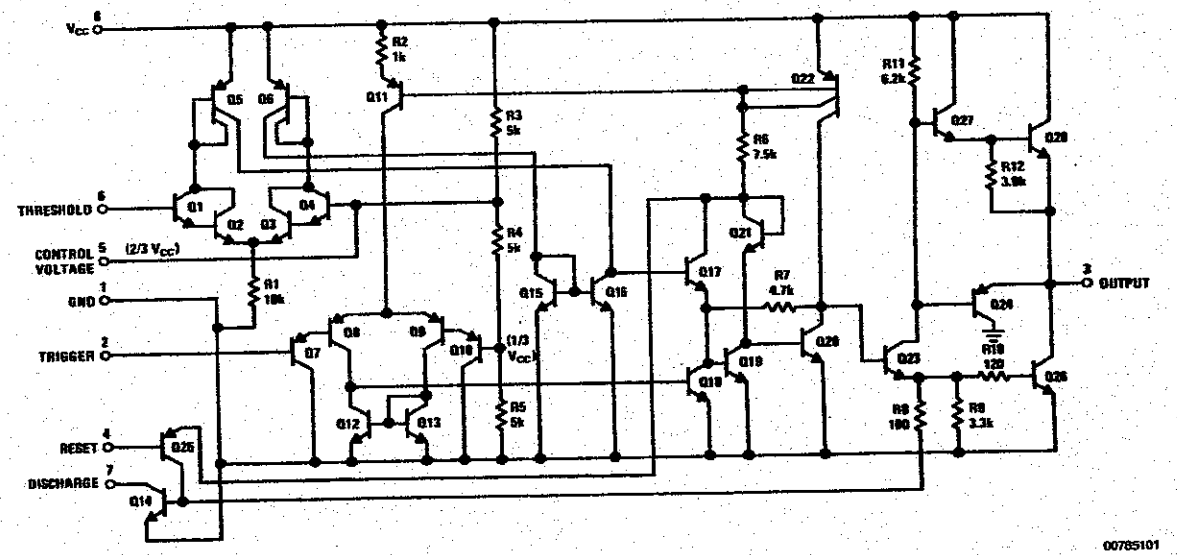
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

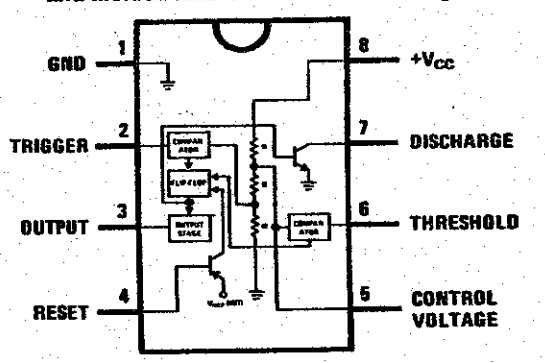
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagram

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages



Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)

f Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits LM555C			Units
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 4)		10	15	mA
Timing Error, Monostable					
Initial Accuracy			1		%
Drift with Temperature	R_A = 1k to 100kΩ, C = 0.1µF, (Note 5)		50		ppm/°C
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100kΩ, C = 0.1µF, (Note 5)		150		ppm/°C
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V		5		V
	V_{CC} = 5V		1.67		V
Trigger Current			0.5	0.9	µA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9	10	11	V
	V_{CC} = 5V	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	V_{CC} = 15V, I_7 = 15mA		180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA				V
	I_{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 106°C/W (DIP), 170°C/W (S0-8), and 204°C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

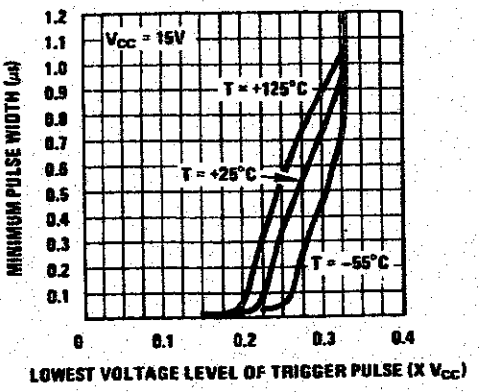
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Typical Performance Characteristics

Minimuim Pulse Width Required for Triggering



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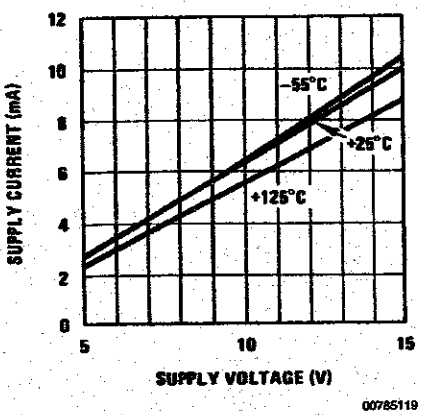
Supply Current vs. Supply Voltage



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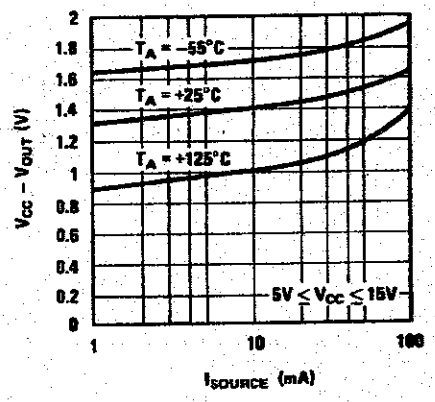
High Output Voltage vs. Output Source Current



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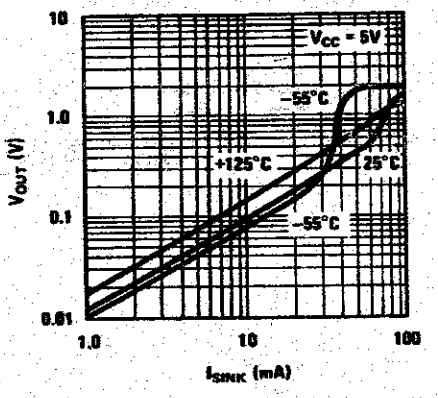
Low Output Voltage vs. Output Sink Current



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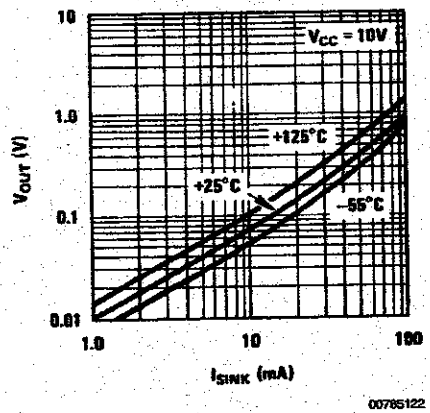
Low Output Voltage vs. Output Sink Current



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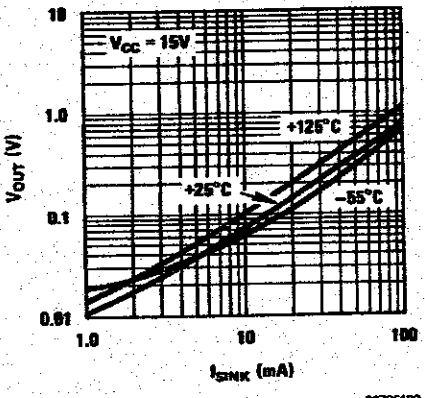
Low Output Voltage vs. Output Sink Current



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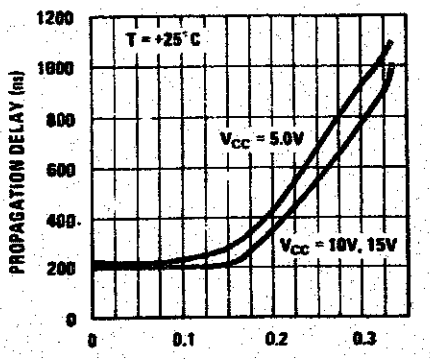
Typical Performance Characteristics (Continued)

Output Propagation Delay vs. Voltage Level of Trigger Pulse



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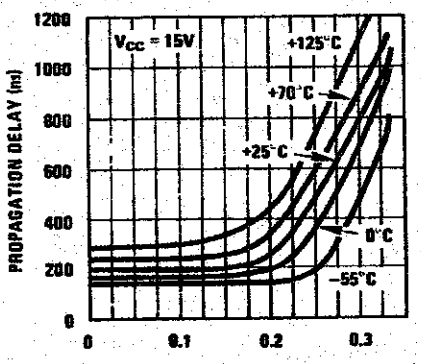
Output Propagation Delay vs. Voltage Level of Trigger Pulse



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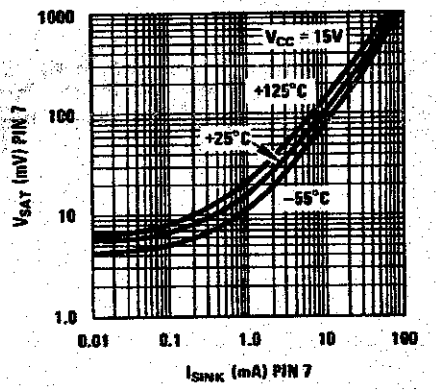
Discharge Transistor (Pin 7) Voltage vs. Sink Current



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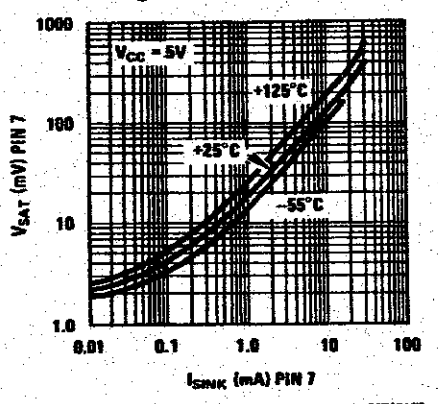
Discharge Transistor (Pin 7) Voltage vs. Sink Current



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Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

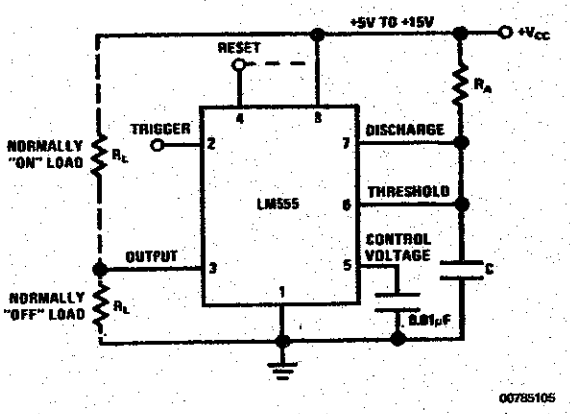
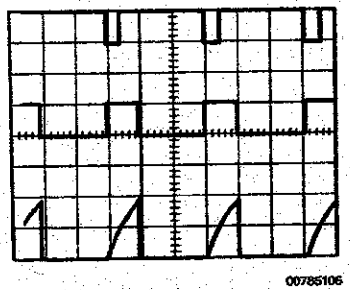


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A\ C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



V_{CC} = 5V — Top Trace: Input 5V/Div.
TIME = 0.1 ms/DIV. — Middle Trace: Output 5V/Div.
R_A = 9.1kΩ — Bottom Trace: Capacitor Voltage 2V/Div.
C = 0.01µF

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

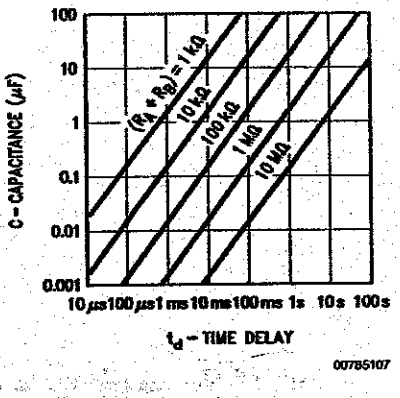


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

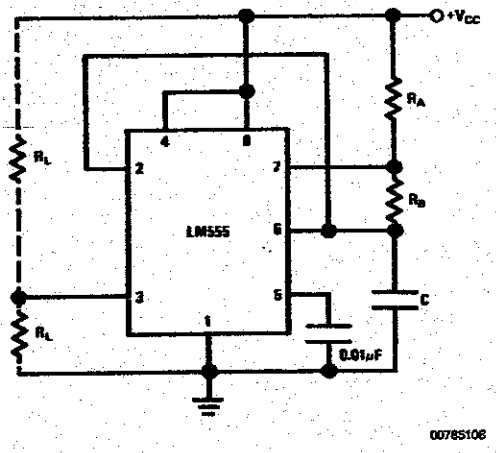
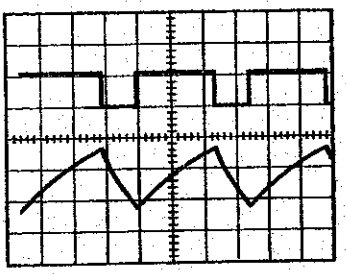


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



00785109

V_{CC} = 5V
TIME = 20µs/DIV.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

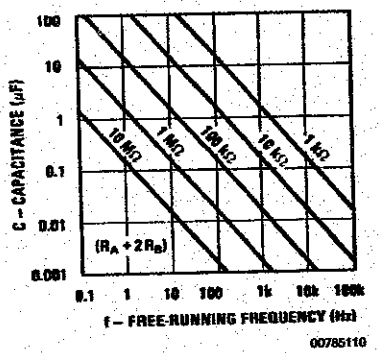
The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\,C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

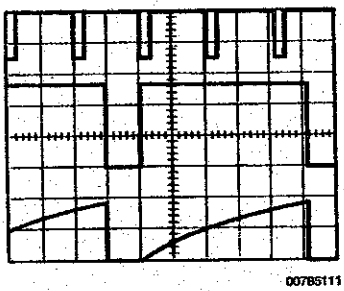


00785110

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



00785111

V_{CC} = 5V
TIME = 20µs/DIV.
R_A = 9.1kΩ
C = 0.01µF

Top Trace: Input 4V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capacitor 2V/Div.

FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

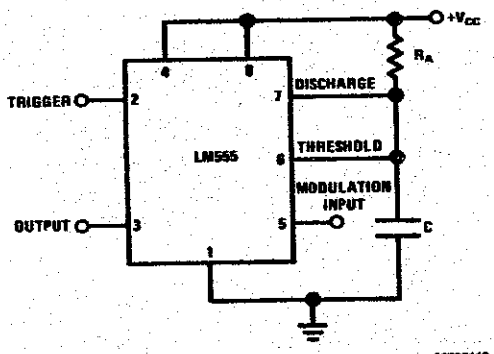


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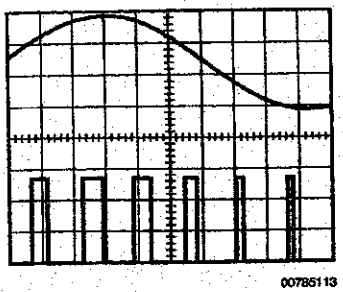
FIGURE 8. Pulse Width Modulator

Applications Information (Continued)



V_{CC} = 5V
TIME = 0.2 ms/DIV.
R_A = 9.1kΩ
C = 0.01µF

Top Trace: Modulation 1V/Div.
Bottom Trace: Output Voltage 2V/Div.

FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

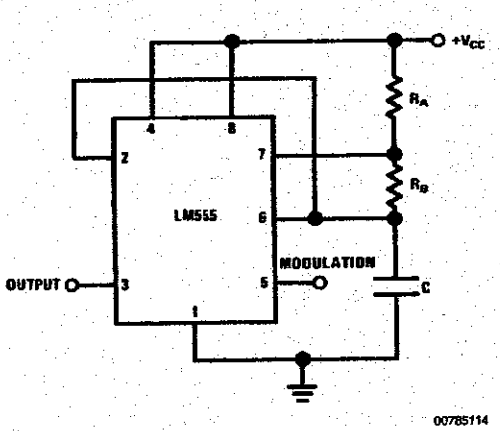
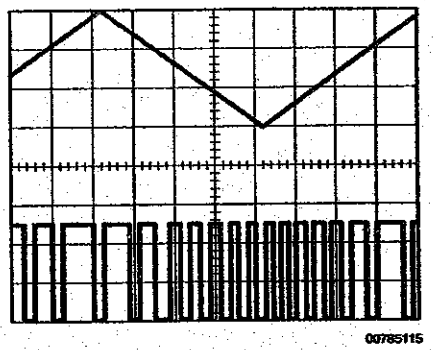


FIGURE 10. Pulse Position Modulator



V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.

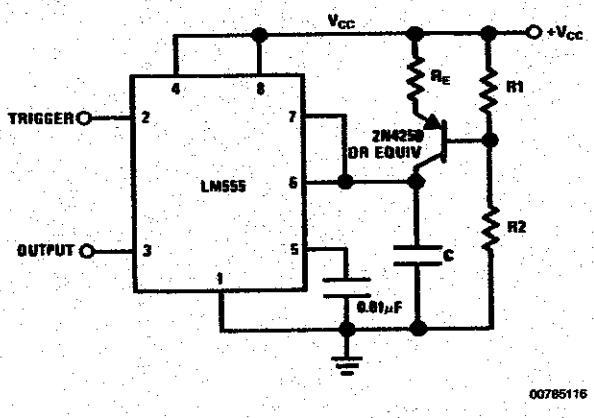


FIGURE 12.

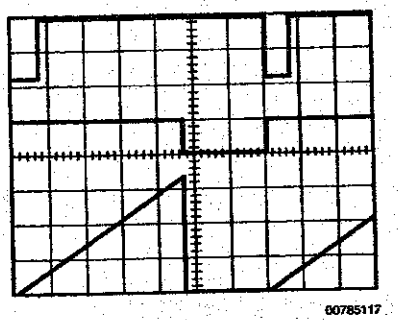
Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} \cong 0.6V$$

Applications Information (Continued)



00785117

V_{CC} = 5V Top Trace: Input 3V/Div.
TIME = 20µs/DIV. Middle Trace: Output 5V/Div.
R_1 = 47kΩ Bottom Trace: Capacitor Voltage 1V/Div.
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 µF

FIGURE 13. Linear Ramp

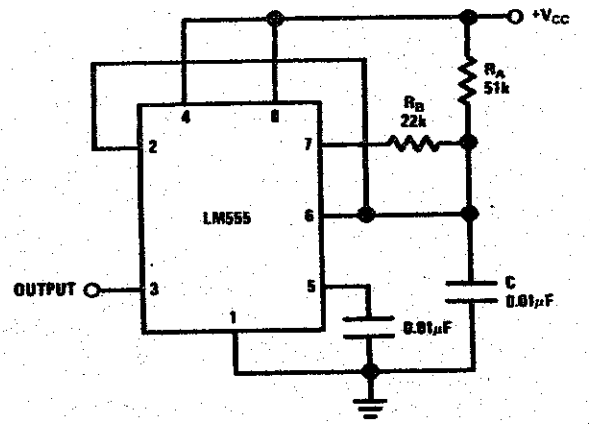
50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ ln\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$



00785118

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

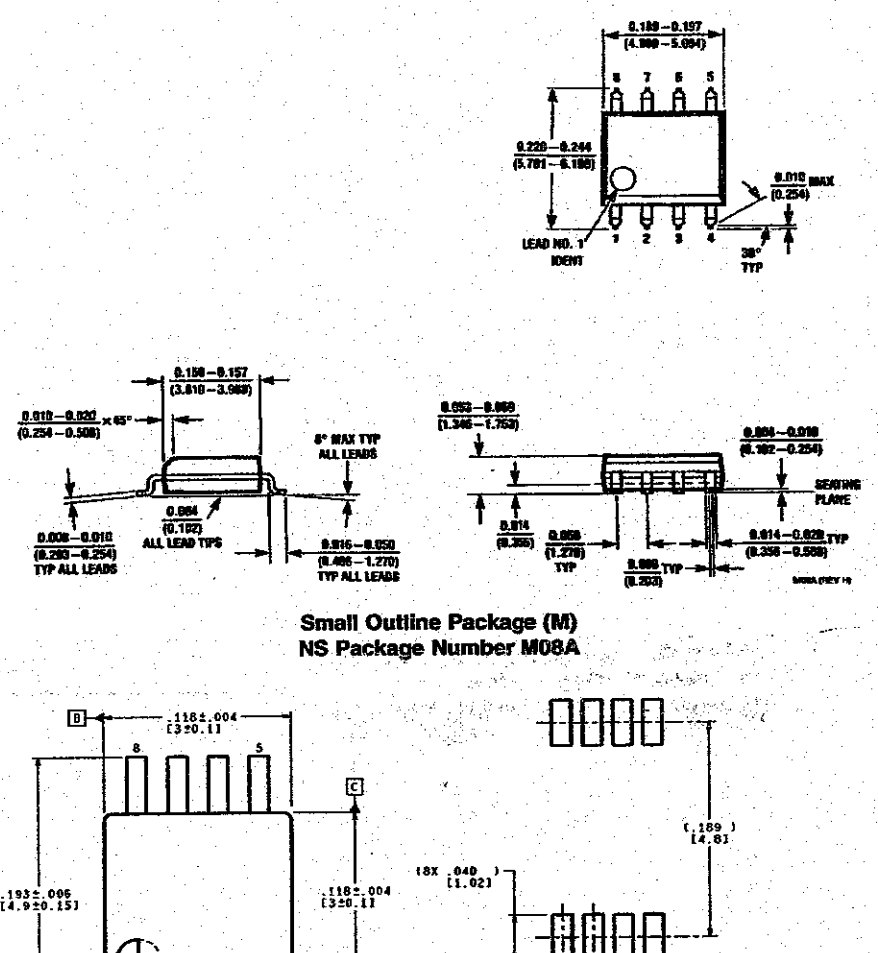
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

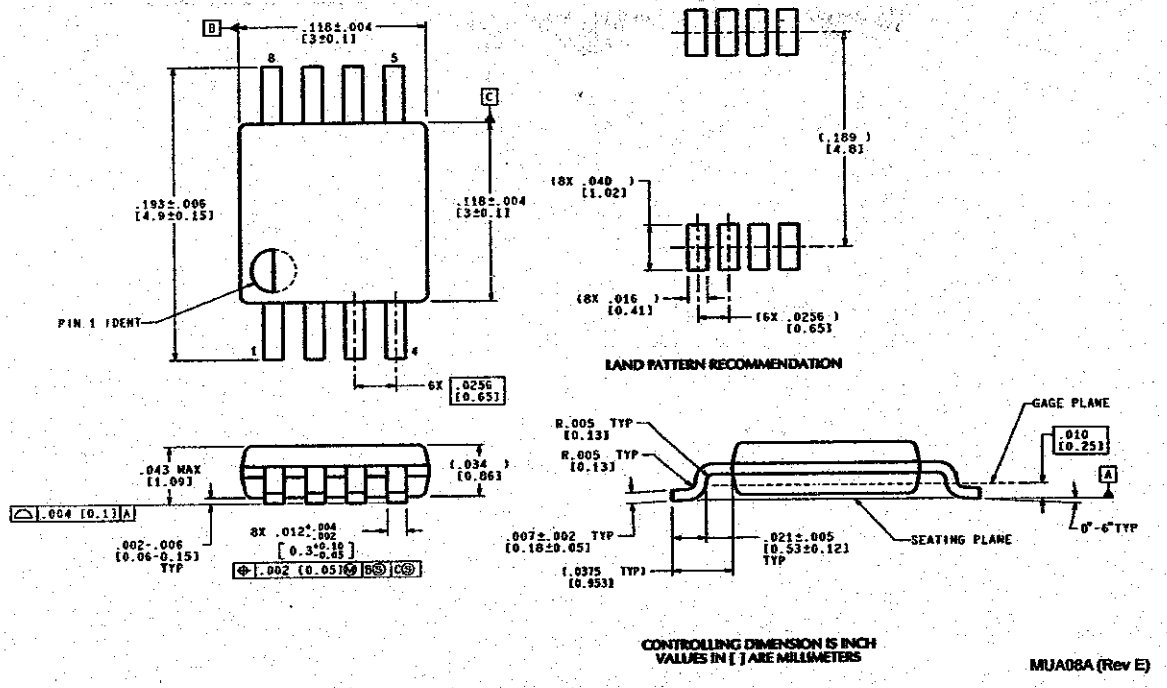
Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters) unless otherwise noted

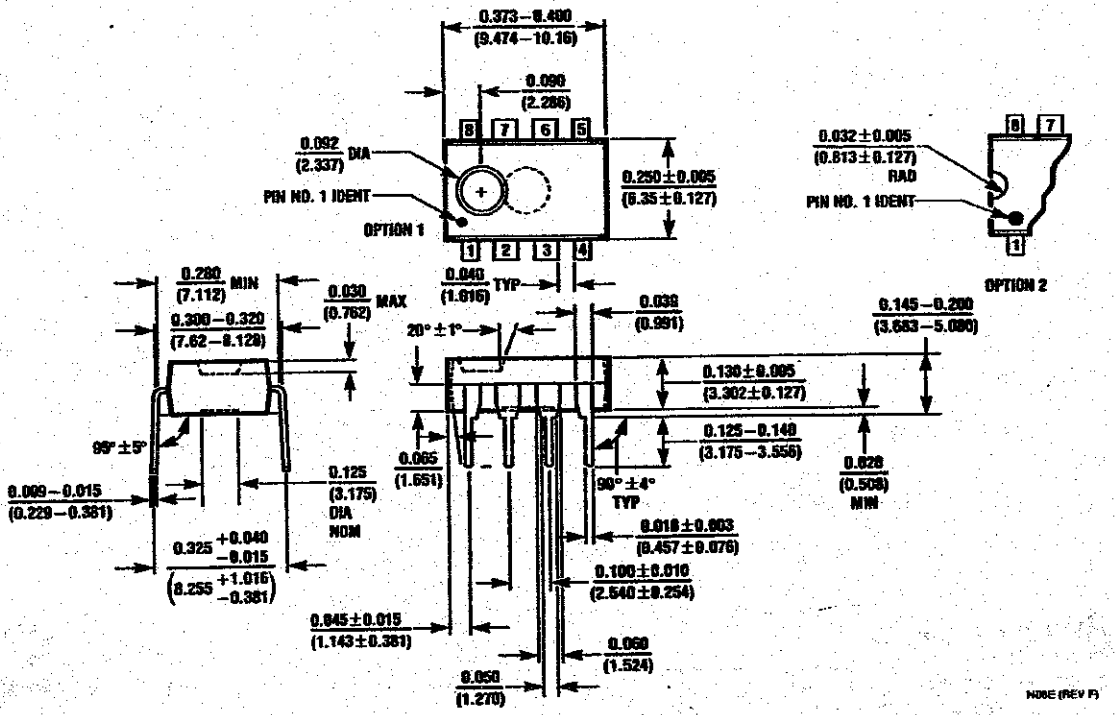


Small Outline Package (M)
NS Package Number M08A



8-Lead (0.118" Wide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

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SHANGHAI SUNRISE ELECTRONICS CO., LTD.

IN4148

SILICON EPITAXIAL PLANAR
SWITCHING DIODE

REVERSE VOLTAGE: 75V
FORWARD CURRENT: 150mA

TECHNICAL SPECIFICATION

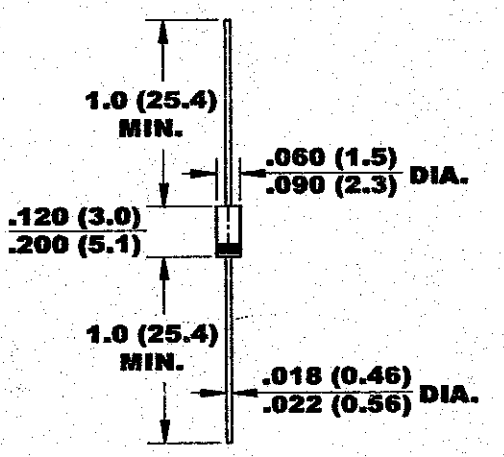
FEATURES

- Small glass structure ensures high reliability
- Fast switching
- Low leakage
- High temperature soldering guaranteed:
  250°C/10S/9.5mm lead length
  at 5 lbs tension

MECHANICAL DATA

- Terminal: Plated axial leads solderable per MIL-STD 202E, method 208C
- Case: Glass,hermetically sealed
- Polarity: Color band denotes cathode
- Mounting position: Any

DO - 35



Dimensions in inches and (millimeters)

MAXIMUM RATINGS AND CHARACTERISTICS

(Ratings at 25°C ambient temperature unless otherwise specified)

RATINGS	SYMBOL	VALUE	UNITS
Reverse Voltage	V_R	75	V
Peak Reverse Voltage	V_{RM}	100	V
Forward Current (average)	I_O	150	mA
Repetitive Forward Peak Current	I_{FRM}	300	mA
Forward Voltage (I_F=10mA)	V_F	1	V
Reverse Current (V_R=20V)	I_{R1}	25	nA
Reverse Current (V_R=75V)		5	μA
Reverse Current (V_R=20V,T_J=100°C)	I_{R2}	50	μA
Capacitance (note 1)	Ct	4	pF
Reverse Recovery Time (note 2)	I_F	4	nS
Thermal Resistance (junction to ambient) (note 3)	R_θ(ja)	0.35	°C/mW
Operating Junction and Storage Temperature Range	T_{STG},T_J	-55 ~+175	°C

Notes:

1: V_R=0V, f=1 MHz

2: I_F=10mA to I_R=1mA, V_R=6V, R_L=100Ω

3: Valid provided that leads are kept at ambient temperature at a distance of 8mm from case.

http://www.sse-diode.com

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4017
Johnson decade counter with 10 decoded outputs

Product specification
File under Integrated Circuits, IC06

December 1990

Philips
Semiconductors

PHILIPS

Johnson decade counter with 10 decoded outputs 74HC/HCT4017

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4017 are high-speed Si-gate CMOS devices and are pin compatible with the "4017" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4017 are 5-stage Johnson decade counters with 10 decoded active HIGH outputs (Q_0 to Q_9), an active LOW output from the most significant flip-flop ($\overline{Q}_{5\text{-}9}$), active HIGH and active LOW clock inputs (CP_0 and $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH-to-LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also function table).

When cascading counters, the $\overline{Q}_{5\text{-}9}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($Q_0 = \overline{Q}_{5\text{-}9}$ = HIGH; Q_1 to Q_9 = LOW) independent of the clock inputs (CP_0 and $\overline{CP}_1$).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP_0, $\overline{CP}_1$ to Q_n	C_L = 15 pF; V_{CC} = 5 V	20	21	ns
f_{max}	maximum clock frequency		77	67	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	35	36	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	Q_0 to Q_9	decoded outputs
8	GND	ground (0 V)
12	$\overline{Q}_{5\text{-}9}$	carry output (active LOW)
13	$\overline{CP}_1$	clock input (HIGH-to-LOW, edge-triggered)
14	CP_0	clock input (LOW-to-HIGH, edge-triggered)
15	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

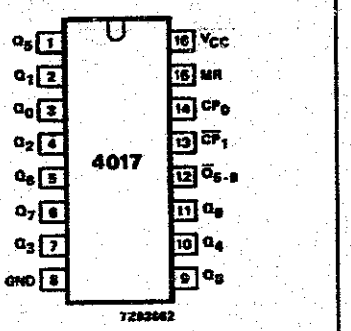


Fig.1 Pin configuration.

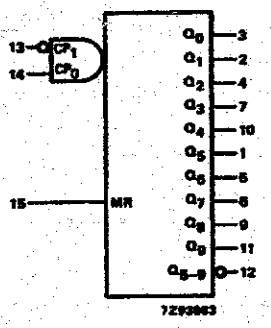


Fig.2 Logic symbol.

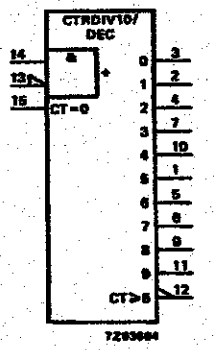


Fig.3 IEC logic symbol.

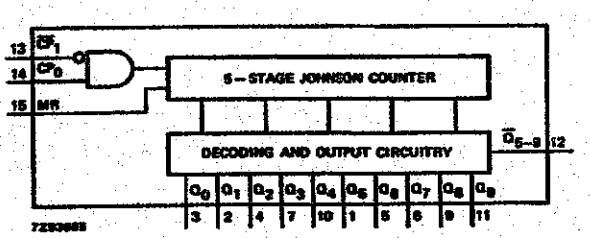


Fig.4 Functional diagram.

FUNCTION TABLE

MR	CP_0	$\overline{CP}_1$	OPERATION
H	X	X	$Q_0 = Q_{5-9} = H$; Q_1 to $Q_9 = L$
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH clock transition
   ↓ = HIGH-to-LOW clock transition

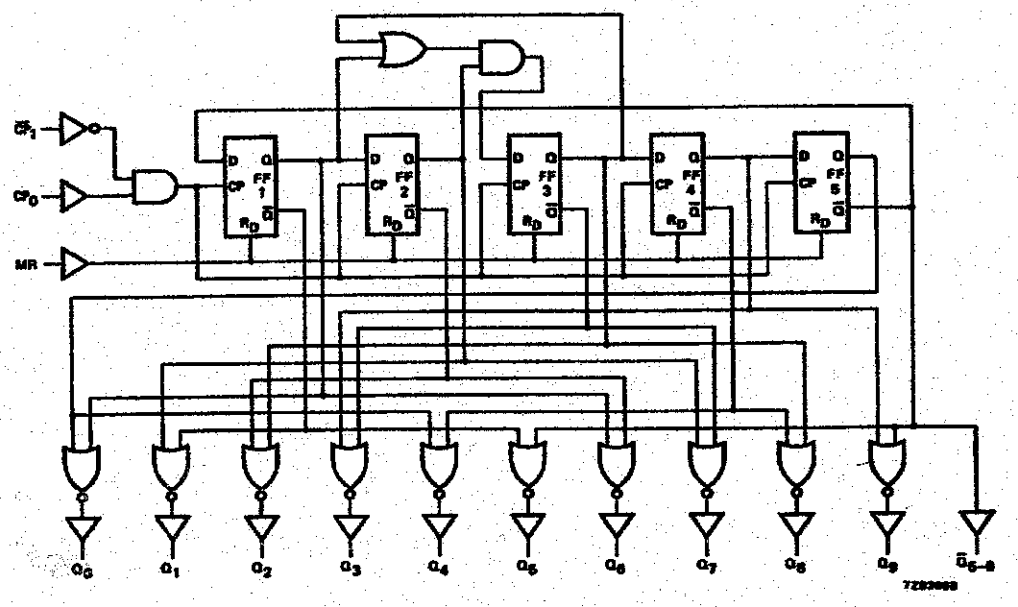


Fig.5 Logic diagram.

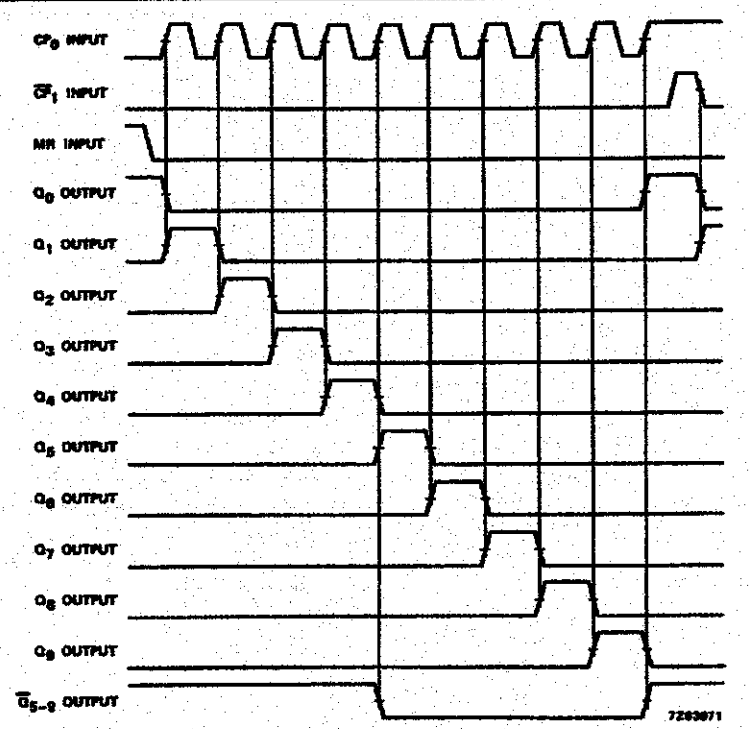


Fig.6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to+85		−40 to+125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP_0 to Q_n		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.9
t_{PHL}/t_{PLH}	propagation delay CP_0 to $\overline{Q}_{5\text{-}9}$		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.9
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to Q_n		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.9
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_1$ to $\overline{Q}_{5\text{-}9}$		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.9
t_{PHL}	propagation delay MR to $Q_{1\text{-}9}$		52 19 15	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.8
t_{PLH}	propagation delay MR to $\overline{Q}_{5\text{-}9}$, Q_0		55 20 16	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.9
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t_W	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t_{rem}	removal time MR to CP_0, $\overline{CP}_1$	5 5 5	−17 −6 −5		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.8
t_{su}	set-up time $\overline{CP}_1$ to CP_0; CP_0 to $\overline{CP}_1$	50 10 9	−8 −3 −2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.7
t_h	hold time CP_0 to $\overline{CP}_1$; CP_1 to $\overline{CP}_0$	50 10 9	17 6 5		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.7
f_{max}	maximum clock pulse frequency	6.0 30 25	23 70 83		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}_1$	0.40
CP_0	0.25
MR	0.50

AC CHARACTERISTICS FOR 74HCT

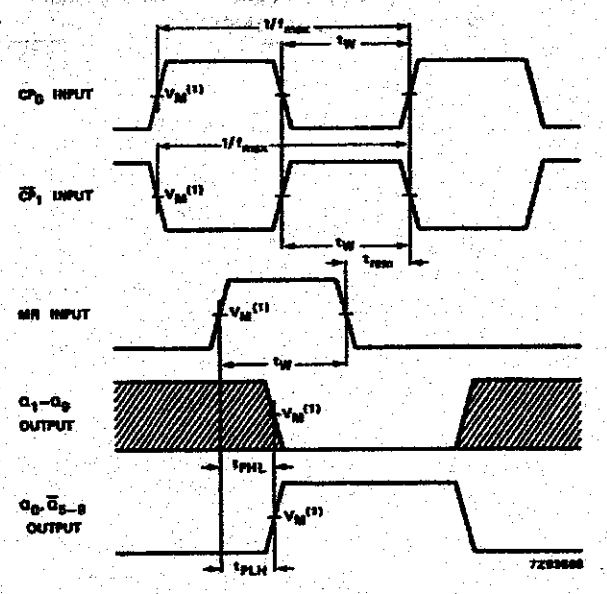
GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to+85		–40 to+125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP_0 to Q_n		25	46		58		69	ns	4.5	Fig.9
t_{PHL}/ t_{PLH}	propagation delay CP_0 to $\overline{Q}_{5-9}$		25	46		58		69	ns	4.5	Fig.9
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}_1$ to Q_n		25	50		63		75	ns	4.5	Fig.9
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}_1$ to $\overline{Q}_{5-9}$		25	50		63		75	ns	4.5	Fig.9
t_{PHL}	propagation delay MR to Q_{1-9}		22	46		58		69	ns	4.5	Fig.8
t_{PLH}	propagation delay MR to $\overline{Q}_{5-9}$, Q_0		20	46		58		69	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.9
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.8
t_W	master reset pulse width; HIGH	16	4		20		24		ns	4.5	Fig.8
t_{rem}	removal time MR to CP_0, $\overline{CP}_1$	5	–5		5		5		ns	4.5	Fig.8
t_{su}	set-up time $\overline{CP}_1$ to CP_0; CP_0 to $\overline{CP}_1$	10	–3		13		15		ns	4.5	Fig.7
t_h	hold time CP_0 to $\overline{CP}_1$; $\overline{CP}_1$ to CP_0	10	6		13		15		ns	4.5	Fig.7
f_{max}	maximum clock pulse frequency	30	61		24		20		ns	4.5	Fig.8

AC WAVEFORMS

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

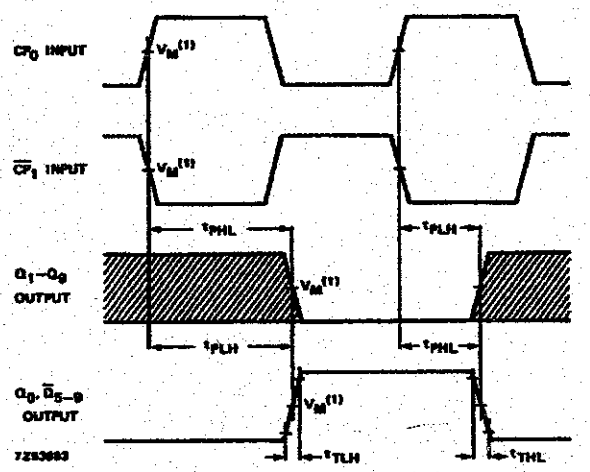
Fig.7 Waveforms showing the hold and set-up times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0.



Conditions:
$\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW-to-HIGH transition and CP_0 = HIGH, while $\overline{CP}_1$ is triggered on a HIGH-to-LOW transition.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the minimum pulse widths for CP_0, $\overline{CP}_1$ and MR inputs; the recovery time for MR and the propagation delays for MR to Q_n and $\overline{Q}_{5-9}$ outputs.



Conditions:
$\overline{CP_1}$ = LOW while CP_0 is triggered on a LOW-to-HIGH transition and CP_0 = HIGH, while $\overline{CP_1}$ is triggered on a HIGH-to-LOW transition.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

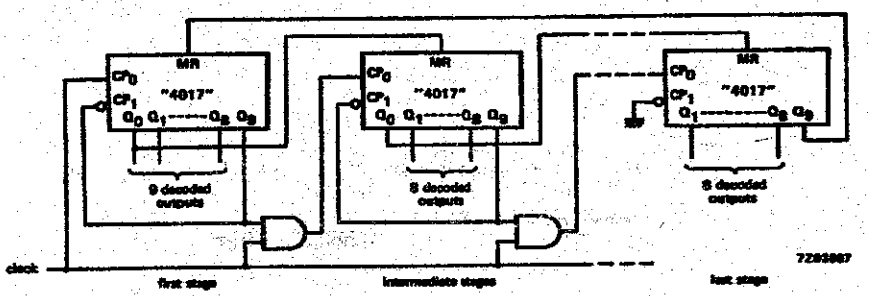
Fig.9 Waveforms showing the propagation delays for CP_0, $\overline{CP_1}$ to Q_n, $\overline{Q}_{5-9}$ outputs and the output transition times.

APPLICATION INFORMATION

Some applications for the "4017" are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

Figure 10 shows a technique for extending the number of decoded output states for the "4017". Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



It is essential not to enable the counter on $\overline{CP}_1$ when CP_0 is HIGH, or on CP_0 when $\overline{CP}_1$ is LOW, as this would cause an extra count.

Fig.10 Counter expansion

Figure 11 shows an example of a divide-by 2 through divide-by 10 circuit using one "4017". Since "4017" has an asynchronous reset, the output pulse widths are narrow (minimum expected pulse width is 6 ns). The output pulse widths can be enlarged by inserting a RC network at the MR input.

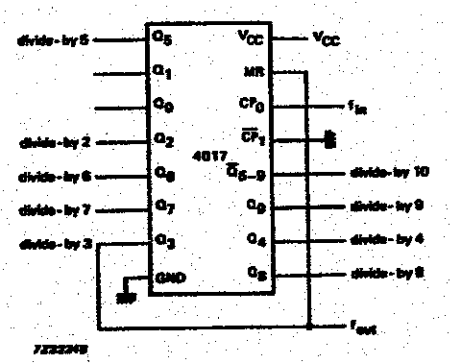


Fig.11 Divide-by 2 through divide-by 10.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

SN74107, SN74LS107A
DUAL J-K FLIP-FLOPS WITH CLEAR

SDLS036 – DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

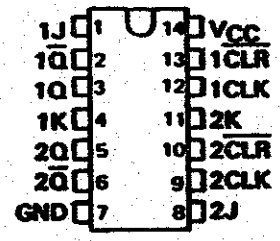
description

The '107 contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '107 is a positive pulse-triggered flip-flop. The J-K input data is loaded into the master while the clock is high and transferred to the slave and the outputs on the high-to-low clock transistion. For these devices the J and K inputs must be stable while the clock is high.

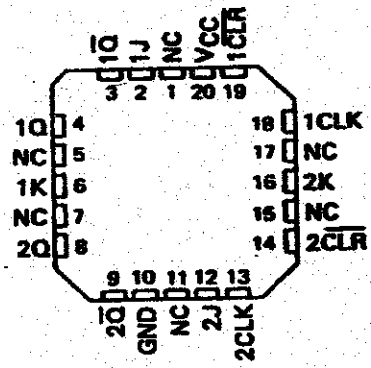
The 'LS107A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the $\overline{Q}$ output high.

The SN54107 and the SN54LS107A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74107 and the SN74LS107A are characterized for operation from 0°C to 70°C.

SN54107, SN54LS107A . . . J PACKAGE
SN74107 . . . N PACKAGE
SN74LS107A . . . D OR N PACKAGE
(TOP VIEW)



SN54LS107A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

'107
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q_0	$\overline{Q}_0$
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	

'LS107A
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

TEXAS INSTRUMENTS
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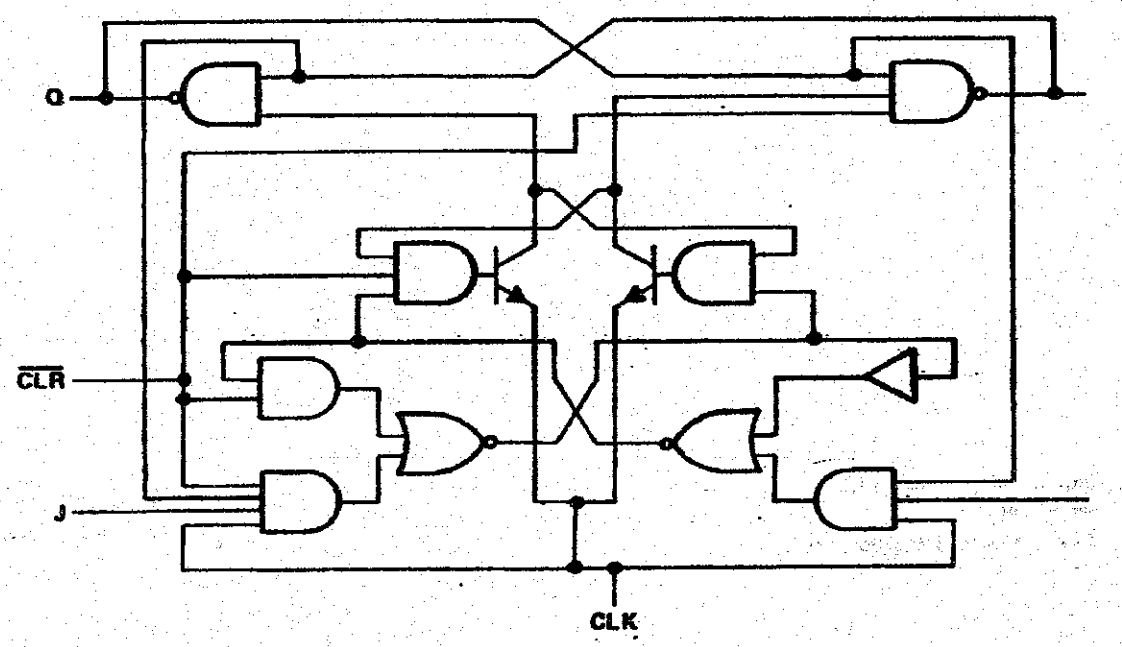
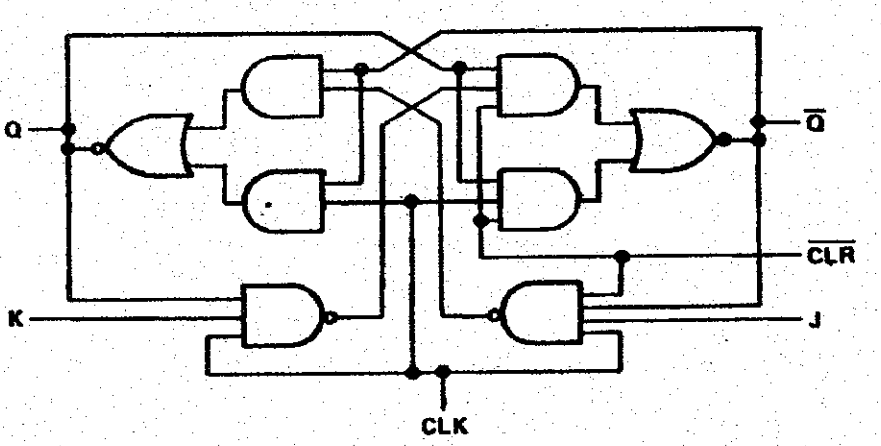
ogic diagrams (positive logic)

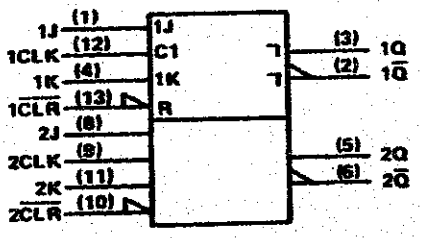


'LS107A

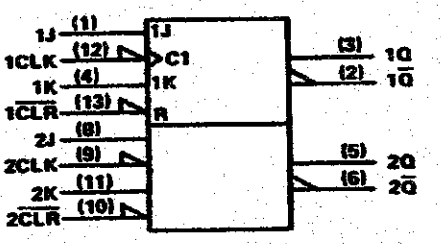


logic symbols†

'107



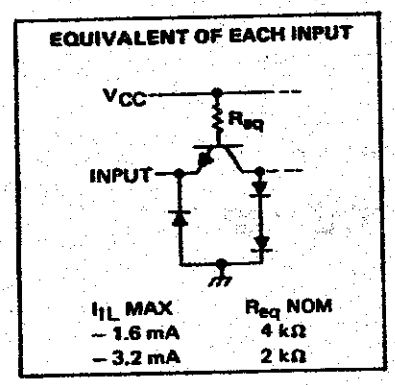
'LS107A

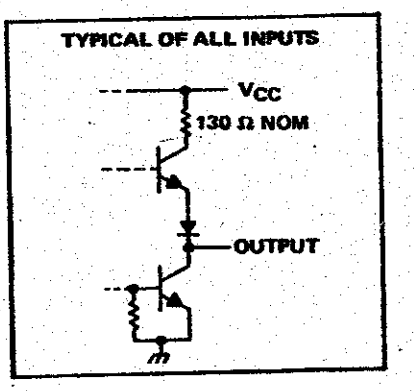


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

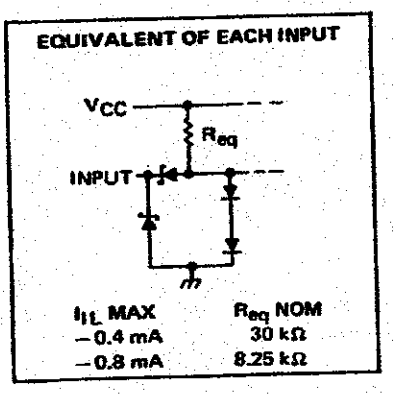
schematic of inputs and outputs

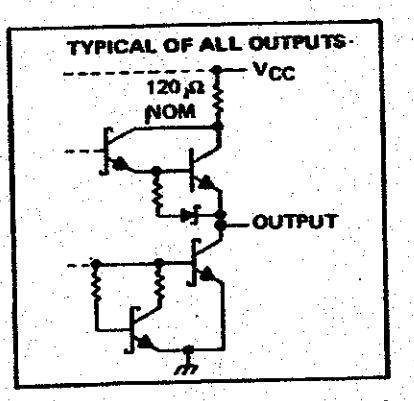
'107





'LS107A





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '107 . . . . . 5.5 V
'LS107A . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . –55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

commended operating conditions

			SN54107			SN74107			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high	20			20			ns
		CLK low	47			47			
		$\overline{CLR}$ low	25			25			
t_{su}	Input setup time before CLK↑		0			0			ns
t_h	Input hold time-data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

ectrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54107			SN74107			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 16 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	J or K	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
	All other						80			80	
I_{IL}	J or K	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
	All other						−3.2			−3.2	
I_{OS}§		V_{CC} = MAX			−20		−57	−18		−57	mA
I_{CC}¶		V_{CC} = MAX,	See Note 2			10	20		10	20	mA

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
All typical values are at V_{CC} = 5 V, T_A = 25° C.
Not more than one output should be shorted at a time.
Average per flip-flop.
OTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

witching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 400 Ω, C_L = 15 pF	15	20		MHz
t_{PLH}	$\overline{CLR}$	$\overline{Q}$			16	25	ns
t_{PHL}		Q			25	40	ns
t_{PLH}	CLK	Q or $\overline{Q}$			16	25	ns
t_{PHL}					25	40	ns

OTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54LS107A			SN74LS107A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		30	MHz
t_w	Pulse duration	CLK high	20			20			ns
		$\overline{CLR}$ low	25			25			
t_{su}	Setup time before CLK↓	data high or low	20			20			ns
		$\overline{CLR}$ inactive	25			25			
t_h	Hold time-data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS107A			SN74LS107A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = MAX,	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 4 mA	V_{IL} = MAX,	V_{IH} = 2 V,		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 8 mA	V_{IL} = MAX,	V_{IH} = 2 V,					0.35	0.5	
I_I	J or K	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
	CLR						0.3			0.3	
	CLK						0.4			0.4	
I_{IH}	J or K	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
	CLR						60			60	
	CLK						80			80	
I_{IL}	J or K	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
	CLR or CLK						−0.8			−0.8	
I_{OS}§		V_{CC} = MAX,	See Note 4		−20		−100	−20		−100	mA
I_{CC} (Total)		V_{CC} = MAX,	See Note 2			4	6		4	6	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	$\overline{CLR}$ or CLK	Q or $\overline{Q}$	R_L = 2 kΩ,	C_L = 15 pF	30	45		MHz
t_{PLH}						15	20	ns
t_{PHL}						15	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

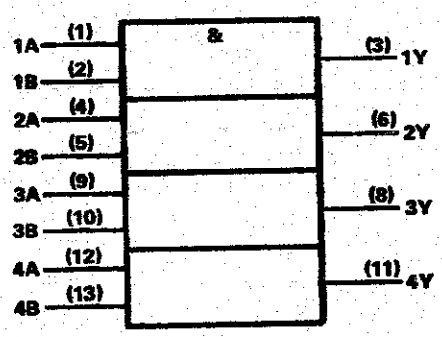
These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7408, SN74LS08 and SN74S08 are characterized for operation from 0° to 70°C.

FUNCTION TABLE (each gate)

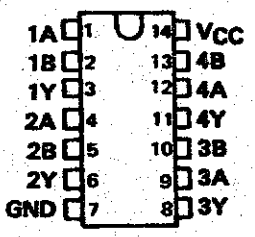
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

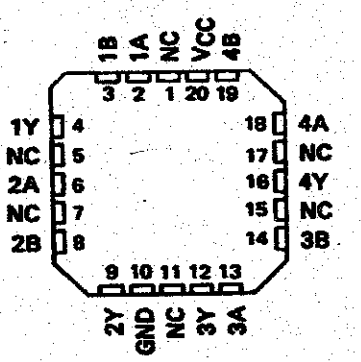


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

SN5408, SN54LS08, SN54S08 . . . J OR W PACKAGE
SN7408 . . . J OR N PACKAGE
SN74LS08, SN74S08 . . . D, J OR N PACKAGE
(TOP VIEW)

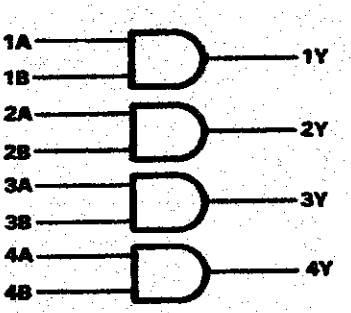


SN54LS08, SN54S08 . . . FK PACKAGE
(TOP VIEW)



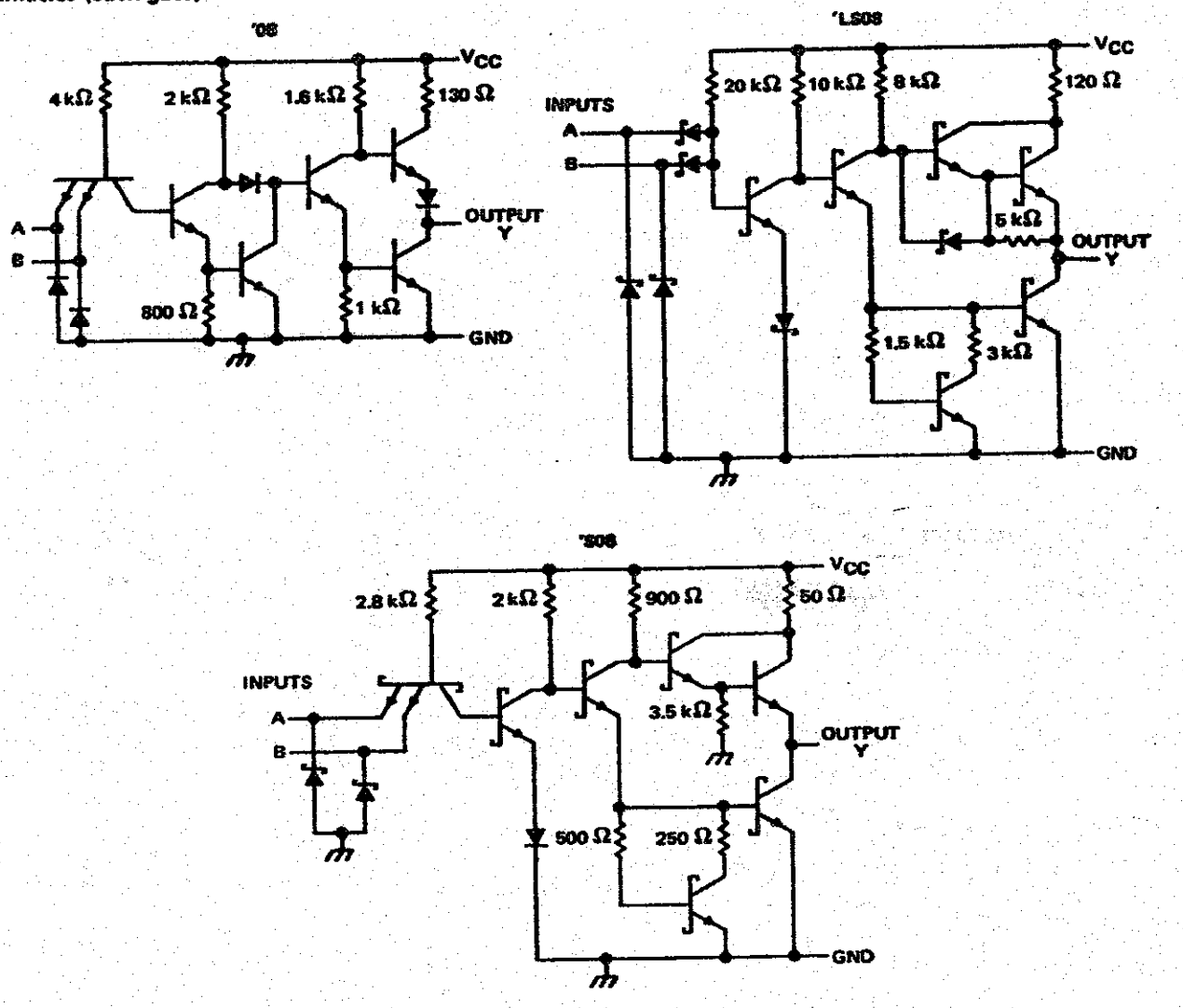
NC—No internal connection

logic diagram (positive logic)



$Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$

hematics (each gate)



esistor values are nominal.

bsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '08, 'S08 . . . . . 5.5 V
'LS08 . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5408			SN7408			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.8			−0.8	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5408			SN7408			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −0.8 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, V_I = 4.5 V		11	21		11	21	mA
I_{CCL}	V_{CC} = MAX, V_I = 0 V		20	33		20	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		17.5	27	ns
t_{PHL}					12	19	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

commended operating conditions

		SN54LS08			SN74LS08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

ectrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †			SN54LS08			SN74LS08			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = MIN,	V_{IL} = MAX,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 4.5 V			2.4	4.8		2.4	4.8	mA
I_{CCL}	V_{CC} = MAX,	V_I = 0 V			4.4	8.8		4.4	8.8	mA

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
All typical values are at V_{CC} = 5 V, T_A = 25°C
Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

witching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ,	C_L = 15 pF		8	15	ns
t_{PHL}						10	20	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54S08			SN74S08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †				SN54S08			SN74S08			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA					−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OH} = −1 mA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IL} = 0.8 V	I_{OL} = 20 mA				0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V					1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V					50			50	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V					−2			−2	mA
I_{OS}§	V_{CC} = MAX				−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 4.5 V				18	32		18	32	mA
I_{CCL}	V_{CC} = MAX,	V_I = 0 V				32	57		32	57	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω,	C_L = 15 pF		4.5	7	ns
t_{PHL}						5	7.5	ns
t_{PLH}			R_L = 280 Ω,	C_L = 50 pF		6		ns
t_{PHL}						7.5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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